

Dynamic Behavior of the TLV320DAC23 and the TLV320AIC23B

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ABSTRACT

This application report discusses the following topics:

1. The operation based on various settings of the power-down control register.
2. The time it takes to be stable after returning from a power-down control command.
3. A list of power sequence restrictions.
4. The results of changing the external capacitors on VMID.
5. IIC communication
6. How the sample rate varies proportionally with a change in MCLK while the DAC is in master mode.

DISCLAIMER: The information contained in this document is based on lab evaluations using a limited supply of samples. This document is not intended to replace the TLV320DAC23 or TLV320AIC23B data manuals or is it in anyway a device specification. Values in this document are not assured for every TLV320DAC23 or TLV320AIC23B device. If there are any discrepancies between this document and the data manual, the data manual will prevail.

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1 Power-Down Control Settings

There are various software programmable modes to conserve power. See the power-down control register address 0000110 section in the data manual for more clarification. Described below is each bit of this register and how each bit responds to being toggled.

1.1 D0 Line Input

Function: Powers down both line inputs.

Effect: Can be done dynamically without any audible effects on the DAC or line outputs.

1.2 D3 DAC

Function: Powers down both the DAC and DAC filters.

Effect: If done dynamically, audible pops and clicks on the DAC.

Solution: SoftMute the DAC bit D3 register 0000101. Deselect the DAC bit D4 register 0000100. Power down the DAC.

1.3 D4 OUT

Function: Powers down both the line and headphone outputs.

Effect: If done dynamically audible pops and clicks on the DAC.

Solution: SoftMute the DAC bit D3 reg 0000101.

1.4 D5 Oscillator

Function: Powers off the on-board crystal oscillator.

Effect: MCLK still functions with the oscillator being powered down. Preliminary tests show that the oscillator can be powered off and on dynamically without any audible effects on the DAC or line outputs. Further verification might be required if this option is required.

1.5 D6 Clock

Function: Powers off the CLKOUT pin. CLKOUT pin is powered low when turned off.

1.6 D7 Device Power

Function: In this power-down mode the control interface is still active. The analog VMID reference is disabled. Due to the VMID being disabled, audible effects will be heard when it is turned back on.

Effect: This conserves power, reduces digital noise, and RF emissions.

1.7 Standby Mode

In standby mode, the control interface and the VMID reference are still active.

LINE = OFF Bit D0

DAC = OFF Bit D3

OUT = OFF Bit D4

The OSC (D5) and CLK (D6) can be turned off if they are not being used to generate the system master clock.

The device transmits audio without any audio imperfections after leaving the standby mode. The TLV320DAC23 maintains all previous settings, therefore it will be ready to receive and transmit data immediately after returning to active mode.

1.8 Power-Down Mode

OFF = OFF Bit D7

The device transmits audio without any audio imperfections after leaving the power-down mode. The TLV320DAC23 maintains all previous settings, therefore it will be ready to receive and transmit data immediately after returning to active mode.

2 Noise Fixed by Toggling Bit D7 of Power-Down Control

The TLV320DAC23 experiences noise on the analog output on one or both channels when the MCLK is removed. This noise occurs about 20% of the time when the MCLK is removed. The MCLK is removed as a power saving measure within the DSP. It is good practice to always power up bit D7 of the power-down control register last.

2.1 Lab Setup

The TLV320AIC23 was used for this experiment so that I could feed analog into the ADC and loop the digital data out back into the DAC. The analog input signal is a 1-kHz single tone, but it can be varied up to 24 kHz. The analog signal is being generated using an audio precision analyzer. The MCLK is running at 12.288 MHz and the device is in master mode. The TLV320AIC23 EVM2 is being used to control the I2C data from the graphical user interface (GUI) software.

2.2 Lab Testing Process

The analog output from the DAC is monitored on the oscilloscope and should produce a clean 1-kHz sine wave. The MCLK can be connected-disconnected-connected multiple times while the device is running and streaming audio. About 20% of the time, the MCLK can be disconnected and upon reconnection, a 48-kHz noise can be seen riding upon the 1-kHz output. The level of the noise is about 154-mV peak-to-peak and the level of the 1-kHz signal is about 1.44-V peak-to-peak.

2.3 Lab Correlation

Note that the 48-kHz noise is the same frequency as the sample rate. If the sample rate is changed to 8 kHz, then the noise changes to 8 kHz. This shows that the digital filters are not being reinitialized after the MCLK is removed. This fits with hearing the problem mostly at 8-kHz, 11-kHz, 12-kHz, and 16-kHz melodies. The 48-kHz noise cannot be heard because it is out of the audio band.

2.4 Lab Conclusion

Various commands have been tried to clear the noise. However, toggling bit D7 on the powerdown control register clears the noise every time.

3 Power-Up Stability Time

This section discusses the time it takes for the TLV320DAC23 to be stable after returning from a power-down control command. This occurs by toggling bit D7 of the power-down control register (address 0000101).

A TLV320AIC23 EVM was configured in USB mode with an MCLK of 6 MHz and programmed with a sample rate of 48 kHz. A 1-kHz full-scale sine wave was recorded on a CD and connected to the Line In of the TLV320AIC23 EVM. The EVM was configured in a loop back mode, so that the *Digital Out* of the TLV320AIC23 was feed back in to the *Digital In* of the TLV320AIC23.

The headphone out was monitored on an oscilloscope. The oscilloscope was triggered on the IIC SCL transaction of the power-up command. The time from the end of the power-up transaction to the point where the sine wave became stable ranged from 346 μ s to 384 μ s. Therefore, 400 μ s is a safe value, but it cannot be assured for all cases. Note that this time includes the transaction through the analog-to-digital converter and back through the digital-to-analog converter; therefore, the time for just the digital-to-analog converter (TLV320DAC23) to be stable may be less.

4 Power Sequence

4.1 Power Restrictions

The digital supply voltage (DVDD) must always be less than or equal to the analog supply voltage (AVDD). The digital supply voltage (DVDD) must always be less than or equal to the digital buffer supply voltage (BVDD). The digital buffer supply voltage (BVDD) must always be less than or equal to the analog supply voltage (AVDD).

DVDD must always be less than or equal to BVDD. Also, BVDD must always be less than or equal to AVDD and BVDD must always be less than or equal to HPVDD. This is summarized below.

- DVDD may not exceed BVDD
- BVDD may not exceed AVDD
- BVDD may not exceed HPVDD

Therefore:

- $DVDD \leq BVDD$
- $BVDD \leq AVDD$
- $BVDD \leq HPVDD$
- $DVDD \leq AVDD$
- $DVDD \leq HPVDD$

4.2 Power Up

The power restrictions are easy to meet if all voltages are tied together to the same value. It may be desired to operate DVDD at 1.8 V and set the remaining voltages at 3.3 V. In this case the power up sequence of each voltage is important, since the 1.8-V supply may come up first and violate the rules.

Since operating DVDD at 1.8 V is intended to save power, we first had to determine if operating DVDD at 1.8 V would actually lead to lower power consumption. This has been verified with an TLV320AIC23 running in master mode, OSC off and all voltages set to 3.26 V. DVDD was connected through a 2.2- Ω resistor. The input voltage was varied from 3.26 V down to 1.42 V. There is a reduction in power consumption over this range and Table 1 shows these results. Note that these measurements are only a reference using a crude lab arrangement and these values should not be used to imply performance of the TLV320AIC23 or TLV320DAC23 under all circumstances.

Table 1. Reduction in Power Consumption Results

Resistor	DVDD ⁽¹⁾	MV	mA	mW
2.20	3.26	10.96	4.98	16.24
2.20	3.1	10.26	4.66	14.46
2.20	3	9.8	4.45	13.36
2.20	2.8	9	4.09	11.45
2.20	2.6	8.18	3.72	9.67
2.20	2.4	7.36	3.35	8.03
2.20	2.2	6.65	3.02	6.65
2.20	2	5.9	2.68	5.36
2.20	1.8	5.26	2.39	4.3
2.20	1.6	4.6	2.09	3.35
2.20	1.42	4.03	1.83	2.6

⁽¹⁾ NOTE: The THD+N measurements were not done at these low power settings of DVDD.

4.3 Power-Up Sequence Suggestion

To control the power-up sequence a transistor or FET may be used. Drive the base of the transistor with voltage X, where voltage X must always be higher than DVDD. Switch the transistor to ensure that DVDD is never present, unless voltage X is present and of sufficient value. In this case, AVDD, HPVDD, and BVDD are all equal to voltage X and it is set to 3.3 V.

4.4 Power-Down Sequence

Verify that DVDD is powered off first or at the same time as AVDD, HPVDD, and BVDD.

5 VMID Capacitor Variations

The capacitor values at VMID on the TLV320AIC23 EVM are 10 μ F in parallel with 0.1- μ F capacitor. This information is available in the AIC23EVM2 user's guide (SLEU016). This document is available on the Texas Instruments web site.

A 4.7- μ F capacitor in parallel with a 0.1- μ F capacitor has been recommended. Due to space constraints, it is recommended to have two 1- μ F capacitors in parallel and have them in parallel with 0.1- μ F capacitor. This will probably be sufficient if the low frequency noise of the system is well controlled.

Figure 1 shows the theoretical low frequency attenuation for each of the three capacitors. The three capacitors in the chart are 10.1 μ F, 4.8 μ F, and 2.1 μ F. The equivalent resistance of the two 50-k Ω resistors internal to the TLV320DAC23 is 25 k Ω . This analysis is theoretical and does not accurately account for internal leakage characteristics of the capacitors. It is recommended that the 0.1- μ F capacitor remain separate.

$$\text{Freq 3 db} = 1 / (2 \pi \times 25 \text{ k}\Omega \times 10.1 \mu\text{F}) = 0.63 \text{ Hz}$$

$$\text{Freq 3 db} = 1 / (2 \pi \times 25 \text{ k}\Omega \times 4.8 \mu\text{F}) = 1.32 \text{ Hz}$$

$$\text{Freq 3 db} = 1 / (2 \pi \times 25 \text{ k}\Omega \times 2.1 \mu\text{F}) = 3.03 \text{ Hz}$$

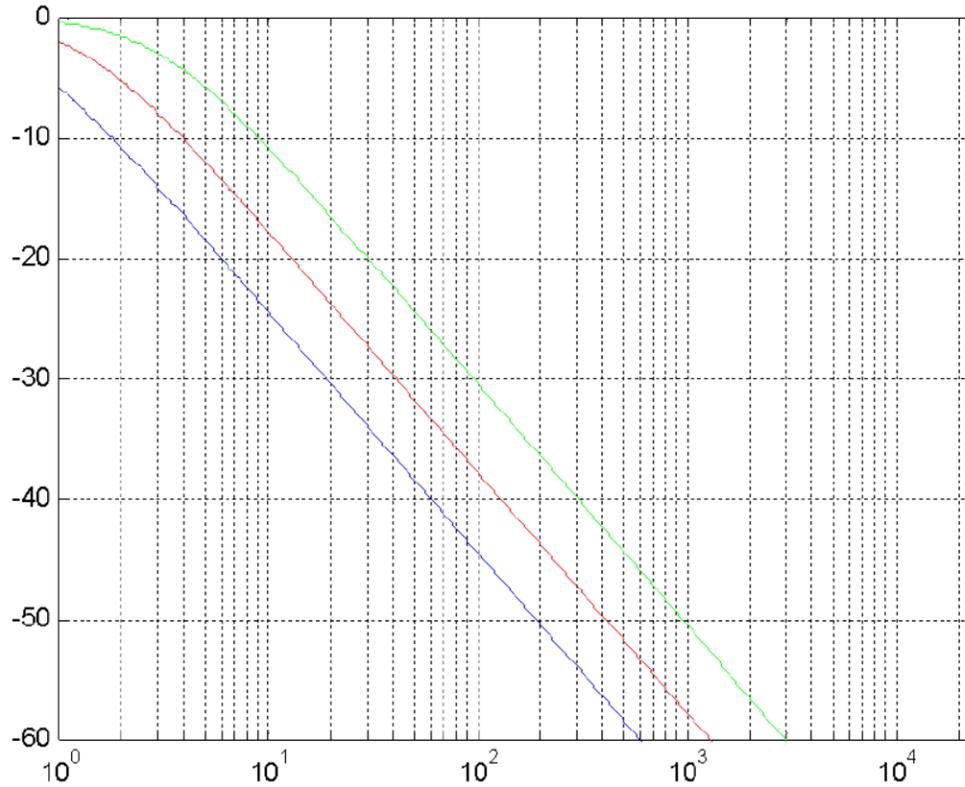


Figure 1. Theoretical Low-Frequency Attenuation

6 TLV320DAC23 IIC Communication

This section describes the general communication protocol to the TLV320DAC23 with examples.

Three bytes for each IIC command must be sent:

1. The IIC address is the first byte.
2. The second byte consists of the register address plus D8 of the data.
3. The D7–D0 of the data comprises the third byte.

The tricky part is the data is 9 bits long, which means bit D8 of the data is bit D0 of the register address. To write 0xFF to the PD control register, you must write the following:

- 0x34 0x0C 0xFF

NOTE: The PD control register address is address 0x06, but 0x0C must be sent since the first bit is carried over from the data.

The following gives more examples of I2C registers settings:

- 0x34 0x00 0x00 (Left Line Input Control: Unmuted)
- 0x34 0x02 0x00 (Right Line Input Control: Unmuted)
- 0x34 0x0C 0x06 (Power Down Control: line = on, DAC = on, out = on, CLK = on, OSC = on)
- 0x34 0x08 0x10 (Analog Audio Path Control: bypass = disabled)
- 0x34 0x0E 0x00 (Digital Audio Interface Format: Right Justified 16 bits)
- 0x34 0x10 0xA0 (Sample Rate Control: CLKOUT=MCLK/2, Sample Rate = 44.1 kHz)
- 0x34 0x12 0x01 (Digital Interface Activation: ActivateInterface = Active)
- 0x34 0x04 0x01 (Left Headphone Volume Control: ZC = on, volume = +6 dB)
- 0x34 0x06 0x01 (Right Headphone Volume Control: ZC = on, volume = +6 dB)

7 Sample Variance With MCLK Changes

The section describes how the sample rate of the TLV320DAC23 varies proportionally with a change in MCLK, while the DAC is in master mode. In [Table 2](#), the specified MCLK is 12 MHz and the specified sample rate (fs) is 48 kHz. The TLV320DAC23 device supports a proportional change in fs for each change in MCLK from their specified values. These tests were done in USB mode, but similar results were obtained in normal mode.

Table 2. Sample Rates

MCLK (Hz)	CLKIN	MODE	fs Setting (kHz)	fs Actual (Hz)	MCLK % Change	fs % Change
12000000	0	USB	48	48000	0%	0%
11000000				44000	-8.33%	-8.33%
10000000				40000	-16.67%	-16.67%
9000000				36000	-25%	-25%
8000000				32000	-33.33%	-33.33%
7000000				28000	-41.67%	-41.67%
6000000				24000	-50%	-50%
5000000				20000	-58.33%	-58.33%
4000000				16000	-66.67%	-66.67%
3000000				12000	-75%	-75%
2000000				8000	-83.33%	-83.33%
1000000				4000	-91.67%	-91.67%
500000				2000	-95.83%	-95.83%
250000				1000	-97.92%	-97.92%
100000				400	-99.17%	-99.17%
10000				40	-99.92%	-99.92%
1000				4	-99.99%	-99.99%

Changes from Original (June 2004) to A Revision
Page

- Updated to latest format and removed *Preliminary* watermark..... 1

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