

# **TVP5154 PCB Layout Guidelines**

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## **1 PCB Layer Stack**

TI recommends using at least four layers in the PCB layout to ensure proper isolation between the signals, the power supplies, and the grounds. The following layer stack is used in the EVM design:

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|---------------|--------------------------|
| 1. Top        | Signal layer             |
| 2. Internal 1 | Split ground plane layer |
| 3. Internal 2 | Power plane layer        |
| 4. Bottom     | Signal layer             |

The Top and Bottom layers are reserved for signals. The Internal 2 layer is a power plane where all power supplies are assigned to their own area or region within the layer.

The Internal 1 layer is considered a split ground plane. The analog and digital areas of the TVP5154 EVM are isolated throughout the board by using a split of a 30-mil trace between the regions. The analog and digital areas of the TVP5154 EVM are then connected via ferrite beads as close to the power source as possible. This helps minimize the coupling of digital noise into the analog signals and vice versa.

## **2 Layout Recommendations**

The following are only PCB layout recommendations based on methods commonly used in TI EVMs:

1. Maintain good insulation between four channels of the TVP5154 to minimize introduction of crosstalk.
2. Keep digital and analog signals away from crystal on every layer.
3. While using one ground plane, TI recommends using a split plane to isolate the analog and digital ground planes underneath the analog and digital supply voltages.
4. Do not route any signals or create a signal layer within the ground plane or the power plane.
5. Be sure that the power planes are the same size or smaller than their respective split ground planes.
6. Do not overlap the analog power plane with the digital ground plane and vice versa.
7. Do not place analog areas too close to the clock domain areas.
8. Do not cross another signal with the analog trace. If necessary, signals must be perpendicular.
9. Do not place digital signals in the analog areas.
10. Avoid long traces for analog signals, and use of guard (ground) trace is recommended.
11. Make the length of the digital trace for data and clock as equal as possible.
12. Place decoupling capacitors close to the power pins of the ICs. Typically, 0.1- $\mu$ F capacitors are used.

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