

TPIC74100-Q1 Buck/Boost Switch-Mode Regulator

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ABSTRACT

This document explains the features and benefits of the TPIC74100 buck/boost switch-mode regulator, which has been designed for automotive power-management applications.

It is meant as a guideline to achieve a good configuration of the device.

The configuration of the device is dependent on the individual application. Important topics required for this evaluation are covered. The different operating modes of the device are explained. Help for the selection criteria of external components is given and example calculations are included. In addition, there are rules and hints for an optimized layout and some information about evaluating the thermal condition within the application.

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1 Introduction

The TPIC74100 is a buck/boost switch-mode regulator with integrated switches. It regulates the output voltage to a fixed value of 5 V. Depending on the input voltage, it steps up (boost mode) or steps down (buck mode) the input voltage. The feedback loop for the regulation circuit is internal. The regulator is using voltage-mode control. As the switches are already integrated, the external components are reduced to capacitors, resistors, and an inductor.

In addition to this primary functionality, the TPIC74100 provides circuits to supervise the input and the output voltage. It provides protection against overcurrent, short-circuit, and overtemperature conditions.

As an additional feature, the generated output voltage can be switched to a separate device pin. If the device is enabled, voltage is supplied to a primary/permanent output voltage pin and a secondary/nonpermanent output voltage pin. The secondary output voltage has a supervision functionality implemented to prevent the primary voltage from dipping.

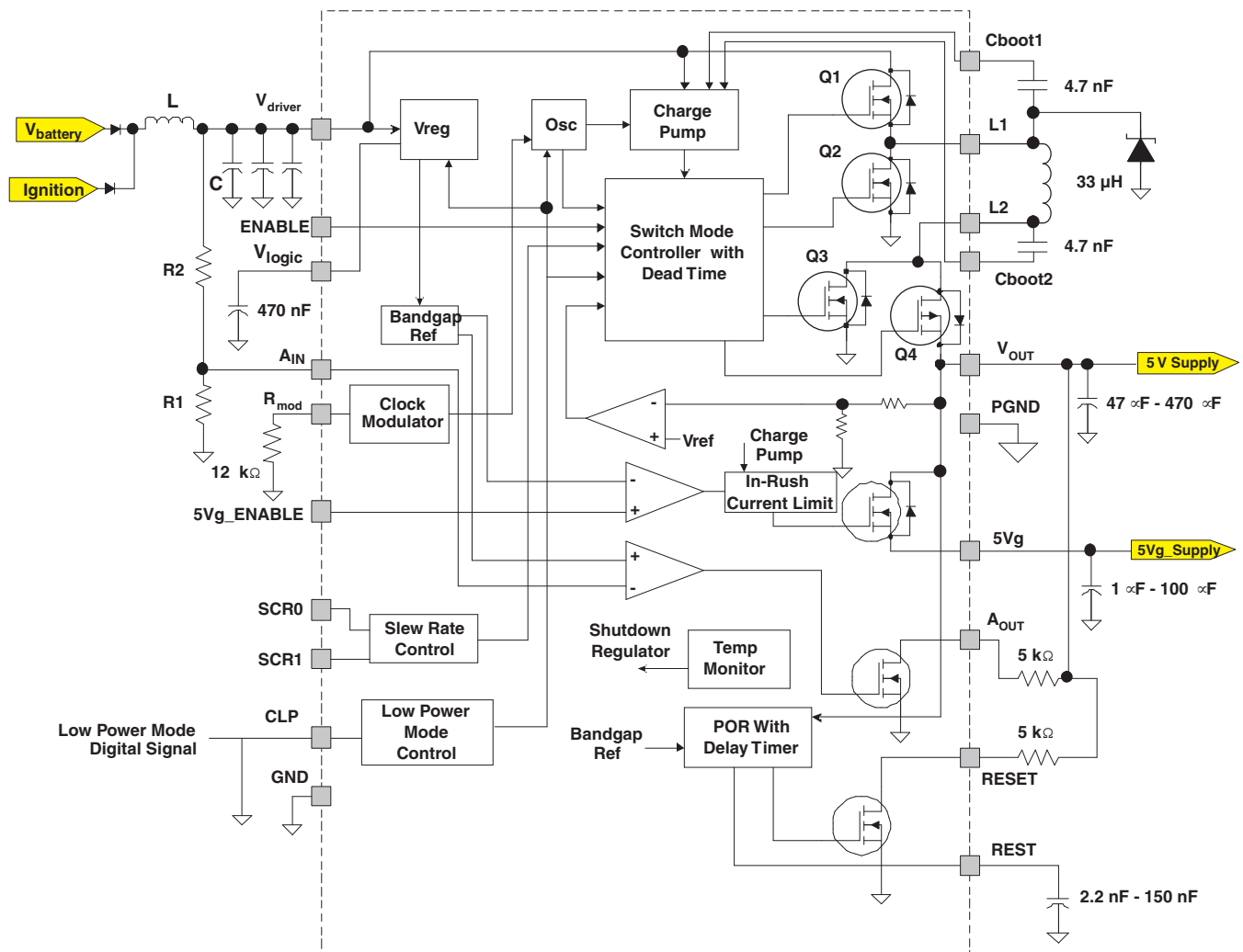


Figure 1. Schematic With Typical External Components

2 Description

2.1 Features and Benefits

- **Switch-Mode Regulator With Integrated Switches**
 - Less board space
 - Lower cost
 - Higher EMI performance
 - Improved protection off the integrated switches
- **Buck/Boost Mode**
 - Wide input voltage range (ideal for automotive applications where the power supply must stay stable during the start of the engine-cranking pulse)
- **Low-Power Operation Mode**
 - Conserves battery power during conditions with low load current
- **Second Output Voltage With Enable Function**
 - The primary/permanent output voltage can be switched to a second pin, which acts as a second output voltage with enable function.
 - Soft-start for second output voltage implemented
 - Conserve battery power by disabling second output voltage under certain conditions
 - V_{OUT} voltage is protected from failures of the 5Vg line
- **Device Enable Function**
 - Conserve battery power during system shutdown by disabling the device
- **Enhanced EMI Performance**
 - Programmable frequency modulation – spread spectrum
 - Programmable slew rate
- **Supervision Functionality**
 - Supervision of input voltage, programmable under-voltage detection threshold, and open-drain output for generation of alarm signal
 - Supervision of output voltage, programmable delay timer, and open-drain output for generation of reset signal, e.g., for supervisor microcontroller
- **Current Limit**
 - Protection in case of overcurrent and short-circuit conditions
- **Thermal Shutdown**
 - Protection in case of overtemperature conditions

2.2 Operating Modes

2.2.1 Start-Up

It is important to consider the separate specification for the input voltage V_{driver} during start-up of the device (setting ENABLE pin from low to high). The device is not able to start up with the lowest specified input voltage.

During start-up, the device internal power supply V_{logic} is fed by the input voltage at V_{driver} . After start-up, it is fed by the output voltage and is no longer dependent of the input voltage (see the TPIC74100 data sheet in the *Electrical Characteristics* section, parameter V_{driver} Start-up condition voltage).

2.2.2 Continuous – Discontinuous Conduction Mode

Whether the device operates in buck or in boost mode, there is a differentiation between continuous and discontinuous conduction mode. For buck and boost mode operation in continuous conduction mode, the function of the inductor current (I_L) is a triangle. In buck mode, the average current of I_L equals the output load current I_{OUT} ; in boost mode, it equals the input current I_{driver} .

As long as the minimum current in the inductor, $I_L(\text{min})$, is greater than 0 mA, the regulator operates in continuous conduction mode. There are two unique stages that the power stage assumes during continuous conduction mode: on stage and off stage. The current flow in the inductor is continuous.

At all other times, the regulator operates in discontinuous mode. There are three unique stages that the power stage assumes during discontinuous conduction mode: on stage, off stage, and idle stage. The current flow in the inductor is discontinuous.

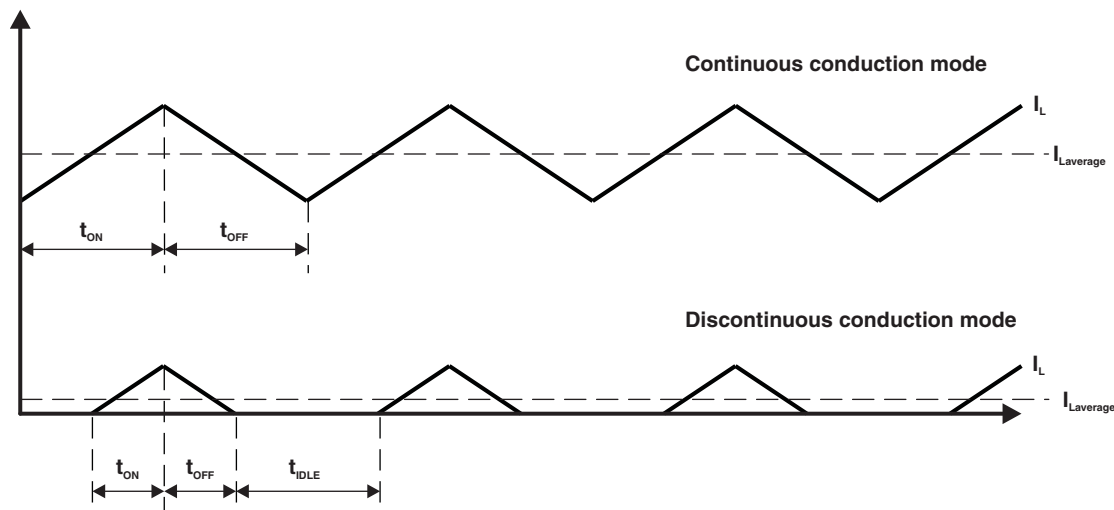


Figure 2. Continuous and Discontinuous Conduction Modes

The frequency response of the regulator changes between the two modes. Continuous conduction mode is considered the main operation condition. The transition threshold of the average inductor current ($I_{L(\text{average})}$) between the two modes is determined by the peak-to-peak value of the ripple current in the inductor (ΔI_L). Within a certain range, it can be modified by selection of the inductance (see [Section 3.1](#)).

2.2.3 Buck Mode

In buck mode, the device is stepping/converting down the input voltage, so $V_{\text{driver}} > V_{\text{OUT}}$.

Figure 3 shows the equivalent schematic for the on and off phases while operating in continuous conduction buck mode. The on and off phases relate to the status of the high-side switch, Q1, which is connected to the input voltage $V_{\text{IN}} = V_{\text{driver}}$.

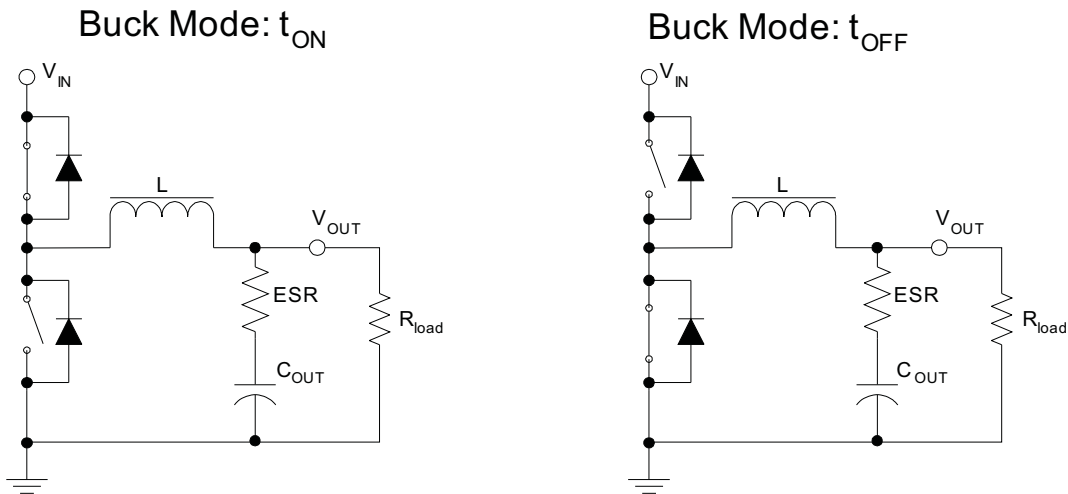


Figure 3. Equivalent Schematics – Buck Mode

During the on phase, the current in the inductor is increasing; during the off phase, it is decreasing. The average current in the Inductor is equal to the output load current (I_{OUT}). As long as the inductor current is higher than the output load current, the output capacitor (C_{OUT}) is charging. If it is lower than the output load current, C_{OUT} is discharging.

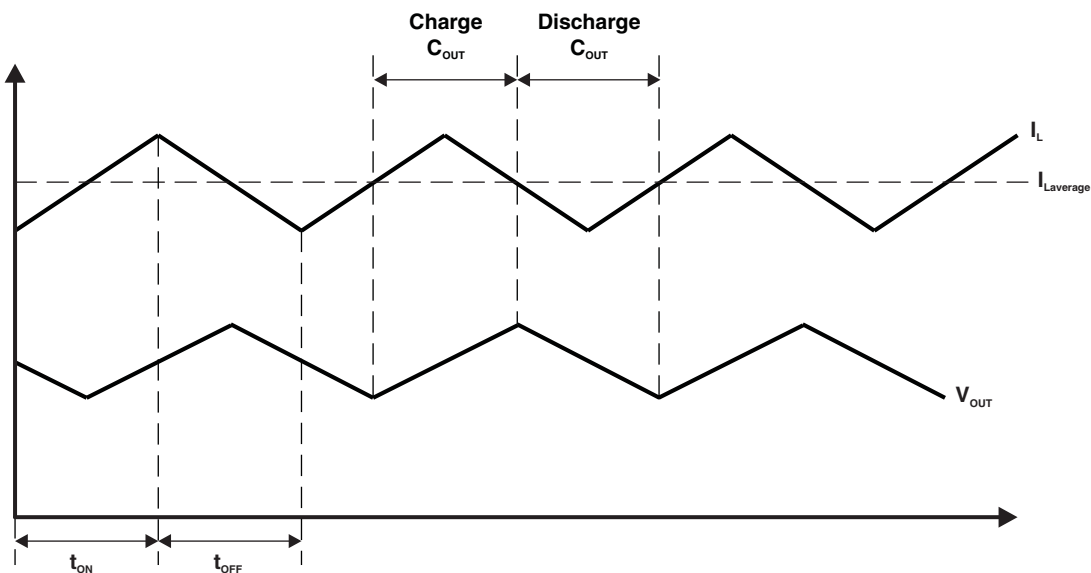


Figure 4. Ideal Buck Converter, Continuous Conduction, I_L and V_{OUT} vs Time

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{t_{\text{ON}}}{T_P} = D$$

$$T_P = t_{\text{ON}} + t_{\text{OFF}}$$

$$I_{\text{Laverage}} = I_{\text{OUT}}$$

2.2.4 Boost Mode

In boost mode, the device is stepping/converting up the input voltage, so $V_{\text{driver}} < V_{\text{OUT}}$.

Figure 5 shows the equivalent schematic for the on and off phases while operating in continuous conduction boost mode. The on and off phases relate to the status of the low-side switch, Q3, which is connected to the ground pin.

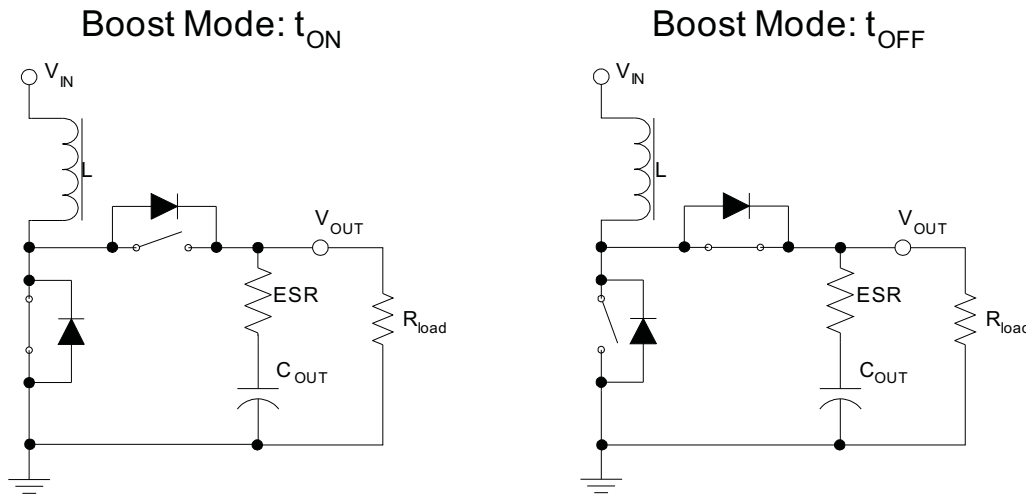


Figure 5. Equivalent Schematics – Boost Mode

During the on phase, the current in the inductor is increasing; during the off phase, it is decreasing. The average current in the inductor is equal to the input current ($I_{\text{IN}} = I_{\text{driver}}$). During the on phase, the output capacitor (C_{OUT}) is discharging; during the off phase, C_{OUT} is charging.

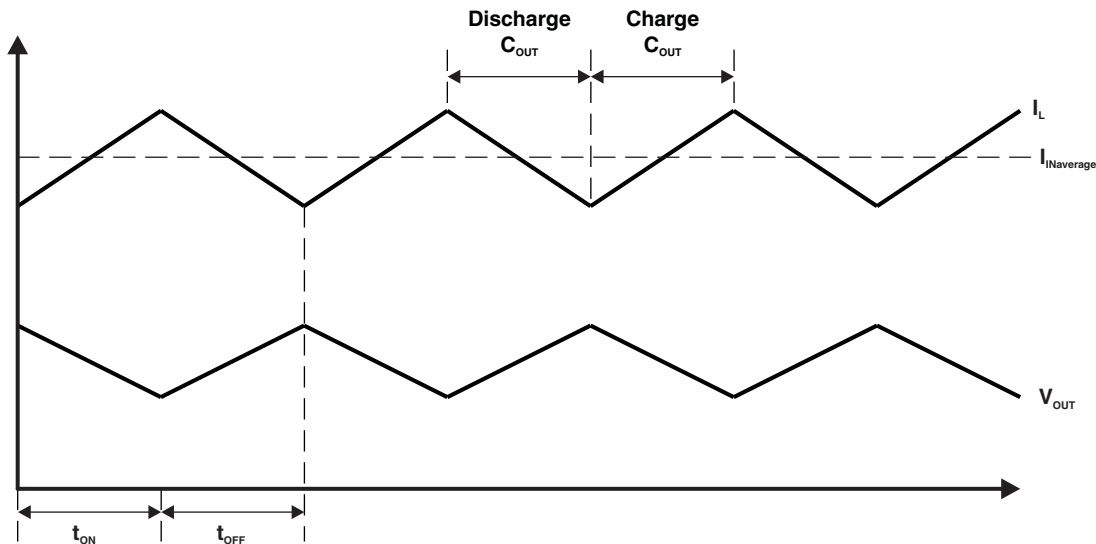


Figure 6. Ideal Boost Converter, Continuous Conduction, I_L and V_{OUT} vs Time

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{T_P}{T_P - t_{\text{ON}}} = \frac{1}{1 - D} \quad T_P = t_{\text{ON}} + t_{\text{OFF}} \quad I_{\text{Laverage}} = I_{\text{IN}}$$

2.2.5 Transition Buck / Boost Mode

The transition between buck and boost mode is done automatically and has almost no impact on the output voltage (V_{OUT}).

These points must be considered:

- Output voltage tolerance increases to worst case value of $\pm 3\%$ instead of $\pm 2\%$ during the transition between the two modes.
- Output current capability decreases with decreasing input voltage (V_{driver}) in boost mode.

The increased output voltage tolerance is specified for the transition phase from buck to boost and from boost to buck.

- Transition from boost to buck occurs during increasing V_{driver} voltage at the threshold of 5.8 V (typical).
- Transition from buck to boost occurs during decreasing V_{driver} voltage, within the so-called crossover window, from 5.8 V (typical) down to 5 V (typical).

The exact threshold for the transition between the modes is dependent on the input voltage V_{driver} , the load current I_{OUT} , and the external components.

The increased tolerance during the transition is primarily required for conditions with low load currents. Ripple of the output voltage in general improves for higher load current conditions.

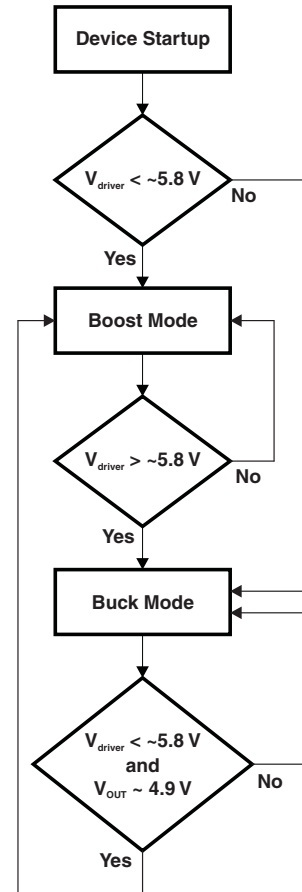


Figure 7. Mode Transition

2.2.6 Low-Power Mode

To increase the efficiency at low output load currents, the device can be switched into a low-power operation mode. Output load currents are considered low if the device operates in discontinuous conduction mode.

During normal operation with no low-power mode activated, the device works in pulse-width modulation (PWM) mode. The switching frequency remains constant, and regulation is accomplished by variation of the duty cycle. In low-power mode, the device is working in pulse-frequency modulation (PFM) mode. Regulation is accomplished by variation of the switching frequency.

There is no reduced load current capability for the output load in PFM mode. Efficiency is lower and output voltage ripple is larger than in PWM mode for higher load currents. Low-power mode functionality is implemented for buck-mode operation. In boost-mode conditions, the device automatically operates in PWM mode. When low-power mode is enabled, the transition between buck and boost is also a transition between PWM mode and PFM mode.

2.2.7 Secondary Output Voltage

The secondary output voltage (5Vg) can be switched on and off while the device is enabled. Internally, the primary output voltage V_{OUT} is shared to the 5Vg pin.

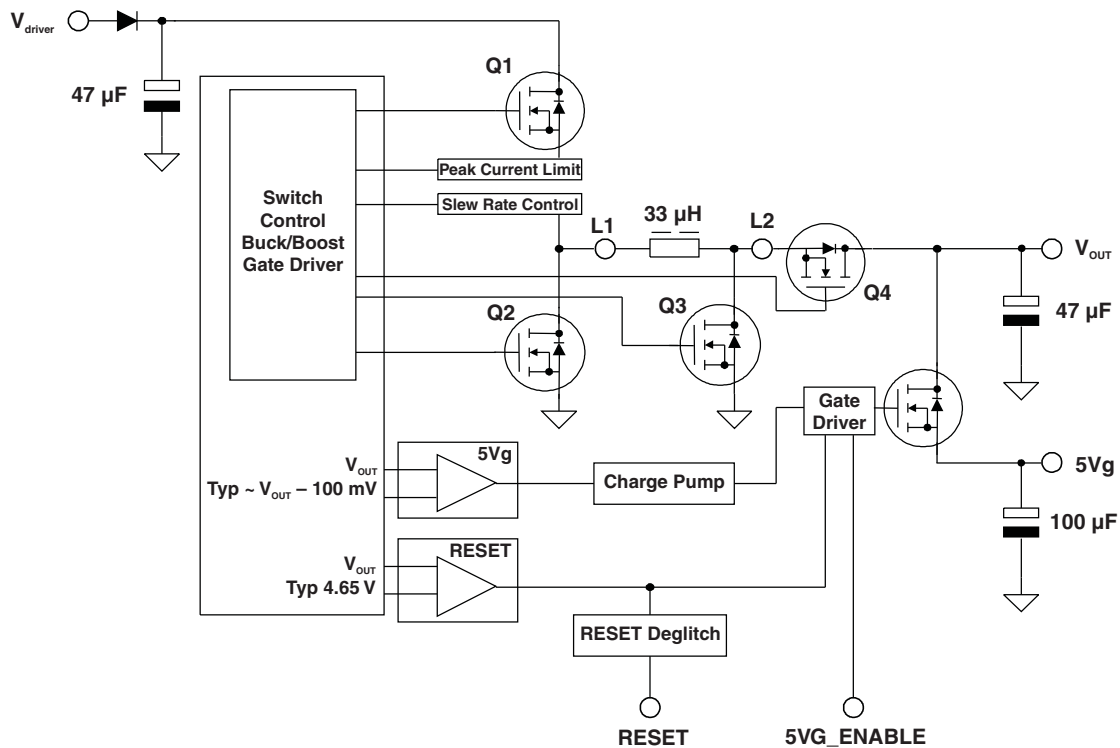


Figure 8. Primary and Secondary Output Voltage Terminals

An internal charge pump drives the internal FET that shares the primary output voltage on the V_{OUT} pin to the 5Vg pin. Protection is implemented to prevent the primary output voltage from dropping below its specified value while the secondary output voltage is enabled. An explanation of the block diagram in Figure 8 is given by the following example:

- The device is enabled, and output voltage V_{OUT} is up and stable.
- 5Vg is enabled (pin 5Vg_ENABLE is set high) with load resistance connected to 5Vg.
- If output voltage V_{OUT} drops below typical ($V_{OUT} - 100$ mV), the charge pump of the 5Vg FET is switched off, and the FET remains on for a while as the gate voltage slowly drops.
- If V_{OUT} drops below the RESET threshold of 4.65 V (typical), the FET of the secondary output voltage 5Vg is switched off (the gate is drawn to ground level).
- A deglitch time ensures that a device reset does not occur if V_{OUT} drops to the reset level during the 5Vg turn-on phase.
- If V_{OUT} is rising above typical ($V_{OUT} - 100$ mV), the charge pump of the 5Vg FET is switched on and drives the gate of the 5Vg FET on.

In summary, the 5Vg output current is limited by a PFM. Modulation is realized by two-point control loop monitoring the primary output voltage V_{OUT} .

2.2.8 Other Operating Conditions/Modes

Overvoltage Protection Circuit for V_{OUT}

The overvoltage protection circuit for V_{OUT} prevents the output voltage from rising above the specified boundaries. It activates during operation in discontinuous conduction mode at very low load currents.

In discontinuous mode, the minimum on time t_{ON} determines the minimum amount of energy that is pumped into the inductance. Once in the inductance, the energy is transferred to the output terminal, V_{OUT} . In other words, every triangle of the inductor current in discontinuous conduction mode (see [Figure 2](#)) transfers a minimum amount of energy to the output. If the output load current consumes less than this amount, the output voltage would rise without the protection circuit.

The overvoltage protection circuit monitors the output voltage and skips the ON phase (that is, it does not switch on the high-side FET Q1) if V_{OUT} is higher than 5.08 V (typical). By skipping the ON phase, a PFM mode is realized within the operation in PWM mode.

Synchronous/Nonsynchronous Mode

To prevent the current in the inductance from reverting during the OFF phase at low load currents (discontinuous conduction mode) in buck mode, the low-side FET Q2 is not switched on. Current flow during OFF phase is through the free-wheeling diode of the low-side FET Q2 and the external Schottky diode. A reverting current in the inductance would add losses and decrease efficiency. When this occurs, the regulator is working in nonsynchronous mode.

If the peak current measured in the high-side FET Q1 exceeds 450 mA (typical), the low-side FET Q2 is switched ON during the OFF phase (see [Figure 3](#)). Voltage drop across the diode is now reduced to the voltage drop across the ON resistance of the low-side FET Q2 ($R_{DS\ ON}$). In this case, the regulator is working in synchronous mode with an increased efficiency.

Slew Rate Control

The slew rate settings control the input current rate of the high-side FET Q1 in buck mode. Buck mode is the most critical mode, because of the high ripple currents at the input terminal V_{driver} . The slew rate control gives the option to improve EMI performance by selecting slower slew rate settings or to improve efficiency by selecting faster slew rate settings (see typical oscilloscope plots of different slew rate setting in the data sheet).

Peak Current Limit

In buck mode, the peak current limit circuit monitors the current flow through the high-side FET Q1, which is connected to the V_{driver} terminal. If a current higher than the peak current limit threshold of 2 A (typical) is detected, FET Q1 is switched off. There is a turn-off delay for the FET of 100 ns (typical). FET Q1 can be turned on again in the next cycle of the switching period. In low-power mode, the peak current limit is reduced to 1 A (typical).

In boost mode, the gate of the high-side FET Q1 is pulled down if the peak current limit threshold of 2 A (typical) is detected. The average current limit is dependent of the external configuration (e.g., capacitor size at V_{OUT} , $R_{DS\ ON}$ of the inductor, etc.). It is slightly higher in boost mode than in buck mode.

The slope of the inductor current determines the actual peak current. The slope of the inductor current can become very large if the inductor is operated in saturation. If the peak current limit is meant as short-circuit protection for the application, an inductor with appropriate saturation current (I_{SAT}) must be selected. Otherwise, the inductor could be destroyed under a short-circuit condition (see [Section 3.1](#)).

2.3 EMI performance

2.3.1 Modulation of the Switching Frequency

Modulation of the switching frequency can improve the EMI performance by spreading the emitted spectrum of the switch-mode regulator (frequency spread-spectrum method).

The switching frequency of the regulator can be modulated with the clock modulator frequency. This modulation frequency can be selected with an external resistor from the R_{mod} pin to the GND pin.

By modulating the switching frequency, its spectral line sweeps back and forth accordingly in the frequency spectrum. The nonmodulated spectral line of the switching frequency is transformed into a spectral band by modulation, causing emitted peak values to decrease. The speed of the sweep is adjusted with the modulator frequency, while the span of the sweep remains constant.

It is not possible to switch on the modulation if the device is already enabled. The check for an external resistor connected to R_{mod} is only performed once when the device is enabled.

2.3.2 Selection of the Slew Rate

The slew rate of the regulator can be programmed in four stages. Depending on application requirements, device operation can be optimized for EMI performance or for high efficiency. Faster slew rates result in higher efficiency, and slower slew rates result in better EMI performance.

2.3.3 Adjustment of the Ripple Current

Another way to improve the EMI performance is to reduce the ripple current in the inductor. The ripple current can be adjusted by the selection of external components.

2.3.4 External Schottky Diode

The external Schottky diode optimizes the regulator for EMI performance and efficiency. It is required for stable operation and placed between pins L1 and PGND.

In buck mode, the voltage drop at the low-side FET Q2 during the off period is determined by its on resistance ($r_{\text{DS(on)}}$). The voltage drop is limited by the forward voltage of the internal diode of the FET Q2 (free-wheeling diode). There is a dead time when both switches are OFF during the transition from ON to OFF. During the dead time, the voltage drop is defined by the forward voltage of the internal diode or the external Schottky diode. With the lower forward voltage of a Schottky diode, the voltage drop is reduced.

For high-power applications, a lower voltage drop means increased efficiency. The fast response time of the Schottky diode also has a positive effect on EMI performance. In addition, part of the overall thermal dissipation loss is transferred from the TPIC74100 to the external Schottky diode.

3 Selection of External Components

3.1 Inductor

Inductance

- Recommended inductance range: 22 μH to 100 μH
- Define the tolerable ripple current (e.g., $dI_L = 0.2 \times I_{\text{OUT}}$) and calculate the inductance.
- Another option is to calculate the ripple current at a given inductance.
- The size of the ripple current (dI_L) determines the threshold for the regulator to operate in continuous or discontinuous conduction mode, which might impact EMI behavior (see [Section 2.2.2](#)).
- A larger inductance value results in lower current ripple, better EMI performance, but it also results in slower response to fast load transients, due to the larger amount of stored energy in the inductor.

$$\text{Buck Mode: } L = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{f_{\text{SW}} \times dI_L \times V_{\text{IN}}} \quad dI_L = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{f_{\text{SW}} \times L \times V_{\text{IN}}}$$

$$\text{Boost Mode: } L = \frac{(V_{\text{OUT}} - V_{\text{IN}}) \times V_{\text{IN}}}{f_{\text{SW}} \times dI_L \times V_{\text{OUT}}} \quad dI_L = \frac{(V_{\text{OUT}} - V_{\text{IN}}) \times V_{\text{IN}}}{f_{\text{SW}} \times L \times V_{\text{OUT}}}$$

DC Resistance (DCR)

- Low DCR is required to reduce losses and achieve high efficiency.

Saturation Current (I_{SAT})

- For a short-circuit proof design, the saturation current (I_{SAT}) of the inductor should be equal to or greater than the internal peak current limit.

Root Mean Square (RMS) Current (I_{RMS})

- The RMS current in the inductor causes the temperature of the inductor to rise a specific amount above ambient temperature.

$$\text{Buck Mode: } I_{L_average} = I_{\text{OUT}} \quad I_{\text{RMS}_L} = I_{\text{RMS}_\text{OUT}}$$

$$I_{\text{RMS}_\text{OUT}} = \frac{0.29 \times V_{\text{OUT}} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right)}{L \times f_{\text{SW}}} = 0.29 \times dI_L$$

$$\text{Boost Mode: } I_{L_average} = I_{\text{IN}} \quad I_{\text{RMS}_L} = I_{\text{RMS}_\text{driver}}$$

$$I_{\text{RMS}_\text{driver}} = \frac{1}{3} \times dI_L = \frac{(V_{\text{OUT}} - V_{\text{IN}}) \times V_{\text{IN}}}{3 \times L \times f_{\text{SW}} \times V_{\text{OUT}}}$$

3.2 Input Capacitor

An external filter capacitor is required at the input terminal V_{driver} . The capacitor needs to support peak currents to reduce voltage ripple at V_{driver} and minimize noise. For the input capacitor, buck mode causes much more stress than boost mode. The following key parameters need to be considered for the selection of C_{IN} .

Capacitance

- For most applications, the requirements for high RMS current rating and low ESR determine the minimum available capacitance.
- Recommended capacitance is 22 μF to 470 μF .

Equivalent Series Resistance (ESR)

- Low ESR required to reduce voltage ripple at the input V_{driver} .
- A low-ESR aluminum or tantalum-type capacitor with $\text{ESR} < 200 \text{ m}\Omega$ is recommended.

Voltage Rating

- Approximately 1.5 times the maximum applied voltage at V_{driver} for an aluminum-type capacitor
- Approximately two times the maximum applied voltage at V_{driver} for a tantalum-type capacitor

Equivalent Series Inductance (ESL)

- Choose low ESL capacitors to avoid potential problems with ringing in the lower MHz range.

RMS Current Rating

- RMS value of the input ripple current ($I_{\text{RMS_driver}}$) heats up input capacitor C_{IN} due to its internal ESR. This rating is especially critical in buck mode.

$$\text{Buck Mode: } I_{\text{RMS_driver}} = I_{\text{OUT}} \times \sqrt{D - D^2} = I_{\text{OUT}} \times \sqrt{\frac{V_{\text{OUT}}(V_{\text{IN}} - V_{\text{OUT}})}{(V_{\text{IN}})^2}}$$

$$\text{Worst Case: } D = 50\%. V_{\text{IN}} = 2 \times V_{\text{OUT}} : I_{\text{RMS_driver}} = \frac{I_{\text{OUT}}}{2}$$

$$\text{Boost Mode: } I_{\text{RMS_driver}} = \frac{1}{3} \times dI_L = \frac{(V_{\text{OUT}} - V_{\text{IN}}) \times V_{\text{IN}}}{3 \times L \times f_{\text{SW}} \times V_{\text{OUT}}}$$

$$\text{Worst Case: } D = 50\%. V_{\text{OUT}} = 2 \times V_{\text{IN}} : I_{\text{RMS_driver}} = \frac{V_{\text{OUT}}}{12 \times L \times f_{\text{SW}}}$$

In parallel to the filter capacitor at the input terminal on V_{driver} , a fast ceramic-type capacitor is recommended for EMI performance reasons.

3.3 Output Capacitors

An external filter capacitor is required at the output pins V_{OUT} and $5V_{\text{G}}$. The capacitors must support the peak currents to reduce voltage ripple at V_{OUT} and minimize noise. For the output capacitor, boost mode causes much more stress than buck mode. Filtering of the output voltage is done by C_{OUT} at the V_{OUT} pin. The on resistance of the $5V_{\text{G}}$ FET ($r_{\text{DS(on)}}$) limits the filter capability of $C_{5V_{\text{G}}}$. The following key parameters must be considered for the selection of C_{OUT} and $C_{5V_{\text{G}}}$.

Capacitance

- Capacitance influences the output voltage ripple, but the ESR of the capacitor has more influence (see the following formulas).
- Recommended capacitance C_{OUT} is 22 μF to 470 μF .
- Recommended capacitance $C_{5V_{\text{G}}}$ is 1 μF to 100 μF .
- Total capacitance ($C_{\text{OUT}} + C_{5V_{\text{G}}}$) must be equal or less than 470 μF .

Equivalent Series Resistance (ESR)

- Low ESR is required to reduce voltage ripple at V_{OUT} .
- A low ESR aluminum or tantalum type capacitor is recommended.
- Ripple of the output voltage is mainly determined by the ESR value.

$$\text{Buck Mode: } dV_{\text{OUT}} = dV_{\text{ESR_COUNT}} + dV_{\text{COUT}} = dI_L \times \left(\text{ESR}_{\text{COUT}} + \frac{1}{8 \times C_{\text{OUT}} \times f_{\text{SW}}} \right)$$

$$\text{Boost Mode: } dV_{\text{OUT}} \approx dV_{\text{ESR_COUNT}} + dV_{\text{COUT}}$$

$$dV_{\text{COUT}} = \frac{I_{\text{OUT}} \times D}{C_{\text{OUT}} \times f_{\text{SW}}} = \frac{I_{\text{OUT}} \times \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}} \right)}{C_{\text{OUT}} \times f_{\text{SW}}}$$

$$dV_{\text{ESR_COUT_MAX}} = \left(\frac{I_{\text{OUT}}}{1 - D} + \frac{dI_L}{2} \right) \times \text{ESR}_{\text{COUT}} = \left(\frac{I_{\text{OUT}} \times V_{\text{OUT}}}{V_{\text{IN}}} + \frac{dI_L}{2} \right) \times \text{ESR}_{\text{COUT}}$$

Voltage Rating

- Approximately 1.5 times the output voltage at V_{OUT} for an aluminum type capacitor
- Approximately two times the output voltage at V_{OUT} for a tantalum type capacitor

Equivalent Series Inductance (ESL)

- Choose low ESL capacitors to avoid potential problems with ringing in the lower MHz range.

RMS Current Rating

- RMS value of the output ripple current I_{RMS_OUT} heats up the output capacitor (C_{OUT}) due to its internal ESR. This rating is especially critical in boost mode.

$$\text{Buck Mode: } I_{RMS_OUT} = \frac{0.29 \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{SW}} = 0.29 \times dI_L$$

$$\text{Boost Mode: } I_{RMS_OUT} = I_{OUT} \times \sqrt{\frac{V_{OUT} - V_{IN}}{V_{IN}}} = I_{OUT} \times \sqrt{\frac{D}{1 - D}}$$

3.4 Stability Considerations

The TPIC74100 is a voltage-mode controlled regulator with fully integrated feedback loop, error amplifier, and compensation. No further external components are required.

The main external influence to the frequency and phase response of the TPIC74100 is determined by the output filter. Inductor and output capacitor should be selected within the following range:

| | | | | |
|------------------|--------------------------|-----------------|------------------|-------------------------|
| Inductor | L (inductance): | Min: 22 μ H | Max: 100 μ H | |
| Capacitor | C_{OUT} (capacitance): | Min: 22 μ F | Max: 470 μ F | ($C_{OUT} + C_{5Vg}$) |

Series resistance of the output capacitor:

| | | | |
|------------------------|---|---------------------|---------------------|
| ESR_C | 22 μ H \geq L \leq 68 μ H | | |
| | 22 μ F \geq C_{OUT} \leq 470 μ F: | Min: 50 m Ω | Max: 500 m Ω |
| | 68 μ H $>$ L \leq 100 μ H | | |
| | 22 μ F \geq C_{OUT} $<$ 33 μ F: | Min: 100 m Ω | Max: 500 m Ω |
| | 33 μ F \geq C_{OUT} \leq 470 μ F: | Min: 50 m Ω | Max: 500 m Ω |

The following values are recommended by TI for best performance:

- L = 33 μ H
- C = 47 μ F
- ESR_C = 50 m Ω to 100 m Ω

3.5 External Schottky Diode

DC Blocking Voltage/Reverse Voltage (V_R)

- $V_R \geq$ maximum input voltage at V_{driver} terminal
- Recommendation: $V_R \geq 40$ V

Feed Forward Voltage

- Maximum voltage drop at 125°C < 0.4 V

Average Rectified Forward Current (I_O)

- $I_O \geq$ maximum specified load current I_{OUT}
- For a short-circuit proof design, I_O must be greater than the internal peak current limit.

See [Section 2.3.4](#).

3.6 Modulator Frequency

Selection is done via external resistor at pin R_{mod} to GND. The resistor is checked only once when the device is enabled. If no resistor is detected, the functionality is disabled. This means the modulation cannot be enabled while the device is operating.

Table 1. Modulator Frequency

| R_{mod} | $f_{(\text{mod})}$ | Minimum Switching Frequency $f_{(\text{SW_MIN})}$ | Maximum Modulation Frequency $f_{(\text{SW_MAX})}$ |
|------------------|--------------------|---|---|
| 0 k Ω | 0 kHz | $f_{(\text{SW_MIN})} = f_{(\text{SW})}$ | $f_{(\text{SW_MAX})} = f_{(\text{SW})}$ |
| 12 k Ω | 28 kHz (typ) | $f_{(\text{SW_MIN})} = f_{(\text{SW})} - \text{modulation span}$ | $f_{(\text{SW_MAX})} = f_{(\text{SW})} + \text{modulation span}$ |
| 24 k Ω | 56 kHz (typ) | $f_{(\text{SW_MIN})} = f_{(\text{SW})} - \text{modulation span}$ | $f_{(\text{SW_MAX})} = f_{(\text{SW})} + \text{modulation span}$ |

The external resistor determines the period $T_{(\text{mod})}$ it takes for the switching frequency $f_{(\text{SW})}$ to sweep from the modulation minimum frequency to the modulation maximum frequency. Modulation minimum and maximum frequency and resulting modulation span (maximum modulation frequency – minimum modulation frequency) are not dependent on the modulation frequency.

Modulation of the switching frequency increases EMI performance (see [Section 2.3.1](#)).

3.7 Slew Rate Selection

The pins SCR0 and SCR1 do not support full input voltage range of V_{driver} (see the maximum ratings specified in the data sheet). Usually they are connected to V_{logic} or V_{OUT} .

Table 2. Slew Rate Selection

| SCR1 | SCR0 | SRQ1 | EMI Performance | Efficiency |
|------|------|-------------------|-----------------|------------|
| GND | GND | Slowest slew rate | Best case | Worst case |
| GND | HIGH | Slow slew rate | | |
| HIGH | GND | Fast slew rate | | |
| HIGH | HIGH | Fastest slew rate | Worst case | Best case |

3.8 Input Voltage Monitoring Threshold

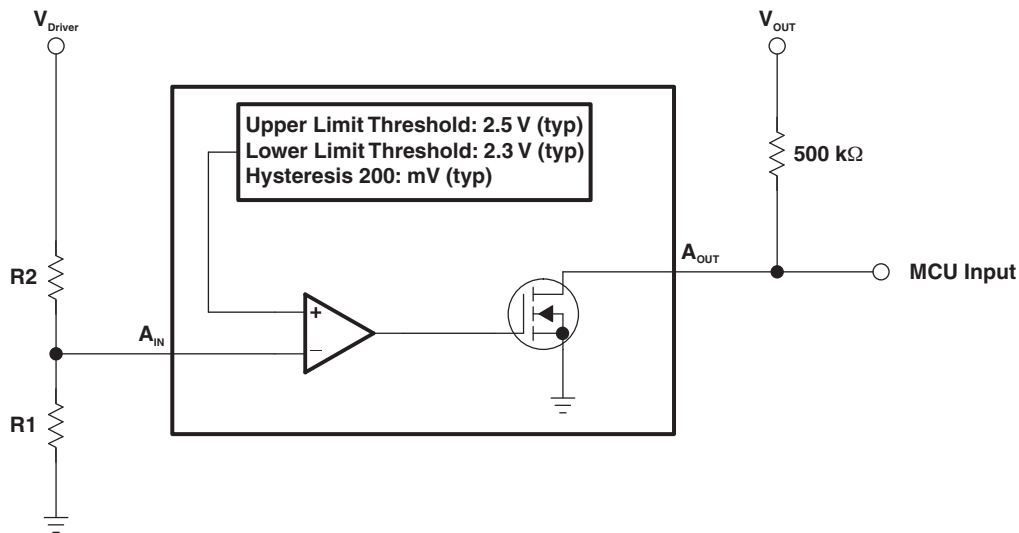


Figure 9. SVS Circuit

Total resistance (R1 + R2) determines additional leakage current.

$$I_{\text{leakage}} = \frac{V_{\text{driver}}}{(R1 + R2)} \quad R1 = (R1 + R2) \times \frac{A_{\text{IN}}}{V_{\text{driver}}}$$

3.9 Reset Timer Delay

Program the desired delay time to assert RESET low after output voltage V_{OUT} has exceeded 4.65 V (typical) by an external capacitor at REST. Delay may be programmed in the range of 2.2 ms to 150 ms.

$$\text{RESET delay} = (C_{\text{RESET}}/1 \text{ nF}) \times 1 \text{ ms} \quad \rightarrow 1 \text{ nF is equivalent to a delay of 1 ms}$$

3.10 Pullup Resistors

Pullup resistors at A_{OUT} and RESET are usually connected to V_{OUT} or V_{logic} . A_{OUT} and RESET do not support full input voltage range of V_{driver} (see maximum ratings specified in the data sheet).

3.11 Miscellaneous

V_{logic}

- During startup, V_{logic} is $\sim V_{\text{driver}}$ but not higher than $\sim 6 \text{ V}$ (start up condition $V_{\text{driver}} > 5 \text{ V}$).
- If the device is operating, V_{logic} is $\sim V_{\text{OUT}}$ (supplied by V_{OUT}).

3.12 Example Calculations

Application Conditions

- V_{driver} : 1.5 V to 40 V \rightarrow Device operating in buck and boost mode
- $V_{\text{dr_typ}}$: 12 V \rightarrow Typical V_{driver} voltage for application
- I_{OUT} : 0 A to 1 A \rightarrow Output load over full specification range

Inductor L

- Maximum ripple current: $dl = 0.2 \times I_{OUT} = 0.2 \times 1 \text{ A} = 200 \text{ mA}$
- L for typical input driver voltage $V_{driver} = V_{dr_typ} = 12 \text{ V}$
 Buck mode:
$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f_{SW} \times dl \times V_{IN}} = \frac{(12 \text{ V} - 5 \text{ V}) \times 5 \text{ V}}{380 \text{ kHz} \times 200 \text{ mA} \times 12 \text{ V}} = 38 \mu\text{H}$$
 → **Selection: L = 33 μH**

- Check worst-case ripple current over operating conditions

Buck mode, worst case: $V_{IN} = V_{driver_max} = 40 \text{ V}$

$$dl_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f_{SW} \times L \times V_{IN}} = \frac{(40 \text{ V} - 5 \text{ V}) \times 5 \text{ V}}{380 \text{ kHz} \times 33 \mu\text{H} \times 40 \text{ V}} = 350 \text{ mA}$$

Boost mode, worst case: $V_{IN} = V_{OUT}/2$

$$dl_L = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{f_{SW} \times L \times V_{OUT}} = \frac{V_{OUT}}{4 \times f_{SW} \times L} = \frac{5 \text{ V}}{4 \times 380 \text{ kHz} \times 33 \mu\text{H}} = 100 \text{ mA}$$

→ **Worst case: buck mode, $dl_L \approx 350 \text{ mA}$**

- RMS current I_{RMS} :

Buck mode, worst case: $I_{RMS_OUT} = 0.29 \times dl_L = 0.29 \times 350 \text{ mA} = 102 \text{ mA}$

Boost mode, worst case: $I_{RMS_driver} = \frac{1}{3} \times dl_L = \frac{1}{3} \times 100 \text{ mA} = 33 \text{ mA}$

→ **Worst case: buck mode, $I_{RMS} \neq 100 \text{ mA}$**

- Saturation current I_{SAT} :

Buck mode, worst case: $I_{L_peak} = I_L + \frac{dl_L}{2} = I_{OUT} + \frac{dl_L}{2} = 1 \text{ A} + \frac{350 \text{ mA}}{2} = 1.18 \text{ A}$

Boost mode, worst case: $V_{IN} = \frac{V_{OUT}}{2} = 2.5 \text{ V}$, $I_{IN} = 2 \times I_{OUT}$, $I_{OUT_max} = \sim 500 \text{ mA}$
 (includes margin, specified is 200 mA for $V_{driver} = 2 \text{ V}$)

$$I_{L_peak} = I_L + \frac{dl_L}{2} = I_{IN} + \frac{dl_L}{2} = 2 \times 0.5 \text{ A} + \frac{100 \text{ mA}}{2} = 1.05 \text{ A}$$

→ **$I_{SAT} \neq 1.2 \text{ A}$, considering short-circuit protection some added margin**

Input Capacitor C_{IN}

- RMS current rating I_{RMS}

Buck mode, worst case: $V_{IN} = 2 \times V_{OUT}$, $I_{RMS_driver} = I_{OUT}/2 = 1 \text{ A}/2 = 0.5 \text{ A}$

Boost mode, worst case: $I_{RMS_driver} = \frac{1}{3} \times dl_L = \frac{1}{3} \times 100 \text{ mA} = 33 \text{ mA}$

→ **Worst case: buck mode, $I_{RMS} > 0.5 \text{ A}$**

Output Capacitor C_{OUT}

- RMS current rating I_{RMS}

Buck mode, worst case:

$$I_{RMS_OUT} = 0.29 \times dI_L = 0.29 \times 350 \text{ mA} = 102 \text{ mA}$$

Boost mode, worst case:

$$V_{IN} = V_{\text{driver_min}} = 1.5 \text{ V}$$

$$I_{OUT_max} \neq 350 \text{ mA (specified 200 mA, additional margin)}$$

$$I_{RMS_out} = I_{OUT} \times \sqrt{\frac{V_{OUT} - V_{IN}}{V_{IN}}} = 350 \text{ mA} \times \sqrt{\frac{5 \text{ V} - 1.5 \text{ V}}{1.5 \text{ V}}} = 535 \text{ mA}$$

→ **Worst case, boost mode, I_{RMS} > 0.5 A**

- Output voltage ripple: → **defined dV_{OUT} ≤ 200 mV**

Buck mode, minimum capacitance C_{OUT}:

$$C_{OUT} = dI_L \times \frac{1}{8 \times dV_{COUT} \times f_{SW}} = 350 \text{ mA} \times \frac{1}{8 \times 200 \text{ mV} \times 380 \text{ kHz}} = 576 \text{ nF}$$

Buck mode, maximum ESR for C_{OUT}:

$$ESR_{COUT} = \frac{dV_{ESR_COUT}}{dI_L} = \frac{200 \text{ mV}}{350 \text{ mA}} = 570 \text{ m}\Omega$$

Boost mode, minimum capacitance C_{OUT}:

$$V_{IN} = V_{\text{driver_min}} = 1.5 \text{ V}, I_{OUT_max} \neq 350 \text{ mA}$$

(specified 200mA, additional margin)

$$C_{OUT} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{dV_{COUT} \times f_{SW}} = \frac{350 \text{ mA} \times \left(1 - \frac{1.5 \text{ V}}{5 \text{ V}}\right)}{100 \text{ mV} \times 380 \text{ kHz}} = 6.4 \text{ }\mu\text{F}$$

Boost mode, maximum ESR for C_{OUT}:

$$ESR_{COUT} = \frac{dV_{ESR_COUT_MAX}}{\left(\frac{I_{OUT} \times V_{OUT}}{V_{IN}} + \frac{dI_L}{2}\right)} = \frac{200 \text{ mV}}{\left(\frac{350 \text{ mA} \times 5 \text{ V}}{1.5 \text{ V}} + \frac{100 \text{ mA}}{2}\right)} = 164 \text{ m}\Omega$$

- **Regarding output ripple voltage: required capacitance is much lower than recommended range of 22 μF to 470 μF.**
- **ESR is the critical parameter for output voltage ripple.**
- **Required ESR for dV_{OUT} ≤ 200 mV of 164 mΩ is within recommended range for stability.**

4 PCB Layout

4.1 Thermal Pad of the Package

The TPIC74100 package is the PWP 20-pin PowerPAD™ plastic small-outline package.

The device package has a thermal pad for optimized transport of the heat from the device. For maximum efficiency, the thermal pad must be attached to a heat spreader (copper area) by using a low thermal impedance attachment method (solder paste or thermal conductive epoxy). In most applications, it is suggested that the ground plane be used as the heat spreader (best compromise between space and performance).

If this needs to be done with the help of thermal vias, use the complete space of the thermal pad for placing several thermal vias.

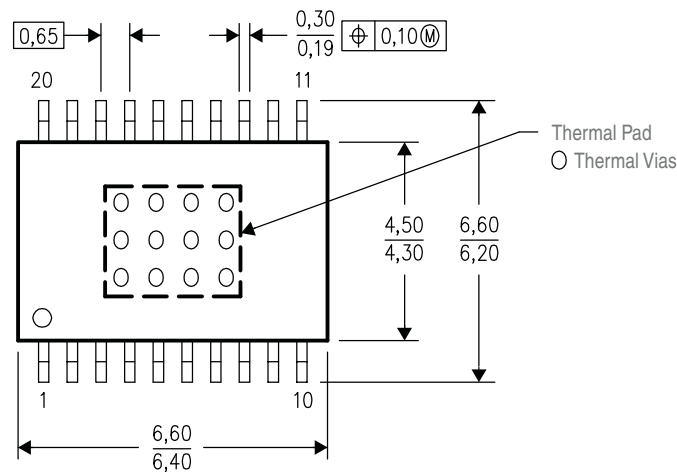


Figure 10. PWP Package With Thermal Pad

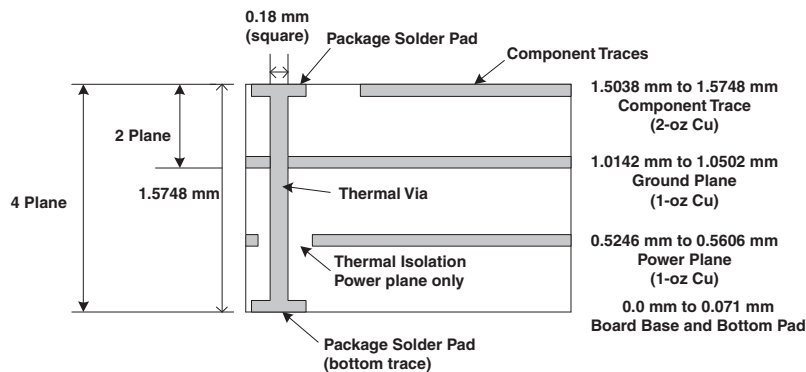


Figure 11. Thermal Vias With Multilayer Board (Side View)

In [Figure 11](#), the thermal via is connected to the internal ground plane. In such a case, the addition of an additional heat spreader on the bottom side is strongly recommended. Copper areas on top or bottom of the board offer much better thermal impedance than internal copper areas.

4.2 Components Placement

The placement of some of the components is critical to the converter efficiency and stability and to the EMI performance of the system. Components need to be placed according to [Table 3](#).

Table 3. Component Placement Priority List

| Priority | Comment | Component |
|----------|---|---|
| 1 | Place as close as possible to the device pins | <ul style="list-style-type: none"> • Inductor L • Output capacitors C_{OUT} and C_{5Vg} • Input capacitor C_{driver} • External Schottky diode • V_{logic} capacitor |
| 2 | Place close to the device pins | <ul style="list-style-type: none"> • Bootstrap capacitors C_{boot1} and C_{boot2} |
| 3 | Least critical components | <ul style="list-style-type: none"> • Pullup resistors for A_{OUT} and RESET • Capacitor at REST • Resistance at R_{mod} • Resistor divider at A_{IN} |

4.3 Traces – Routing

All power traces should use available space for maximum width of the trace. Length of the power traces is critical for EMI radiation. Keep connection traces of the most critical components (Priority 1 components in [Table 3](#)) as short as possible. Avoid routing through different layers. Consider the use of more than a single via if a layer switch is required for a power trace.

4.4 Ground Concept

Using a two-layer ground concept is recommended.

Power ground is connected with the PGND pin. All external components in the power path must connect directly to this power ground layer, including the inductor, input capacitor, output capacitor, 5Vg capacitor, and external Schottky diode.

The second ground layer is connected with the GND pin and the remaining GND pins of the external components, such as the capacitor at V_{logic} and REST, and resistors at A_{IN} and R_{mod} .

Both ground layers are connected to each other at a single location close to PGND and GND of the device.

5 Thermal Analysis

5.1 Terms and Definitions

Maximum power dissipation, $P_{D(MAX)}$:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$$

| | |
|-----------------|--|
| $T_{J(MAX)}$ | – Maximum allowable junction temperature |
| T_A | – Ambient temperature |
| $R_{\theta JA}$ | – Thermal resistance junction to ambient |

Junction temperature, T_J :

$$T_J = P_D \times R_{\theta JA} + T_A$$

$$T_J = (P_{IN} - P_{OUT}) \times R_{\theta JA} + T_A$$

| | |
|-----------|---|
| T_J | – Junction temperature |
| P_D | – Power dissipation |
| P_{IN} | – Input power |
| P_{OUT} | – Output power |
| η | – Efficiency $\eta = (P_{OUT}/P_{IN}) \times 100\%$ |

$$T_J = (1 - \eta/100\%) \times P_{IN} \times R_{\theta JA} + T_A$$

The thermal resistance junction to ambient $R_{\theta JA}$ is specified for systems placed in still air environment unlike the thermal resistance junction to moving air $R_{\theta JMA}$. Several factors have a strong impact on the $R_{\theta JA}$.

$$T_J = T_C + (\Psi_{JT} \times (P_{IN} - P_{OUT}))$$

| | |
|-------------|---|
| Ψ_{JT} | – Junction to top of the package thermal metric |
|-------------|---|

5.2 Package

The TPIC74100 package is the PWP 20-pin PowerPAD plastic small-outline package.

For correct attachment of the thermal pad, certain trace widths, copper size, thermal vias, etc., the following values have been modeled for this package:

- $R_{\theta JA}$: 32.63°C/W
- Ψ_{JT} : 0.607°C/W

See the Texas Instruments application report *PowerPAD™ Thermally Enhanced Package* (literature number [SLMA002](#)).

5.3 Thermal Calculations Example

Application Conditions

- Input: $V_{IN} = V_{driver} = 12\text{ V}$
- Output: $V_{OUT} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$
- Efficiency: $\eta = 80\%$ (estimated)
- Ambient: 100°C

Calculations

$$P_{IN} = \frac{P_{OUT}}{\eta} \times 100\% = \frac{V_{OUT} \times I_{OUT}}{\eta} \times 100\% = \frac{5\text{ V} \times 1\text{ A}}{80\%} \times 100\% = 6.25\text{ W}$$

$$T_J = \left(1 - \frac{\eta}{100\%}\right) \times P_{IN} \times R_{\theta JA} + T_A = \left(1 - \frac{80\%}{100\%}\right) \times 6.25\text{ W} \times 32.63^\circ\text{C/W} + 100^\circ\text{C} = 140^\circ\text{C}$$

→ As explained in [Section 5.1](#), this is a rough estimation.

→ For a closer estimation, the case temperature of the device is measured in the application.

Measured case temperature T_C : $T_J \neq 132^\circ\text{C}$

$$T_J = T_C + (\Psi_{JT} \times (P_{IN} - P_{OUT})) \neq 132^\circ\text{C} + (0.607^\circ\text{C/W} \times (6.25\text{ W} - 5\text{ W})) \neq 132.8^\circ\text{C}$$

This junction temperature is still calculated based values out of a model, but it gives an accurate estimation of the real junction temperature.

Calculations need to be continued accordingly for the external components. In particular, the capacitors for the in and output terminal and the inductor heat themselves due to internal losses.

6 Summary

The sequence of the following questions might help evaluate the exact requirements for the individual power-supply application. Knowing the exact requirements makes it easier to start designing with the TPIC74100. This list does not cover everything, but the most important points to be considered are:

1. Will the device operate in buck mode, boost mode, or in both modes?
 - May influence the selection of external components
2. Is the continuous/discontinuous mode threshold important?
 - Depends on load current and does influence EMI performance
 - Can be influenced by the inductance of the inductor
3. Is short-circuit protection required?
 - Inductor needs to be selected with appropriate saturation current
4. Low-power mode operation?
 - When to enable (verify load current conditions)?
5. What are the efficiency and EMI performance requirements?
 - External Schottky diode?
 - Resistor for modulation?
 - Slew rate control?
 - Add some fast ceramic-type capacitors?
6. Is ripple of the output voltage important?
 - Low-ESR output capacitor
 - Optional, place capacitors in parallel
7. Is the RMS current capability of the input and output capacitors sufficient?
 - Verify for input capacitor, especially in buck mode
 - Verify for output capacitor, especially in boost mode
8. Is the second output voltage at 5Vg required?
 - Additional output capacitor at pin 5Vg
9. Layout?
 - Critical components as close as possible to the device?
 - Power traces at maximum width?
10. Is high-temperature range required?
 - Thermal pad attached to heat spreader?
 - External components verified; self heating due to RMS current?

7 References

TPIC74100-Q1 Buck/Boost Switch Mode Regulator data sheet (SLIS125)

PowerPAD™ Thermally Enhanced Package (SLMA002)

IC Package Thermal Metrics (SPRA953)

Understanding Buck Power Stages in Switch-Mode Power Supplies (SLAV057)

Understanding Boost Power Stages in Switch-Mode Power Supplies (SLVA061)

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