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Interface Circuits for SCSI

ABSTRACT

This design note provides information concerning the designing of SCSI interface circuits. The three types of SCSI transmission (single-ended, high-voltage differential, and low-voltage differential) are discussed. Single-ended SCSI topics include: termination (passive and active), signal transitions, current-source termination, and power considerations. High-voltage differential SCSI topics include: using the SN75976A, skew considerations, power dissipation, and driving wired-OR SCSI lines. Low-voltage differential SCSI topics include: an overview, electrical characteristics, and using the SN75LVDM976.

Introduction

Small computer systems interface (SCSI) is a family of international and industry standards developed by the T10 committee. T10 is a Technical Committee of the National Committee on Information Technology Standards (NCITS). NCITS is accredited by, and operates under rules that are approved by, the American National Standards Institute (ANSI). SCSI documents a computer peripheral bus and command set and is a high-performance data interface that distributes data independently of its host, helping to free up the host for more user-oriented commands. Already there are a large number of disk drives, notebook PCs, and CD-ROM drives incorporating a SCSI port (see Figure 1).

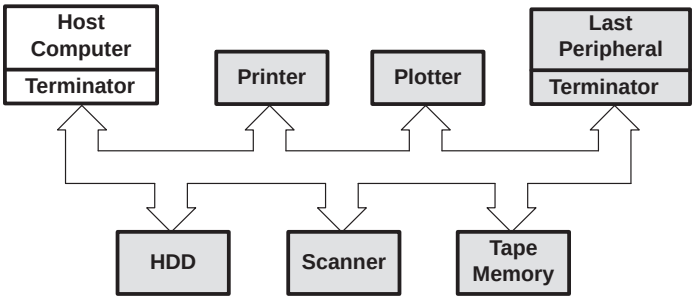


Figure 1. Typical SCSI Peripheral Bus Layout

SCSI now has many options for the physical layer, the most widely used being the basic 8-bit parallel single-ended I/O bus with a parity checking line and nine control/handshake lines, making 18 lines total. There are options available to increase the data transfer rate by increasing the bus width and/or the signaling rate. Most high-performance systems now are operating with 2-byte transfers at 20-million transfers per second (MXfer/s) for a peak data transfer rate of 40-million bytes per second (Mbyte/s). This is referred to as wide SCSI and maintains the nine handshake lines, making the total number of signals 27.

It is beyond the scope of this document to discuss the higher layers of the SCSI standard. This document concerns itself with the electrical layer only. For more information on the entire standard, refer to the numerous publications on SCSI.

There currently are two approved signaling modes allowed in the electrical specifications in the SCSI standard — single ended and differential. A third mode, low-voltage differential or LVD-SCSI is nearing standardization, with silicon now appearing to support even higher signaling rates.

Single-Ended Mode — The single-ended mode utilizes TTL logic levels and is intended primarily for applications with a cabinet or for single-user systems without many peripherals. The maximum line length varies a great deal on the number of peripherals and other system influences, but is usually no more than 6 meters at the fast-SCSI transfer rate of 10 MXfer/s. When using ultra SCSI at rates of 20 MXfer/s this length normally is 3 m, or half the fast SCSI length. Also, the maximum number of connections to the bus may have to be limited to meet the speed or distance requirements.

High-Voltage Differential Mode — The HVD-SCSI mode uses ISO-8482 (TIA/EIA-485) compliant drivers and receivers to significantly improve the electrical performance of the interface circuit. Differential SCSI allows longer cables (25 m), more devices (up to 32), live insertion (hot plugging), and faster signaling than does single-ended SCSI. Differential SCSI is used primarily in multiuser systems when transmitting data between cabinets, on heavily loaded buses, or with high-reliability/availability.

Low-Voltage Differential Mode — LVD-SCSI is an adaptation of TIA/EIA-644 for multipoint buses and maintains many of the advantages of HVD-SCSI, but with less noise margin. The signaling levels are about three times lower than those of HVD-SCSI, but at much lower power consumption. The lower noise margins of LVD-SCSI require fewer and longer segments between devices than HVD-SCSI. LVD-SCSI can be considered as a speed upgrade for single-ended SCSI systems.

Single-Ended SCSI

Termination of Single-Ended Bus

Termination of the single-ended SCSI bus is becoming increasingly important as designers strive for faster system speeds. If error-free data at signaling rates of 10 Mbit/s over a 6-meter bus is to be achieved, then signal integrity must be optimized. Termination reduces unfavorable transmission-line effects such as reflections and distortion that can degrade system performance as signal speeds increase. Bidirectional buses, such as SCSI, require terminators at each end of the cable.

Signal Transitions

The potential for high rates depends on quick, clean transitions between low and high signal levels. The range of SCSI signals is shown in Figure 2. A low-to-high transition or deassertion of a signal is initiated by driver output causing an instantaneous voltage step to travel down the line.

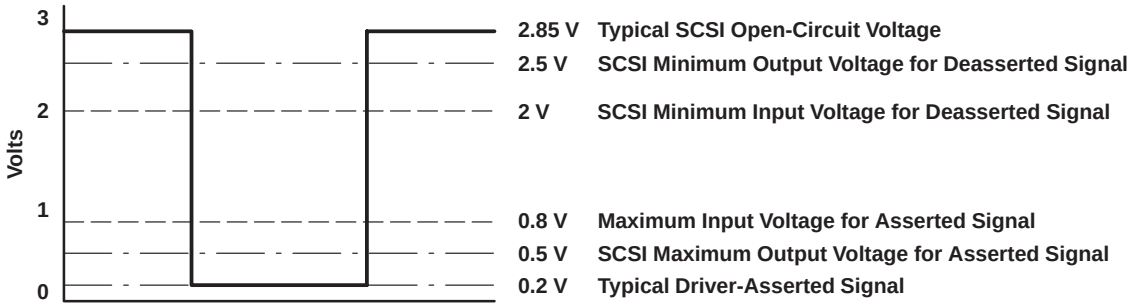


Figure 2. Single-Ended SCSI Signal Levels

The size of the first step on deassertion depends on:

- The amount of current in the line just prior to deassertion (I_L),
- Any current from the driver (I_{OH})
- The load impedance on the driver output (Z_L), where $Z_L = Z_O/2$
- Voltage just prior to deassertion (V_{OL}),

and can be calculated as follows:

$$V_S = V_{OL} + Z_L \left(2I_L + I_{OH}\right)$$

To achieve the maximum data rate, the first step needs to exceed the receiver threshold voltage in a single transition. Although the 110-Ω impedance of a typical SCSI ribbon cable suggests that this requires only limited line-current capability, the impedance seen by a signal is always less than half the specified cable value. Extra capacitance due to peripheral connections to the bus, transmission-line effects, and the position of the signal source can combine to reduce the effective impedance to 30Ω, or less.

To make up for this low impedance, it is the terminator's job to source as much current as possible during deassertion. This role is restricted by the SCSI specification, however, which limits each terminator to supplying a maximum of 24 mA to prevent the line current from exceeding the 48 mA current sink limit of the open-collector drivers.

The role of the SCSI terminator is not confined to low-to-high signal transitions. Once a signal has been deasserted, the terminator is required to bias the bus lines to the correct open-circuit voltage level, and thereby provide maximum noise margins.

Passive and Active SCSI Termination

SCSI termination traditionally has been carried out using passive termination networks. As illustrated in Figure 3, these consist of two resistors for each signal line; a 220-Ω pullup resistor connected to the termination power source (TERMPWR); and the 330-Ω pulldown resistor connected to ground. A Schottky diode is needed by all termination schemes to protect the power source from reverse currents.

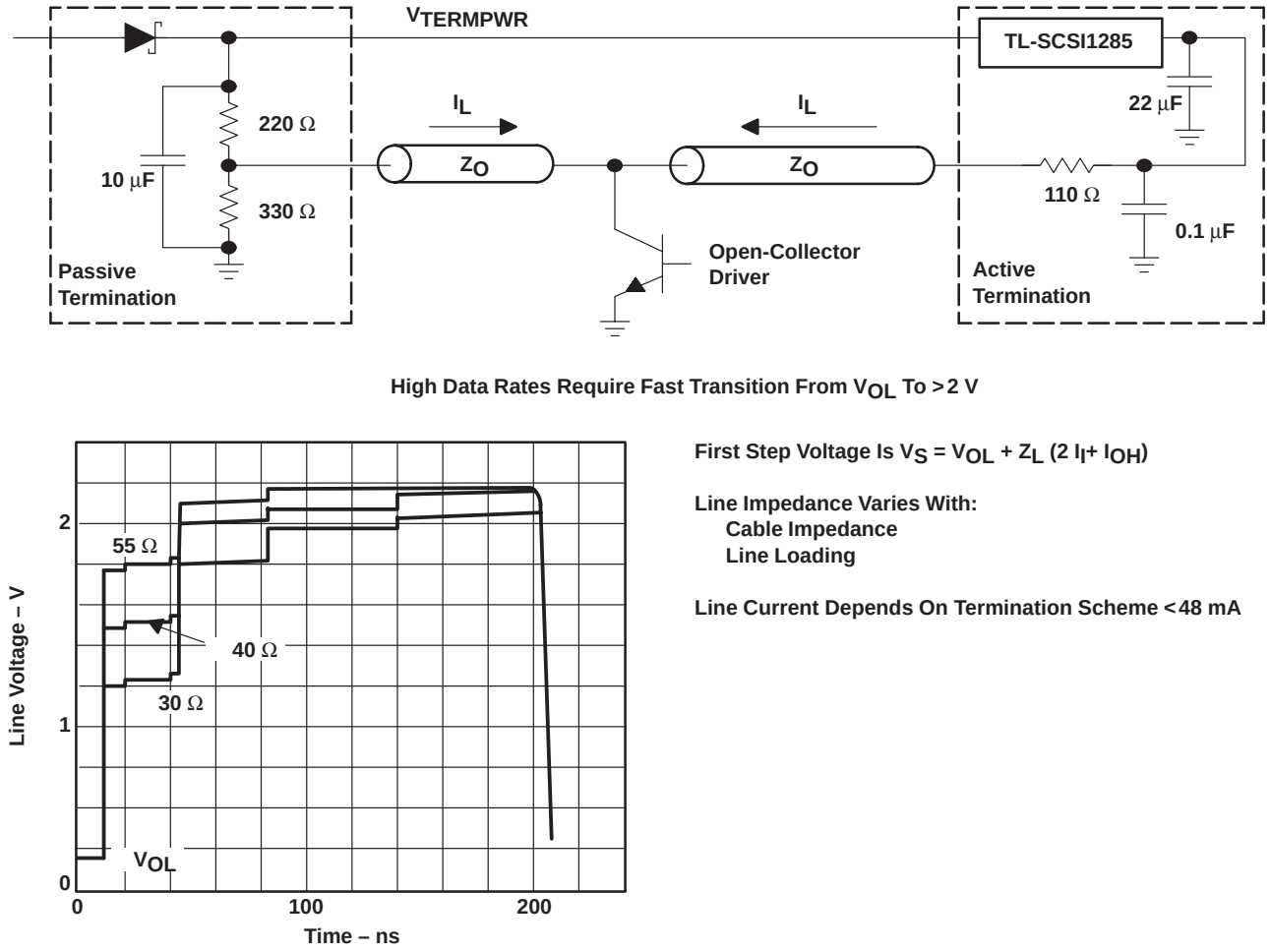


Figure 3. Single-Ended SCSI Termination

This type of termination at each cable end typically results in a maximum line current of around 34 mA. Assuming the terminator is on a heavily loaded bus with a load impedance of approximately 32 Ω, the equation in Figure 3 gives a first step value of 1.76 V — well short of the desired 2-V level.

In addition to this limited-current capability and the power-consumption penalty imposed by the resistor dividers, passive terminators also suffer from an unregulated line bias voltage. As a result, the line voltage fluctuates with variations in the load current and TERMPWR leading to smaller noise margins and reduced data rates.

The most common alternative to passive termination replaces the resistive network with a voltage regulator in series with a single 110-Ω resistor for each line (see Figure 3). This method, known as Active, Boulay, or alternative-2 termination, was developed to overcome two of the main shortcomings of passive termination.

The 110-Ω resistors increase the typical line current available on deassertion to 42 mA, which, from a transmission line viewpoint, is equivalent to a 35% increase in the output voltage. The line current and the high-level noise margins also are more stable since TERMPWR no longer is used to set the bias voltage directly. Instead it is used to form the input to the voltage regulator, which then provides a regulated bias voltage (see Figure 4).

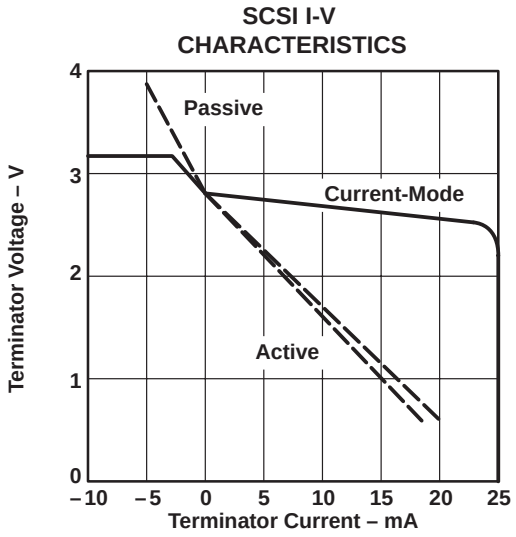
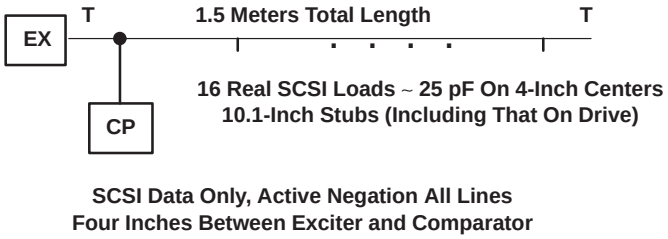


Figure 4. Current-Mode Termination

Current-Source Termination Using the SN75LBC968

There are numerous analog problems associated with driving the single-ended SCSI bus and single-ended parallel buses in general. The SN75LBC968 addresses most of them. This device exhibits the analog performance to maximize first-step assertion levels in wired-OR lines and minimize radiated emissions, crosstalk, and radiated emission susceptibility.



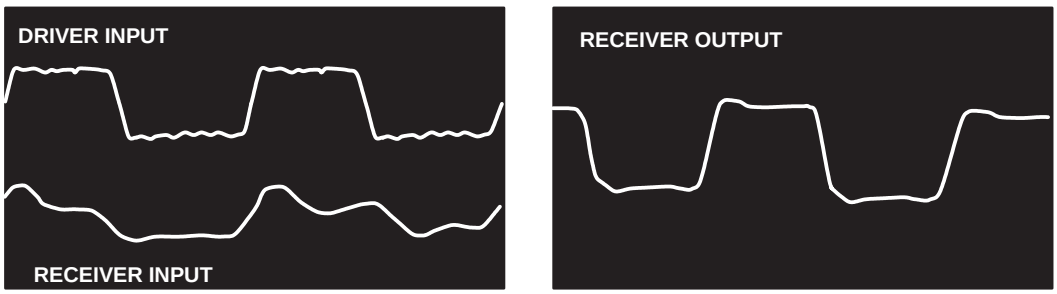


Figure 5. First-Step Voltage Levels

The fundamental cause of the low first-step level is added loading of the bus with distributed capacitance from the attached devices. The ’968 addresses this by offering a lower capacitance to the bus of only 13.5 pF and nearly one-half of the maximum allowed by standard. The current-mode termination of the SN75LBC968 supplies a constant current to the line when the bus voltage falls below 2.5 V. This makes the termination current (and the next low-to-high voltage step) independent of the low-level (asserted) bus voltage, unlike voltage-mode terminators. The constant current supplied by the ’968 provides 16% more minimum current than Boulay termination and 33% more than passive termination. This extra current translates directly to first-step noise margin. The line drivers of the SN75LBC968 have a feature that was introduced in the SCSI standards to address the first-step problem called active negation. Active negation is a controlled amount of output current from the driver during the transition from assertion to negation and now is required on the highest speed versions of SCSI.

There is a capacitance between parallel conductors that is a function of the dielectric, distance, and conductor shape. It is also known that the magnitude of the current through a capacitor is the product of e, ω, and C, where e is the voltage across the capacitance, C is the capacitance, and ω is the angular frequency ($2\pi f$) of the signal. In a parallel data bus, the current through this coupling capacitance generates a noise voltage in adjacent signal lines and, if large enough, can cause erroneous interpretation of the signal logic state. This is crosstalk and it is a major limitation to the ultimate data-transfer rates of single-ended parallel buses.

Since there is usually little that can be done with C or e, the SN75LBC968 driver circuit reduces the amount of crosstalk by limiting ω. The highest frequency in a binary signal is present in the transition between logic states. By necessity, three to five times the fundamental switching frequency is required to adequately define the instance between states. However, energy at higher frequencies is not needed for data transmission and can only lead to more emissions and crosstalk.

Since all single-ended SCSI drivers may not be as analog friendly as the ’968s, the receiver of this device has a noise filter and a large amount of input hysteresis to reject all but the wanted signals. The noise filter rejects voltage spikes less than 5 ns, while the 600 mV of hysteresis rejects lower frequency noise with magnitudes below this level. These features help reject crosstalk-induced noise, but make the bus less susceptible to noise from sources outside the bus as well.

Nine current-mode terminators have been integrated with nine-line transceivers that provide a common multiple to the byte-parity-arranged SCSI bus. With the nine control lines, an 8-bit SCSI bus can be implemented with 2 transceivers, a 16-bit bus with 3, a 32-bit bus with 5, and so on. The other features of this device, such as 3-V logic compatible inputs, power-up/-down glitch protection, and shrink small-outline packaging with flow-through architecture, make this an excellent solution to driving high-speed parallel data buses with single-ended signals.

Power Considerations

As well as enabling increased date rates, termination also increases the power consumption of a SCSI system. As SCSI has found increased usage in portable or battery-powered systems, this has become more important. Exactly how much more power is needed depends on the method of termination, but this is not quite as obvious as it may first seem.

During data-on periods, the power dissipation of each of SCSI termination method is very similar. For an 8-bit bus with all the data lines asserted, the power dissipation in the termination is approximately 1 W.

During data-off periods, the position significantly changes. The resistor dividers of a passive terminator still draw around 750 mW of power. Both the SN75LBC968 and Boulay terminators, however, require a total quiescent current of less than 10 mA, providing a 30× saving in power consumption.

High-Voltage Differential SCSI

SN75976A — Nine-Channel RS-485 Transceiver

As discussed earlier, SCSI comes in 9-bit slices: 8 data with parity and 9 control lines, making 18 signals, or channels, for 8-bit SCSI and 27 channels for wide SCSI. In the past, the only differential transceivers capable of transmitting at a 10 Mbit/s signaling rate or above were manufactured in low-power Schottky (LS) and advanced low-power Schottky (ALS) bipolar technologies. Considering the power needs of bipolar and the number of channels, the power consumption for one SCSI interface could use up to 4 W and require multiple packages for the 485 transceivers.

From a designer's viewpoint, 4 W is a considerable amount of heat to remove from a system. This is especially so in the case of compact hard disk drives. A further factor is board area, using one discrete transceiver for each channel is unacceptable for many applications.

From an integrated circuit designer's viewpoint, integrating multiple transceivers is possible; however, the limiting factor once again is power dissipation. The SN75976A is designed to overcome both the problems of power dissipation and integration. The device incorporates on a single IC, nine RS-485 configurable transceivers, each capable of operating at 20 Mbit/s or higher. This is made possible using LinBiCMOS™ technology. With all drivers disabled, the quiescent power consumption of the '976A is a mere 50 mW. With all drivers enabled, the quiescent consumption rises to 300 mW, a considerable saving over LS and ALS parts. The package size also has been reduced to a minimum using the 0.5 mm pitch 56-pin thin shrink small-outline package (TSSOP) which reduces board area significantly compared with alternate packages such as plastic leaded chip carrier (PLCC). Irrespective of the device power, there is still the relatively high line current. The TSSOP package has been thermally enhanced to handle this level of power dissipation. This point is covered later in the discussion of the thermal characteristics of the package.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

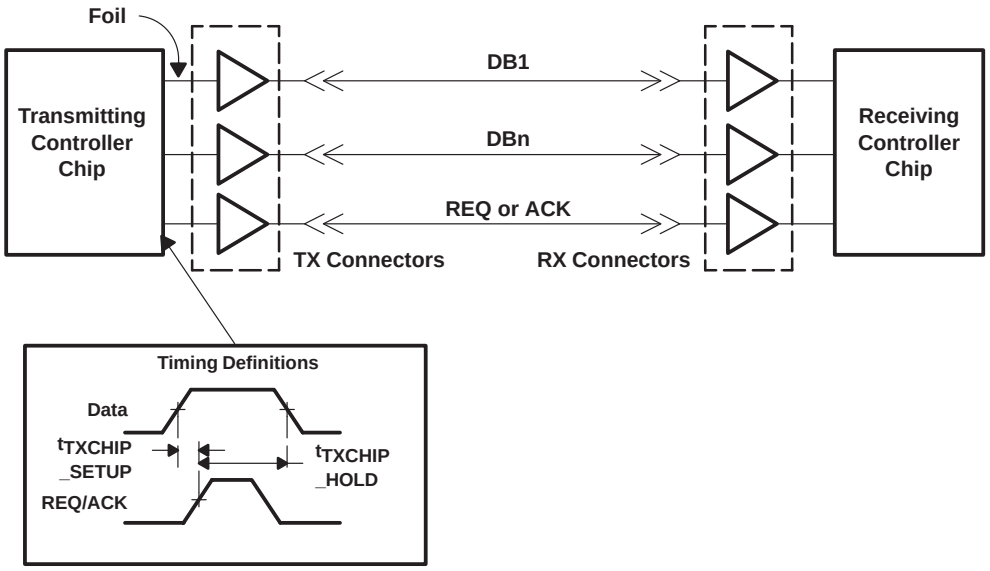
SCSI Skew Considerations

SCSI, as discussed earlier, is a parallel data bus. This is also the case with the intelligent peripheral interface (IPI). IPI is similar to SCSI in that it is a high-speed peripheral bus with the same high-speed differential interface requirements. Being parallel, both standards transfer data over the cable more than one bit at a time. SCSI and IPI allow 8-bit (one byte) or a 16-bit (one word) data width and transfers as often as once every 50 ns or 20 million transfers per second.

Since the logical state of any one bit can change every 50 ns, this defines a period during which the logical state should be valid across the bus. This is the unit interval (UI). The voltage transitions that define the start and end of the UI can propagate along the bus at different velocities due to the physical differences along each electrical path. So the original UI at the start of the electrical path is different at the destination.

Time variation of the defining voltage transitions typically is called skew. The limit for skew, designated $t_{sk(lim)}$, is the fastest propagation delay minus the slowest propagation delay along any part of the bus. This, in effect, reduces the UI by $t_{sk(lim)}$, establishing a minimum unit interval, UI_{min}, that can be transmitted with a particular data bus.

The SCSI standard defines UI_{min} in terms of setup and hold times at the SCSI connector for interoperability with any other SCSI device. The requirements are summarized in Figure 6.



SCSI-3 Standard Requirements:

- $t_{TXCHIP\_SETUP} - t_{SK\_DRVR} - t_{SK\_FOIL} = t_{TXCONNECTOR\_SETUP} \geq 23$ ns
- $t_{TXCHIP\_HOLD} - t_{SK\_DRVR} - t_{SK\_FOIL} = t_{TXCONNECTOR\_HOLD} \geq 33$ ns
- $t_{RXCONNECTOR\_SETUP} = t_{RXCHIP\_SETUP} - t_{SK\_RCVR} - t_{SK\_FOIL} \geq 15$ ns
- $t_{RXCONNECTOR\_HOLD} = t_{RXCHIP\_SETUP} - t_{SK\_RCVR} - t_{SK\_FOIL} \geq 25$ ns

Figure 6. SCSI-3 Fast-Transfer Skew Budget

The budget behind the connector is left to the designer and depends on the SCSI controller, transceivers, and layout being used. Table 1 shows some skew budget examples with various controller chips that comply with the requirements at the SCSI connector. The recommended column is data for the worst case number for SCSI controllers surveyed by the SCSI SPI working group and budgets 8 ns for the external driver and 9 ns for the external receiver. A similar table can be constructed for fast-20 timing.

Table 1. Transceiver Skew Budgets for Various Fast-SCSI Controllers

PARAMETER	RECOMMENDED BUDGET	VENDOR A	VENDOR B	VENDOR C	UNITS
min Tx_controller_setup =	32	30	35	35	ns
min Tx_controller_hold =	42	42	45	45	ns
min Rx_controller_setup =	5	0	5	0	ns
min Rx_controller_hol =	15	20	15	10	ns
t_{sk_etch} =	1	1	1	1	ns
max t_{sk_dvr} =	8	6	11	11	ns
max t_{sk_rvc} =	9	4	9	14	ns

The time it takes from the input-state change to one transceiver of the ‘976A until a change in state at the output is called the propagation delay time. For a driver this is designated as $t_{d(D)}$ and for a receiver this is designated t_{pd} and does not differentiate whether the logical transition is from high-to-low or low-to-high level. The $t_{sk(lim)}$, as specified in the data sheet, and the recommendation of the SCSI standard are assured by measuring the propagation delay time of each channel of each ‘976A and accepting only those devices within the specified $t_{sk(lim)}$ range. To keep the production costs reasonable, these tests are done at 25°C and at 70°C ambient temperatures at a V_{CC} of 5 V.

Admittedly, the die temperatures and supply voltages are all the same (or nearly the same) during TI’s production testing, and the same would not necessarily be seen in actual use. However, the sensitivity of the propagation delay times to these factors is the same and is repeatable from device to device. In other words, as long as the operating environment of all of the SCSI interface channels is similar, the change in propagation delay times from the data sheet conditions is the same. This maintains the $t_{sk(lim)}$ specification even though the actual propagation delay times may change slightly.

It is nearly impossible to predict the instantaneous die temperatures of these devices in actual use. Due to the nondeterministic nature of the state of any one channel and the averaging effect of nine channels and of the package thermal time constant, the die temperature must be considered using the mean power dissipation. It also is reasonable to assume that mean power dissipation of separate devices on the same printed circuit board is close to each other and the temperature of the air around them does not have a large gradient between them. Even if there were an air temperature gradient of 45°C, there would be only about a 2-ns difference in the driver propagation delay times and little or no difference in the receiver propagation delay times. If such a temperature gradient actually exists across a board, it is likely that skew budgets are not going to be the problem with the equipment.

Power-Dissipation Considerations

Power Dissipation – To understand the SN75976A power dissipation when connected to a SCSI bus and the subsequent heat-sinking requirements, a realistic model for the power consumption under working conditions needs to be developed. The power dissipation within the silicon must be considered. There are three primary sources — the dc quiescent power, the ac or switching power, and the dc or resistive losses in the output drivers.

The current necessary to bias the nine driver circuits of an enabled ‘976A is typically 39.7 mA and a maximum of 60 mA. Nine enabled receiver circuits require 25.2 mA typically and 45 mA maximum. These values are from statistical characterization of seven different wafer lots over a supply voltage range of 4.75 V to 5.25 V and a case temperature range of 0°C to 125°C.

It follows that the driver quiescent power consumption, P_{DCC} is

$$P_{DCC} = I_{CC} \times V_{CC}$$
$$= 39.7\ mA \times 5\ V = 198.5\ mW\ average$$
$$= 60.0\ mA \times 5.3\ V = 318.0\ mW\ maximum$$

The increase in the average I_{CC} for an unloaded driver of the SN75976A was measured on four representative samples. The average increase was 4.88 mA/channel when switching at 10 MHz (20 MXfer/s), a 50% duty cycle, and at a V_{CC} of 5 V. At a V_{CC} of 5.25 the single largest measured increase was 5.3 mA/channel.

One driver’s switching loss at 10 MHz:

$$P_{DAC} = I_{CC} \times V_{CC}$$
$$= 4.9\ mA \times 5\ V$$
$$= 24.4\ mW/channel\ typical$$
$$= 27.8\ mW/channel\ maximum$$

A receiver, switching at the same frequency and duty cycle with unloaded outputs, consumed an additional 2 mA/channel above the steady state on average. The maximum was 2.5 mA/channel on one sample at a V_{CC} of 5.25 V.

One receiver’s switching loss at 10 MHz:

$$P_{RAC} = I_{CC} \times V_{CC}$$
$$= 2.0\ mA \times 5\ V$$
$$= 10.0\ mW/channel\ typical$$
$$= 13.1\ mW/channel\ maximum$$

The output stage losses vary with either the magnitude of the output voltages, the output transistor saturation or drain-to-source voltages, and with the load conditions. The following is derived from the solution of the equivalent circuit of a differential SCSI bus and no further proof is included in this analysis.

The typical single-ended output voltages of the ’976A driver have been characterized with a SCSI load test circuit with the following results.

Table 2. SN75976A Output Voltages With a SCSI Load

PARAMETER			TYPICAL† (V)	WORST CASE‡ (V)
V_O	+ SCSI line voltage	Asserted	1.5	1.3
		Negated	3	3.7
V_O	– SCSI line voltage	Asserted	3.3	3.9
		Negated	1.6	1.5
V_{OD}	Differential output voltage	Asserted	–1.8	–2.6
		Negated	1.4	2.2

† Typical is the statistical average of the measurements on 268 samples from 7 wafer lots at a case temperature of 25°C and a V_{CC} of 5 V.
‡ Worst case is the maximum differential output voltage measured on 268 samples from 7 wafer lots at a case temperature of 125°C and a V_{CC} of 5.25 V.

Solution of the circuit with the SCSI test load and the voltages in Table 2 results in a typical power dissipation in the output transistors of 117 mW when asserted and 60 mW when negated. The worst case power is 167 mW asserted and 113 mW negated.

Driver output dc losses:

$$P_{DOH} = 117.0 \text{ mW/channel typical}$$
$$< 167.0 \text{ mW/channel maximum}$$

$$P_{DOL} = 60.0 \text{ mW/channel typical}$$
$$< 113.0 \text{ mW/channel maximum}$$

At an I_{OL} of 8 mA, the typical receiver V_{OL} is 0.6 V with a maximum test limit of 0.8 V. At an I_{OH} of –8 mA, the typical V_{OH} is 4.5 V, with a minimum limit of 2.4 V.

Receiver output dc losses:

$$P_{ROH} = I_{OH} \times (V_{CC} - V_{OH})$$
$$= 8 \text{ mA} \times (5 \text{ V} - 4.5 \text{ V})$$
$$= 4.0 \text{ mW/channel typical}$$
$$< 8 \text{ mA} \times (5.3 \text{ V} - 2.4 \text{ V})$$
$$= 23.2 \text{ mW/channel maximum}$$

$$P_{ROL} = I_{OL} \times V_{OL}$$
$$= 8 \text{ mA} \times 0.6 \text{ V}$$
$$= 4.8 \text{ mW/channel typical}$$
$$< 8 \text{ mA} \times 0.8 \text{ V}$$
$$= 6.4 \text{ mW/channel maximum}$$

The components of the power dissipation in the SN75976A are summarized in Table 3.

Table 3. Components of Power Dissipation

PARAMETER		TYPICAL	MAXIMUM	UNIT
P_{DCC}	Steady-state supply power for nine drivers	198.5	318	mW
P_{DAC}	Switching power for one driver at 10 MHz	24.4	27.8	mW/channel
P_{DOH}	Driver output power loss when asserted	117	167	mW/channel
P_{DOL}	Driver output power loss when negated	60	113	mW/channel
P_{RCC}	Steady-state supply power for nine receivers	126	238.5	mW
P_{RAC}	Switching power for one receiver at 10 MHz	10	13.1	mW/channel
P_{ROH}	Receiver output power loss when asserted	4	23.2	mW/channel
P_{ROL}	Receiver output power loss when negated	4.8	6.4	mW/channel

Device Power – To determine the total power dissipated in the package, the operation of the device and the power component contributions must be evaluated. The steady-state quiescent power is a constant, but the switching power and output stage power depends on the data being transmitted or received and the duration of the transfer. Three cases are analyzed: 1) nine channels continuously transmitting random data to a fast-20 SCSI bus, 2) nine channels continuously receiving random data from a fast-20 SCSI bus, and 3) the unlikely assertion of all nine bits continuously.

Since the assumption in case 1) and 2) is random data, the probability that any one bit on the bus is asserted is equal to the probability of it being negated. With equal probability and a long observation period relative to the data transfer period, the mean power in an output stage is the average of the high-level and low-level values. For nine channels and the three cases;

1) $P_{DO1} = \frac{P_{DOH} + P_{DOL}}{2} \times 9$

2) $P_{RO2} = \frac{P_{ROH} + P_{ROL}}{2} \times 9$, and

3) The driver outputs are continuously asserting the bus so, $P_{DO3} = P_{DOH} \times 9$

The circuit switching losses, P_{DAC} and P_{RAC}, were measured with the switching loss occurring on every cycle. Because the state of the output is random and non-deterministic, the probability that the driver output changes state on the next cycle is equal to the probability that it will not. Again, over a long observation period, the mean switching power for each operating case is

1) $P_{DAC1} = \frac{P_{DAC}}{2} \times 9$

2) $P_{RAC2} = \frac{P_{RAC}}{2} \times 9$

3) The driver outputs are continuously asserting the bus so, $P_{DAC3} = 0$

The power dissipated in the package for the three cases is then

$$P_{D1} = P_{DCC} + \left(\frac{P_{DOH} + P_{DOL}}{2} + \frac{P_{DAC}}{2} \right) \times 9$$

$$P_{D2} = P_{RCC} + \left(\frac{P_{ROH} + P_{ROL}}{2} + \frac{P_{RAC}}{2} \right) \times 9$$

$$P_{D3} = P_{DCC} + P_{DOH} \times 9$$

Table 4. Device Power for Three Cases

PARAMETER		TYPICAL	MAXIMUM	UNIT
P_{D1}	Power dissipation when transmitting at 20 MXfer/s	1104	1703	mW
P_{D2}	Power dissipation when receiving data at 20 MXfer/s	210	430	mW
P_{D3}	Power dissipation with all drivers asserted	1251	1821	mW

Junction Temperature – Measurements of the SSOP-56 package and lead frame used on the SN75976ADL were performed on a 13.0 cm by 9.8 cm six-layer printed circuit board. The board was built with the ground and heatsinking pins soldered to individual pads and connected to a second-layer ground plane through 0.15-mm etch runs. There was one common via interconnect per side (see *Measurement of $R_{\Theta JA}$ and $R_{\Theta JC}$*). The ground plane was 0.254 mm below the surface of the 1.6-mm-thick board and was a 1-oz. copper layer. The results of tests on two samples were an average $R_{\Theta JA}$ of 49.7°C/W with a watt of power dissipation and no airflow.

Measurements on six TSSOP-56 packages and lead frames used on the SN75976ADGG were performed. The test board was 13.7 cm by 8 cm by 1 mm thick with a ground and V_{CC} plane of 1-oz. copper. The ground and heatsinking pins were soldered to individual pads and connected to the ground plane through 0.15 mm etch runs and one common via interconnect per side. The result of the test was an average $R_{\Theta JA}$ of 46.7°C/W at one watt of power dissipation and no air flow.

Using a rounded 50°C/W for each package, the mean junction temperature rise above ambient can then be calculated. Table 5 shows the results for each case using the relationship $T_J - T_A = R_{\Theta JA} \times P_D$.

Table 5. Estimated Junction Temperature Rise Above the Free-Air Temperature

PARAMETER		TYPICAL	MAXIMUM	UNIT
T_{J1}	Junction temperature rise when transmitting at 20 MXfer/s	55	85	°C
T_{J2}	Junction temperature rise when receiving data at 20 MXfer/s	10	21	°C
T_{J3}	Junction temperature rise with all drivers asserted continuously	63	91	°C

Conclusion – Most designs impose two junction-temperature restrictions:

1. The junction operating temperature should not exceed 150°C under worst case operating conditions
2. The mean operating junction temperature should be no more than 110°C.

The junction temperature rise above the free-air temperature is estimated in Table 5 for three operating conditions. The worst-case temperature rise is T_{J3} and is applicable to requirement 1 above. Written in equation form and solving for T_A,

$$T_A + T_{J3} < 150°C$$

$$T_A < 150°C - T_{J3}$$

$$T_A < 150°C–90.9°C = 59.1°C$$

Evaluation of the mean operating junction temperature can vary a great deal, based on the assumptions of mean free-air temperature and transmit-to-receive duty cycles. In any case, the use of the typical values T_{J1} and T_{J2} is required. The following table calculates the projected mean junction temperature for various duty cycles and ambient air temperatures.

Table 6. Projected Mean Junction Temperatures vs Duty Cycles and Free-Air Temperature

TRANSMIT	RECEIVE	MEAN T_J (°C)		
		T_A = 25°C	T_A = 55°C	T_A = 70°C
100%	0%	80.2	110.2	125.2
67%	33%	65.4	95.4	110.4
50%	50%	57.9	87.9	102.9
33%	67%	50.3	80.3	95.3
0%	100%	35.5	65.5	80.5

Driving the Wired-OR SCSI Lines With the SN75976A

The control lines of the SCSI bus have three wired-OR lines, they are busy (BSY), reset (RST), and select (SEL). These lines are wired-OR in that the line drivers connected to these lines drive in one direction only (assertion) and are changed to 3-state (high impedance) when negated. This allows numerous drivers to be active at the same time without affecting the logic state of the line and requires that all drivers be released or off before the logical state can change. When are changed to 3-state, the bus termination network passively negates the signal.

The technique used for wired-OR operation with differential transceivers is to input the signal into the driver enable terminal and connect the driver input to a fixed logic level input. When the input signal to the driver enable is active (high), the driver becomes enabled and the outputs drive the SCSI bus to the state of the driver input. When the input signal at the driver enable goes low, the driver turns off and allows the bus termination to negate the signal on the bus after all other drivers on the bus also are shut off.

Many communications controllers used for differential SCSI have separate inputs and outputs for these signals. When used with the SN75176-type RS-485 transceiver, the controller I/Os can be directly connected to separate driver enable inputs or receiver outputs. The SN75976A device does not have a separate driver input and receiver input; these are tied together internally to save terminals.

Controllers with separate I/Os still can be used with the ’976A using the connections shown in Figure 7. The controller output goes high and enables the driver and disables the receiver. Upon disabling the receiver, the external pullup or pulldown resistor drives terminal A of the ’976A to the correct level for bus assertion and the driver asserts the SCSI signal line. When the controller output goes low, the driver disables and allows the termination to negate the bus signal. After a short delay, the receiver outputs are enabled and reflect the logical state of the bus signal.

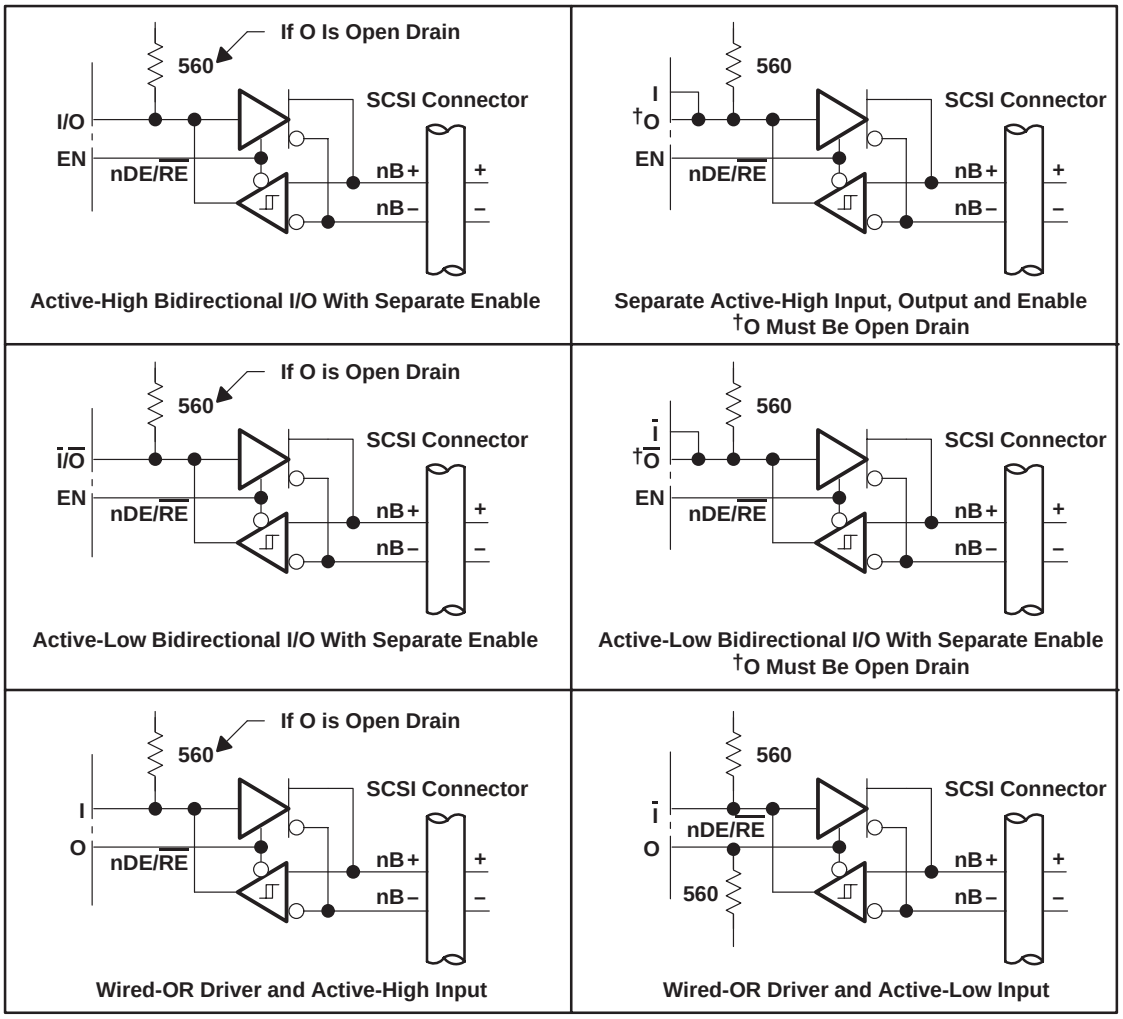


Figure 7. Typical SCSI Transceiver Connections

Low-Voltage Differential SCSI

Overview

Low-Voltage Differential SCSI (LVD-SCSI) is the latest signaling technology for multipoint or multiplexed data buses. LVD-SCSI evolved from the TIA/EIA-644 electrical specification with adaptations to support the lower driver load impedance, reflections, and fault-conditions that can be encountered in this type of bus architecture.

Since this technology is a recent development, most of the following text describes the standard and application. Finally, the SN75LVDM976 dual-mode transceiver is introduced.

General Description

An LVD-SCSI system consists of up to 16 compatible devices connected to a single continuous bus segment. The segment can be constructed of any type of conductor as long as it meets the specified electrical requirements. Normally, shielded twisted-pair cable or a printed circuit board backplane is used.

The top data-signaling rate over a bus segment is specified to be 40 Mbit/s or MXfer/s with the clock operating at 40 MHz. At these signaling rates, the cable or backplane definitely takes on distributed parameter circuit characteristics and those of the transmission-line model. The effects of loads presented by the devices distributed along the transmission line further complicate the system design by lowering the effective load impedance to the drivers and the wave propagation velocity along the media. Allowances have been made in the electrical specification to cover other factors such as, reflections, attenuation, and noise coupling.

As with any parallel bus, the system timing constraints may further limit the data transfer rate under that which the electrical layer could theoretically support. The timing margin is reduced by skew between the clock and data bits from intersymbol interference and propagation delay differences between the electrical paths. This, along with the tolerances provided with the initial setup and hold times of the transmitting or receiving controller, make accounting for every nanosecond of time delays a requirement.

None of these issues is unique to LVD-SCSI. They apply to any bus of similar architecture. What LVD-SCSI does provide is the inherent electrical advantages of balanced signaling with much lower power requirements than with 5 V-based interfaces.

Electrical Characteristics

Drivers – An LVD-SCSI driver is required to drive the test circuit shown in Figure 8 to the levels shown in Table 7. The test circuit is constructed to simulate the load presented to a driver in the middle of a cable of 110-Ω differential characteristic impedance terminated at both ends by an LVD-SCSI termination with nominal characteristics. The voltages V1 and V2 are chosen to provide the nominal differential bias voltage provided by the termination and a common-mode load over the allowed range of ground noise.

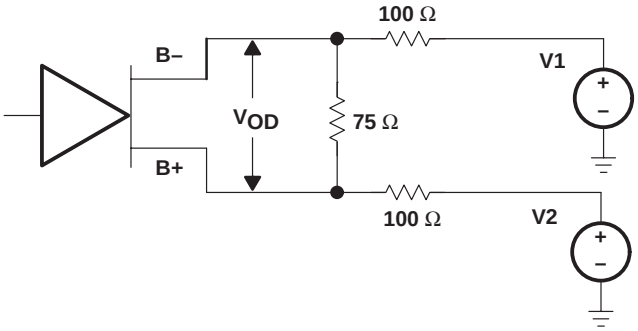


Figure 8. LVD-SCSI Driver Test Circuit

The voltage limits under the test-circuit conditions are derived to account for the worst case conditions that are allowed to exist on a standard compliant bus. The signal amplitudes ensure minimum input levels to a bus receiver while the maximums keep the bus voltages within the receiver's common-mode input voltage range. The additional constraint on the asserted output levels is driven by the need to maintain some measure of symmetry on the differential signal for first-step transition through the receiver input voltage threshold on heavily loaded buses. The relationship between $V_{(A)}$ and $V_{(N)}$ is shown graphically in Figure 9.

Table 7. LVD SCSI Driver Output Voltage Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(A)}$	Asserted differential output voltage	V1 = 0.96 V, V2 = 0.53 V	270		780	mV
			$0.69\|V_{OD}\|+50$		$1.45\|V_{OD}\|-65$	mV
		V1 = 1.95 V, V2 = 1.53 V	270		780	mV
			$0.69\|V_{OD}\|+50$		$1.45\|V_{OD}\|-65$	mV
$V_{(N)}$	Negated differential output voltage	V1 = 0.96 V, V2 = 0.53 V	–260		–640	mV
		V1 = 1.95 V, V2 = 1.53 V	–260		–640	mV

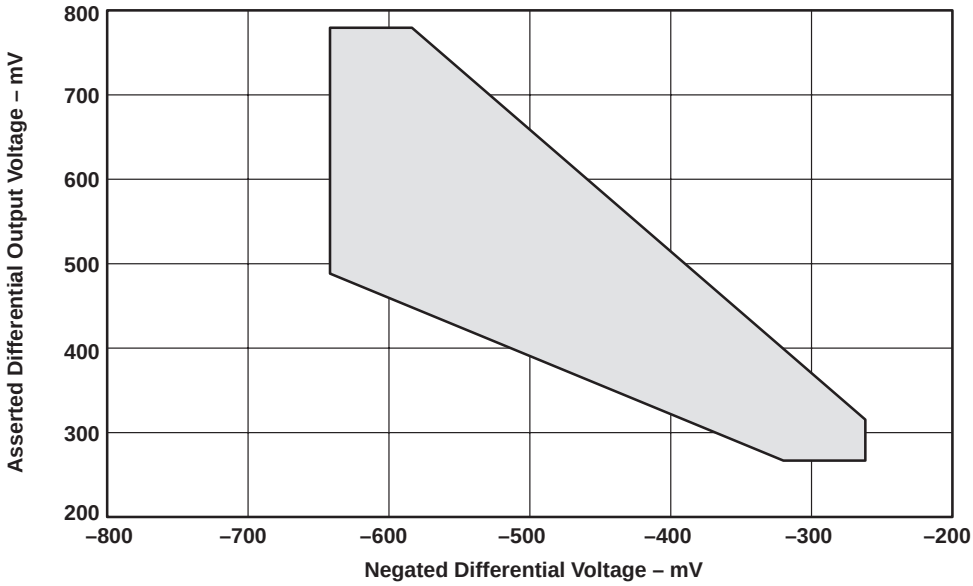


Figure 9. Relationship Between $V_{(A)}$ and $V_{(N)}$

There are numerous other electrical requirements on the driver and the reader is referred to the standard for further information.

Receivers –An LVD-SCSI receiver detects the logical state of the bus with as little as a 30 mV potential difference between the inputs of the signal pair. It also must do this over an input common-mode range of 0.7 V to 1.8 V. There is little room for any hysteresis, so any conditions that hover around the threshold could cause an oscillation at the output. To prevent this, LVD-SCSI uses a dc bias of 100 mV to 125 mV on the bus. This bias is provided by the termination.

SN75LVDM976 Dual-Mode Nine-Channel SCSI Transceiver

The SN75LVDM976 has nine transceivers for transmitting or receiving the signals to or from a SCSI data bus. It offers electrical compatibility to both the single-ended SCSI and LVD-SCSI. As might be deduced from the part number, it is also pin-compatible with the SN75976A HVD-SCSI transceiver to provide a common footprint for all three of the SCSI electrical layers.

The CDE0 input to the ’LVDM976 incorporates a window comparator to detect the status of the DIFFSENS line of a SCSI bus. This line is below 0.5 V if using single-ended signals, between 1.9 V and 2.4 V if low-voltage differential, and above 2.4 V if high-voltage differential. The outputs assume the characteristics of single-ended or LVD accordingly or place the outputs into high-impedance if HVD is detected.

Each of the nine channels has a direction control for selecting read or write operations. This necessitates that the protocol controller provide inputs to the enables. The ’LVDM976 also offers some common enables for the drivers in CDE1 and CDE2.

As described previously, the LVD-SCSI bus uses a dc bias on the line for wired-OR signaling and terminated failsafe protection. This and the need for minimization of the pulse skew from the driver requires that the driver be asymmetrical in its drive. In other words, the driver has to supply more current to the line during assertion than it does during negation of the bus. This means that logical inversion cannot be achieved simply by reversing the output pins of a symmetrical differential driver such as the ’976A. To accommodate differing controllers, an invert/noninvert control pin has been provided to select between active-high and active-low logic conventions.

Figure 10 is a laboratory setup of a 20-meter point-to-point connection of a ’LVDM976 driver and receiver.

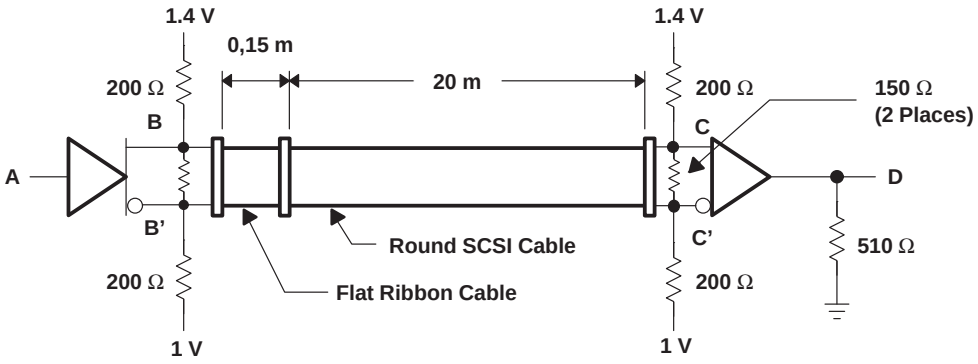


Figure 10. SN75LVDM976 LVD-Mode Signaling Example

Figure 11 shows the signals of an isolated 12 ns pulse being transmitted from the input to the driver (A) to the output of the receiver (B) with the intermediate points of the driver outputs (B and B’) and the receiver inputs (C and C’).

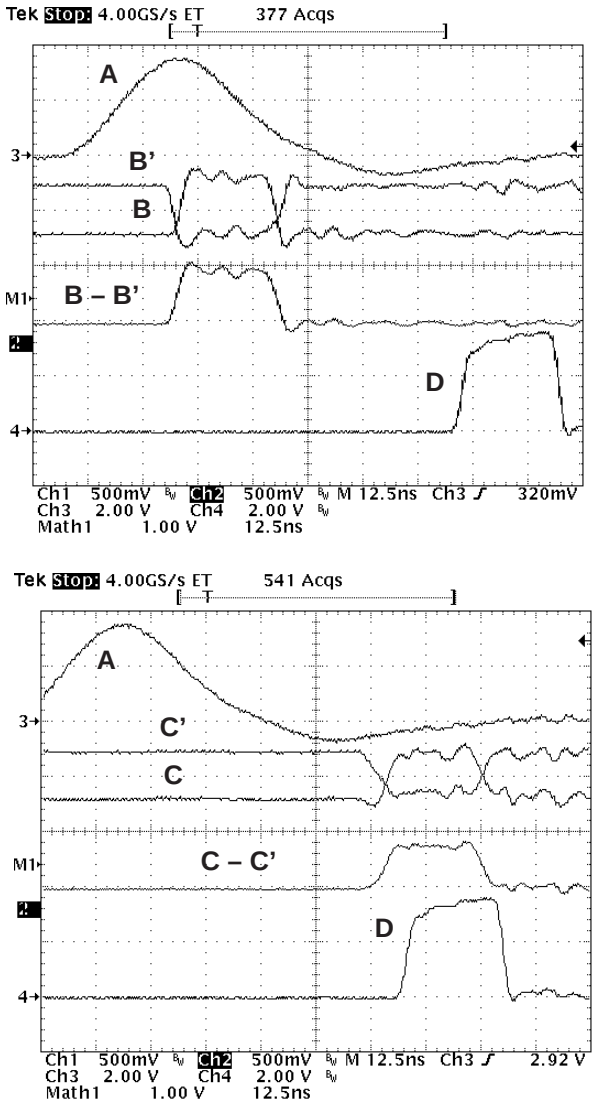


Figure 11. Typical LVD Signals