TEXAS INSTRUMENTS

Selection and Specification of Crystals for Texas Instruments IEEE 1394 Physical Layers

Application Report

2000

Mixed-Signal Products

SLLA051

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Contents

List of Figures

Selection and Specification of Crystals for Texas Instruments IEEE 1394 Physical Layers

Burke Henehan

ABSTRACT

To comply with the IEEE 1394 standard, each node in a 1394 bus must have a system clock of 49.152 MHz ±100 parts per million (ppm) (approximately 49.1471 MHz to 49.1569 MHz). For Texas Instruments (TI™) 1394 physical layers, this clock is derived from an external crystal with a frequency of 24.5760 MHz. An accurate clock requires careful selection and specification of the crystal used to supply the clock, along with the layout of the crystal circuit. This application report describes an appropriate specification for a crystal, and includes recommendations for layout and capacitor selection.

1 Introduction

TI physical layers (PHYs) may use an external 24.5760-MHz crystal connected between the XI and XO pins on the PHY to provide the PHY clock. The clock from the crystal input must be accurate within ±100 ppm for the PHYs to function correctly. This frequency tolerance—required by the IEEE 1394 standard for the PHY clocks on each node—must be maintained over variations introduced over production runs of boards and the environment in which the boards operate. Every board must have a system clock (SCLK generated by the PHY) within ±100 ppm of 49.152 MHz (49.1471 MHz to 49.1569 MHz) to comply with the 1394 standard. If adjacent nodes differ by more than 200 ppm (one 100 ppm, the other –100 ppm), long packets sent across the 1394 bus may be corrupted, with the final bits of the packet being lost, causing a packet data CRC error. TI PHYs are designed with maximum margins, but the 1394 limits must still be observed. The following are typical specifications for crystals used with TI physical layers, and some recommendations for implementation. Points discussed include:

a. Crystal frequency
b. Crystal mode of operation
c. Crystal circuit type
d. Frequency tolerance
e. Temperature tolerance
f. Aging
g. Load capacitance
h. Load capacitors tolerance
i. Maximum equivalent series resistance
j. Crystal and load capacitors layout
k. Testing

2 Crystal Frequency of Oscillation

The frequency of oscillation for the crystal should be specified as 24.5760 MHz.

2.1 Crystal Oscillation Mode

The oscillation mode of operation for the crystal should be specified as fundamental mode. This simplifies the resonant circuit that must be designed for the crystal.

2.2 Crystal Circuit Type

The type of circuit for the crystal should be specified as parallel resonance. This type of crystal is more precise and is needed to keep all nodes in a network to within ±100 ppm. The frequency of oscillation for parallel resonance crystal oscillator circuits is also dependent on the load capacitance presented to the crystal. See load capacitance below for more information.

2.3 Frequency Tolerance

Frequency tolerance is the maximum allowable deviation from nominal frequency at a specified temperature, usually 25°C. The tolerance of the crystal frequency over the manufacturing process should be specified at approximately ±30 ppm. The total tolerance from the crystal, the load capacitors, the capacitive load of the board, the capacitive load of the PHY pins, variation over temperature, variation with gain, and the circuitry of the PHY must be less than ±100 ppm. For this reason the total tolerance specified for the crystal must be less than 100 ppm. TI currently recommends a crystal frequency tolerance of ±30 ppm.

2.4 Temperature Tolerance

Temperature tolerance is the maximum allowable deviation, from the frequency at room temperature, over a specified temperature range. The tolerance of the crystal frequency over temperature should be approximately ±30 ppm. Again, the total tolerance from the crystal, the load capacitors, the capacitive load of the board, the capacitive load of the PHY pins, variation over temperature, variation with aging, and the circuitry of the PHY must be less than ±100 ppm. For this reason the tolerance specified for the crystal must be less than 100 ppm. TI currently recommends a crystal frequency tolerance of ±30 ppm.

2.5 Aging (Long-Term Stability or Drift)

Aging is the gradual change of a crystal's frequency of oscillation over time. There are many causes, including mass accumulation on the crystal due to contamination and stress relief or buildup on the mechanical structures around the quartz and the electrodes. Aging is typically specified as ppm per year value and so must be accounted for over the expected lifetime of the end equipment. The crystals used on TI lab test boards have an aging specification of ±5 ppm per year.

These values can be traded off, for example the frequency tolerance may be specified at ±40 ppm, the temperature may be specified at ±30 ppm, and aging specified at ±3 ppm per year to give a total of ±79 ppm possible variation just due to the crystal over three years.

2.6 Load Capacitance

For parallel resonant mode type circuits, the load capacitance specified for the crystal is very important since the frequency depends on the resonance of the circuit, including the load capacitors. However, the total load capacitance is not just the load capacitors, but will also be a function of the board layout and circuit. The total load capacitance (CL) will affect the frequency the crystal oscillates at. This means the load specified for the crystal includes the load capacitors (C9, C10), the loading of the PHY pins (Cphy), and the loading of the board itself (Cbd). See the schematic diagram in Figure 1.

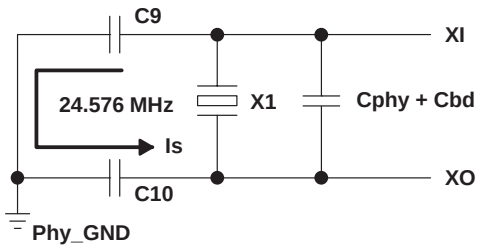

Figure 1. Crystal Equivalent Loading Schematic

To summarize: CL = [(C9×C10)/(C9+C10)] + Cphy + Cbd. Representative values for Cphy are ~1 pF and for Cbd are about 0.8 pF per centimeter of board etch, a typical board can have from 3 pF to 6 pF or more. The layouts of the TI evaluation module boards show approximately 4 pF to 5 pF of board and PHY capacitance. The capacitance of load capacitors C9 and C10 combine as capacitors in series. This means that variation on each capacitor only adds about one half to the total variation of the load capacitance. If the load capacitors were 22 pF ±5% and if both were exactly 22 pF the load they would present would be $(22 \times 22)/(22+22) = 11$ pF. If both were at the high limit:

$$[(22 \times 1.05) \times (22 \times 1.05)] / [(22 \times 1.05) + (22 \times 1.05)] = 11.55 \text{ pF}.$$

The difference, 11.55 – 11 = 0.55 pF is half of the 1.1 pF that is 5% of 22 pF. Since the value of any capacitor is a random draw, the values will tend to moderate one another, decreasing dependence on the variation introduced by the tolerance on the load capacitors. For this reason 5% tolerance capacitors should be sufficient.

An example plot of how the frequency of oscillation is influenced by the load capacitance is shown in Figure 2.

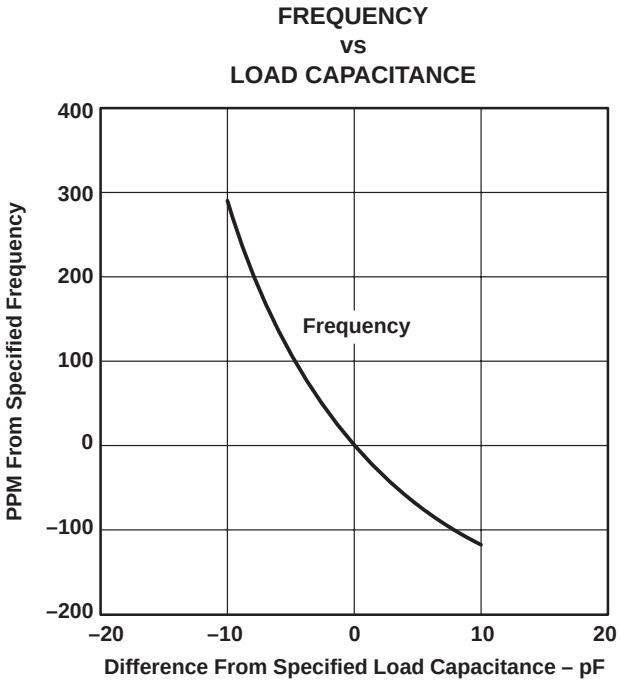

Figure 2. Crystal Frequency Dependence on Loading

In this idealized case, if the load capacitance is exactly what is specified for the crystal (difference = 0.0 pF), the unit oscillates at exactly the specified frequency (PPM = 0). Note that the curve is steeper when the capacitive load is lower than specified. However, another consideration is that if the load capacitance is too high or the series equivalent resistance is too high (see below) the oscillator within the PHY itself will not be able to drive the load and will not oscillate. For TI PHYs the load capacitance recommended is from 10 pF to 15 pF with lower values recommended, such as 10 or 12 pF. The crystal load should never be specified as more than 20 pF as this may be more than the oscillator inside the PHY can drive. If too large a value is used the oscillator may never start to oscillate or may oscillate at a very low frequency, outputting an SCLK of ~32 MHz.

2.7 Equivalent Series Resistance (ESR)

Crystals may be modeled by a series circuit of an inductor, a capacitor, and a resistor; along with a shunt capacitance in parallel with all three. The resistor is known as the equivalent series resistance. The equivalent series resistance is a figure of merit that is related to the loading the crystal and its resonance circuit present to the PHY oscillator pins. For the purposes of specification, a smaller maximum series resistance is better. For the TI PHY devices it is recommended that the maximum equivalent series resistance of a crystal specified for a loading of 15 pF should be less than 30 Ω. Lower capacitive load values should have lower maximum ESRs specified. The specified maximum ESR should never be more than 50 Ω.

2.8 Circuit Layout

The layout of the crystal portion of the PHY circuit is important for getting the correct frequency from the crystal, minimizing the noise introduced into the PHY phase lock loop, and minimizing any emissions from the circuit. The crystal and the two load capacitors should be considered a unit during layout. The crystal and the load capacitors should be placed as close as possible to one another while minimizing the loop area created by the combination of the three components. Using smaller size capacitors may help in making this unit more compact. Minimizing the loop area minimizes the effect of the resonant current (Is) that flows in this resonant circuit. This layout unit (crystal and load capacitors) should then be placed as close as possible to the PHY XI and XO pins to minimize etch lengths. The silkscreen outlines for the TI TSBKOHCI403 EVM crystal and load capacitors are shown on the left with the pad layouts for them shown on the right. This layout is an example; other layouts may be done following the above guidelines for even more compact layout with smaller loop areas.

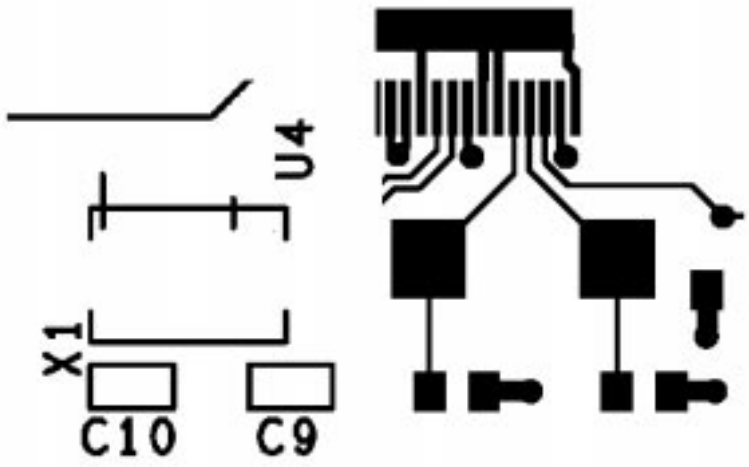

Figure 3. Example Crystal Layout

3 Summary

To summarize the recommendations:

- Crystal frequency: 24.5760 MHz
- Crystal mode of operation: fundamental
- Crystal circuit type: parallel resonance
- Frequency tolerance at 25°C: ≤ ±30 ppm
- Frequency stability over temperature: ≤ ±30 ppm
- Aging: ≤ ±5 ppm/year
- Load capacitance: [parallel (pF)]: 12 pF
- Load capacitors tolerance ≤ ±5%
- Maximum equivalent series resistance: ≤ 30 Ω
- Crystal and load capacitors placed as close as possible together as a unit
- Crystal and load capacitors unit placed as close as possible to PHY XI and XO pins
- Test the frequency of SCLK output from the PHY and iterate on the load capacitance to achieve a frequency within the tolerance specified for the crystal.

4 References

- *Specifying Crystals for use in VCXOs and TCXOs for Wireless Designs*, by James Northcutt on Fox Electronics web page: http://foxonline.com/tech3031.htm
- Document link labeled *In order to use a crystal unit* under *crystal units* link on KSS Kinseki web page (document in English): http://www.kinseki.co.jp/eng/product.html
- *Electronic Engineers' Handbook* by Donald G. Fink and Donald Christiansen, Sections 7 and 13.

5 Product Support

The following sources provide related product support information.

5.1 Related Documentation

Further information and data sheets can be obtained via the Internet at: http://www.ti.com/sc/1394.

Application reports can be obtained via the Internet at: http://www.ti.com/sc/docs/psheets/app msp.htm.

The following documents are available via links from the TI 1394 external web page:

- Data sheets for all TI 1394 devices
- Application notes for TI 1394 devices
- Errata list for all TI 1394 devices
- Information on designer kits

The IEEE 1394-1995 standard is available for purchase at: http://standards.ieee.org/catalog/index.html

5.2 World Wide Web

Our World Wide Web site at www.ti.com contains the most up to data product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new production updates automatically via email

The URL specifically for the TI 1394 external web site is http://www.ti.com/sc/1394. On this page, one can subscribe to 1394Times, which periodically updates subscribers on events, articles, products, and other news regarding 1394 developments.

5.3 Email

For technical issues or clarification on products, send a detailed email to: sc-infomaster@ti.com.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.