Application Report
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The MuxIt™ Data Transmission System: Applications, Examples, and Design Guidelines

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ABSTRACT

MuxIt is a family of general-purpose integrated-circuit building blocks, which was designed for implementing data transmission serializer-deserializer subsystems. This application report describes the types of applications in which MuxIt™ can be used, introduces the individual component devices, and provides guidelines for designing MuxIt systems. System design guidelines include PC board layout considerations, LVDS signal terminations, interface signal routing constraints, timing margins, and input-output bitmapping.

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1 MuxIt: What It Is

MuxIt is a family of general-purpose, integrated-circuit building blocks developed for data transmission serialization and deserialization subsystems. The MuxIt system allows for multi-bit parallel data to be transmitted through a reduced number of differential transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) interface. The number of bits combined or multiplexed per transmission-line link is user selectable, allowing for higher transmission efficiencies than available with fixed ratio solutions. MuxIt utilizes the low-voltage differential signaling (LVDS) technology defined by the TIA/EIA-644-A standard for communications between the data source and destination.

The MuxIt family initially includes three devices supporting simplex (one way) communications: the SN65LVDS150 phase locked loop (PLL) frequency multiplier, the SN65LVDS151 serializer-transmitter, and the SN65LVDS152 receiver-deserializer.

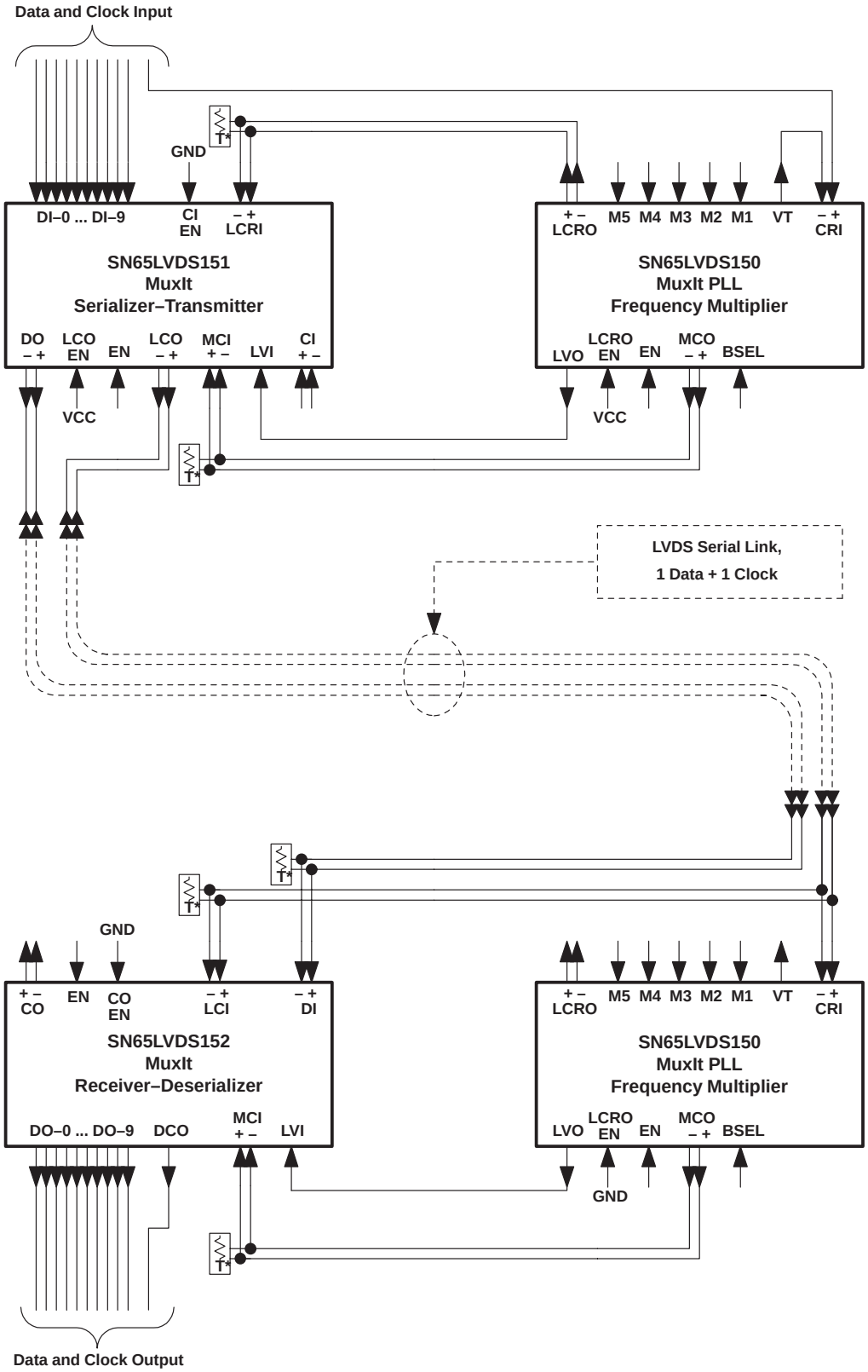


Figure 1. Basic MuxIt System

The simplest MuxIt implementation is illustrated in Figure 1. Between 4 and 10 bits of parallel source data are serialized by the SN65LVDS151 serializer-transmitter, and transmitted over a single high-speed LVDS transmission line link. The parallel data clock is used by the SN65LVDS150 PLL-frequency multiplier to generate the high-speed clock needed for transmitting the serialized data. The number of bits multiplexed onto the high-speed serial transmission line link is controlled by the frequency multiplication ratio set by the M1 through M5 control pins on the SN65LVDS150 PLL-frequency multiplier. A clock reference at the parallel data clock rate is also transmitted over an additional LVDS transmission line link.

At the destination end of the transmission line link, the high-speed serialized data and the clock reference are converted back to the original format of the parallel data and its related clock signal. The received clock reference signal is used to regenerate the high-speed clock in the SN65LVDS150 PLL-frequency multiplier. The frequency multiplication ratio is set to the same value as at the source end by using the same settings of the M1 through M5 control pins. The SN65LVDS152 receiver-deserializer shifts in the high-speed serial data in synchronization with the recovered high-speed clock and latches out the parallel data in synchronization with the clock reference.

Additional configurations, including multiplexing ratios up to 40, are examined in detail in this report.

2 MuxIt System Concept

2.1 A Simple 3-Step Process

The process of serializing, transmitting, and deserializing data can be divided into three steps.

2.1.1 Serialize the Parallel Input Data into a Higher-Speed Bit Stream

Parallel data is latched into the input registers of the serializer-transmitter in synchronization with the low-frequency data clock. That data is then loaded into the serial shift register after an additional count delay of the high-frequency multiplied clock. The high-frequency multiplied clock shifts the serial data through the shift register and into the LVDS output driver.

2.1.2 Transmit and Receive the Serialized Data Stream and Clock Reference

The serialized input data and the companion low-frequency data clock reference are transmitted from the source-end serializer-transmitter over LVDS transmission line links. These two signals are deskewed before transmission to improve system performance. At the destination end, the low-frequency data clock reference is multiplied to match the serial data frequency. The incoming serial data is clocked into the shift register of the destination-end receiver-deserializer.

2.1.3 Deserialize the Received Stream to Recover the Original Parallel Data and Clock

The received serial data is shifted through the receiver-deserializer shift register by the recovered multiplied clock. The serially-shifted data is then latched out in parallel to the output registers in synchronization with the low-frequency data clock reference after an additional count delay of the multiplied clock.

2.2 System Configuration Features and Flexibility

2.2.1 Number of Parallel Input-Output Bits

The serializer-transmitter and receiver-deserializer chips provide for up to ten bits of parallel data on their inputs and outputs respectively. Each of these devices may be connected in series (cascaded) with additional devices of the same type to support parallel data paths greater than ten bits. The diagram in Figure 2 illustrates how two shift registers in separate serializer-transmitter or receiver-deserializer chips are connected in series through the cascade I/O ports. The cascade connections increase the total length of the shift registers available for loading in or out parallel data. The actual number of bits used is determined by the multiplication or multiplexing ratio of the two clock signals that drive the chips. The PLL-frequency multiplier is recommended as the source for the two clocking signals because it maintains the proper timing relationship between them.

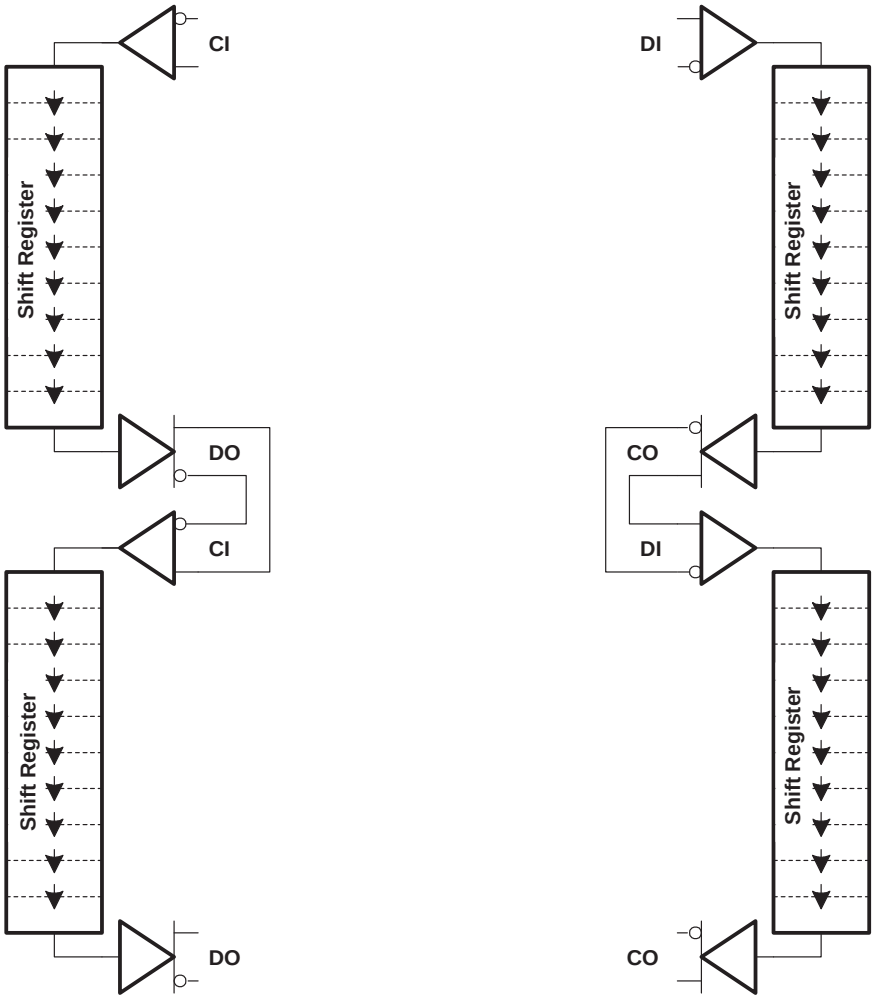


Figure 2. Cascade Connection of Shift Registers

2.2.2 Number of LVDS Transmission Line Links Used

The minimum basic configuration has two LVDS transmission line links, one for the serial data, and one for the clock reference. For higher aggregate bandwidth on the source-to-destination link, multiple serializers and deserializers may be operated in parallel from each clock-sourcing PLL chip. In these parallel-mode configurations, only the single (basic) clock reference line is needed. A single LVDS transmission line link can support up to 200 Mbps; multiple parallel transmission line links are specified to support 100 Mbps on each. Reducing the signalling rate by using multiple parallel transmission lines may be advantageous in allowing for greater transmission line lengths. Detailed information on the signaling rate and transmission line length tradeoffs can be found in *Performance of LVDS With Different Cables*, SLLA053.

2.2.3 Range of Parallel Bit-Multiplexing Ratios

The serializer-transmitter and receiver-deserializer chips are controlled by the two clocking signal inputs so they do not impose a limit on the number of parallel bits that may be multiplexed for serial transmission. The companion PLL-frequency multiplier chip is designed to support selected ratios between 4 and 40.

2.2.4 Simplex Point-to-Point or Simplex Multidrop Data Transmission

The serializer-transmitter and receiver-deserializer chips are designed for one-way (simplex) data transmission. This may be configured as a one-to-one (point-to-point) connection, or as a one-to-many (multidrop) configuration.

2.2.5 Wide PLL-Frequency Multiplier Data Clock Range

With a single chip and no external components, the PLL-frequency multiplier can operate with an input signal having a frequency between 5 MHz and 50 MHz. A band-select pin is used to control the internal circuit configuration, for minimum jitter, as a function of the frequency and multiplier ratio.

2.2.6 PLL-Frequency Multiplier Lock Indicator

An internal circuit in the PLL-frequency multiplier monitors the phase detector for a phase-locked condition during MuxIt system startup. This function provides the lock-valid-output (LVO) signal, which is used for enabling the serializer-transmitter and receiver-deserializer chips. Those chips have lock-valid-inputs (LVI) for this signal. While the LVI inputs are in a logic-low state, the LVDS link outputs from the SN65LVDS151, and the parallel data and clock outputs from the SN65LVDS162 are inhibited. This is done to prevent invalid data from being passed through or out of the MuxIt system until it has stabilized. After the LVI inputs have transitioned to a logic-high state the LVDS link and parallel data outputs are enabled. This signal is not intended to be used for any purpose other than inhibiting invalid data flow during system startup.

2.2.7 Link Clock and Link Data Synchronizer

The serializer-transmitter includes circuits on the LVDS output for skew reduction. This minimizes the time displacement between the serialized data and reference clock, improving system performance.

2.3 Determining the Link Topology

There are three key performance parameters that determine the link topology, i.e., the number of serial link data transmission lines required. They are:

- The number of parallel data bits, N_P
- The clock rate of the parallel data, R_P
- The maximum signaling rate supported by the serial links, R_L

The number of transmission lines that are required for the serial link is simply the rounded-up value of the aggregate bandwidth divided by the individual link transmission-rate capability:

$$N_L \geq \frac{N_P \times R_P}{R_L}$$

This relationship is shown in Figure 3. The plot is based on a serial link signaling-rate capability of 200 Mbps, which is limited to this value by the physical transmission line and connector system chosen, and by the capabilities of the high-speed portions of the serializer-transmitter and receiver-deserializer chips.

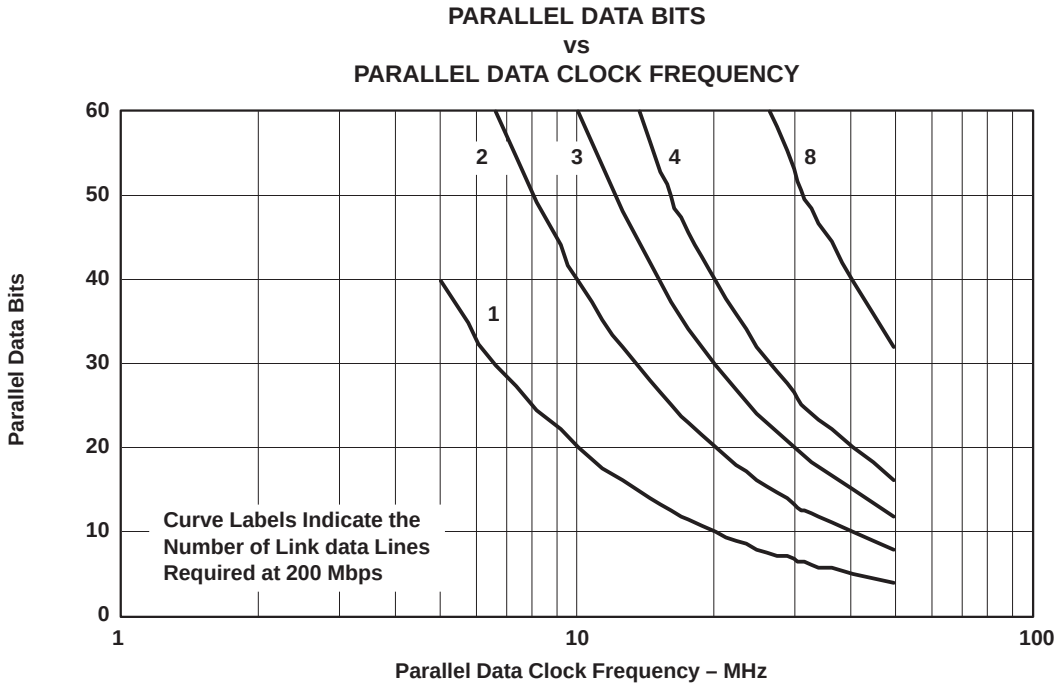


Figure 3. Link Data Rate—Parallel Data Bits vs Parallel Data Clock Frequency

The lower limit for the number of parallel data bits is determined by the SN65LVDS150 PLL-frequency multiplier minimum-multiplier-value of four. The minimum and maximum parallel data clock frequencies are determined by the SN65LVDS150 PLL frequency multiplier input frequency range of 5 MHz to 50 MHz.

2.4 Multidrop Topologies

A single source serializer can drive more than one destination deserializer system. This type of multidrop configuration must have only a single terminator on each of the link transmission lines, and that terminator must be located at the end furthest from the source. An example with two destination deserializer nodes is shown in Figure 4. For simplicity, this example shows only two nodes of the most basic 10-bit configuration—more complex nodes and a higher number of nodes are possible.

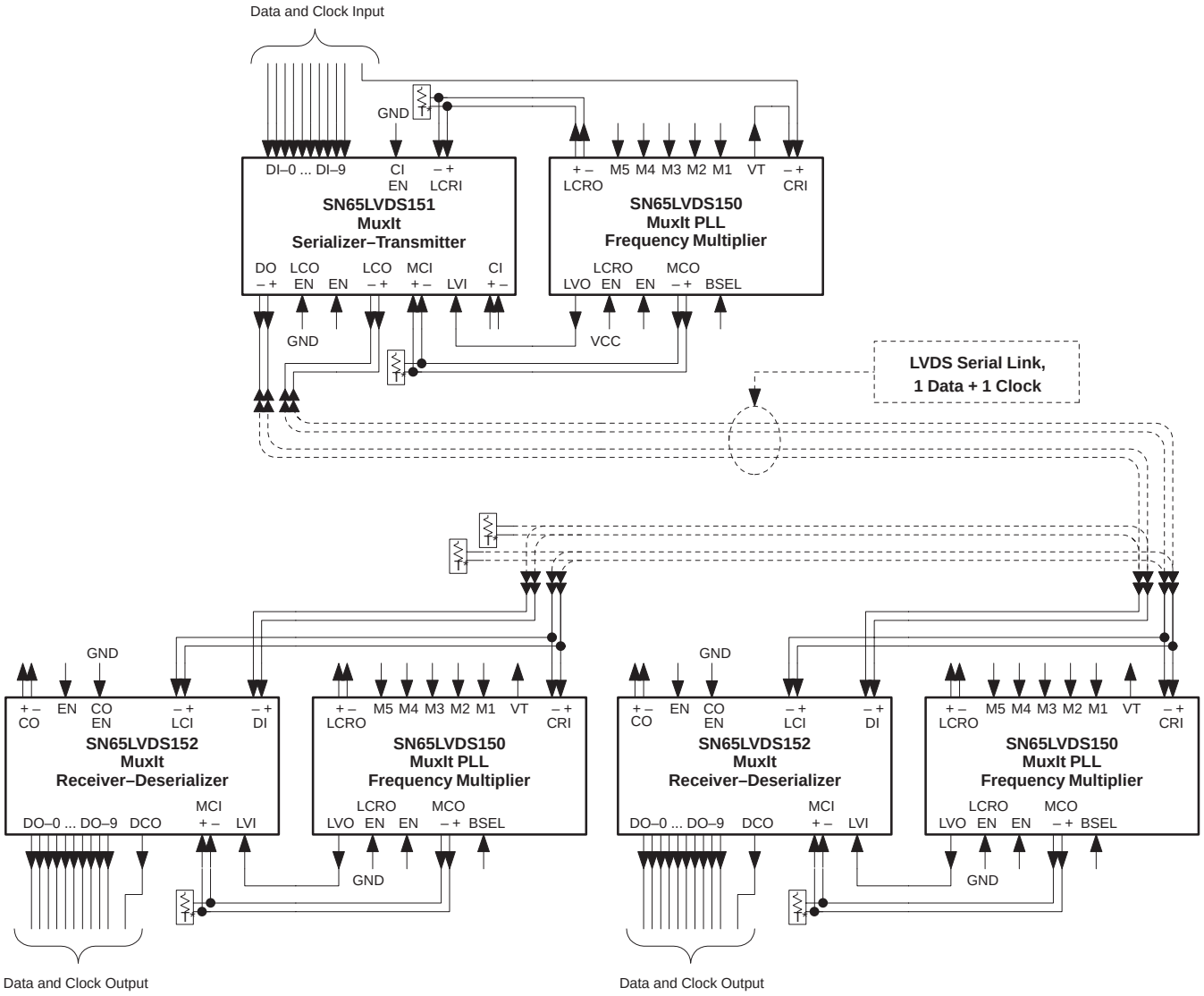


Figure 4. Illustrating a Multidrop Configuration of Receiver-Deserializers

3 MuxIt Family

3.1 The SN65LVDS150 PLL-Frequency Multiplier

The SN65LVDS150 is a PLL-based frequency multiplier designed for use with the serializer–transmitter and receiver-deserializer members of the MuxIt family. The frequency multiplication ratio is pin selectable over a wide range of values to accommodate a broad spectrum of user needs. Table 1 provides details on setting the multiplication ratio. No external filter components are needed. A PLL lock indicator output is use to inhibit link data transfers or parallel data output until the system has stabilized during startup.

The design of the SN65LVDS150 allows it to be used at both the transmit and receive ends of the MuxIt serial link. In Figure 5, the differential clock reference input (CRI) is driven by the system's parallel data clock when at the source end of the link, or by the link clock when at the destination end of the link. The differential CRI may be driven by either an LVDS-compatible differential signal, or by a single-ended clock of either polarity. For single-ended use, the non-clocked input is biased to the logic threshold voltage. For convenience, a $V_{CC}/2$ threshold reference, VT, is provided on a pin adjacent to the differential CRI pins for easier access when the input is used in a single-ended mode.

The multiplied clock output (MCO) is an LVDS-compatible differential signal used to drive the high-speed shift registers in either the SN65LVDS151 serializer-transmitter or the SN65LVDS152 receiver-deserializer. The link-clock-reference-output (LCRO) signal is an LVDS-compatible differential signal provided to the SN65LVDS151 serializer-transmitter for transmission over the link.

An internal power-on-reset and an enable-input (EN) control the operation of the SN65LVDS150. When V_{CC} is below 1.5 V, or when EN is low, the device is in a low power disabled state and the MCO and LCRO differential signals are in a high-impedance state. When V_{CC} is within the recommended operating range, and EN is high, the device and the two differential outputs are enabled and operating to specifications. The link-clock-reference-output-enable (LCRO_EN) input is used to turn off LCRO when it is not being used. A band-select input (BSEL) is used to optimize the VCO performance for minimum jitter as a function of which portion of the multiplied clock band of frequencies is being used: For multiplied clock frequencies below 100 MHz, BSEL should be tied low; at or above 100 MHz it should be tied high.

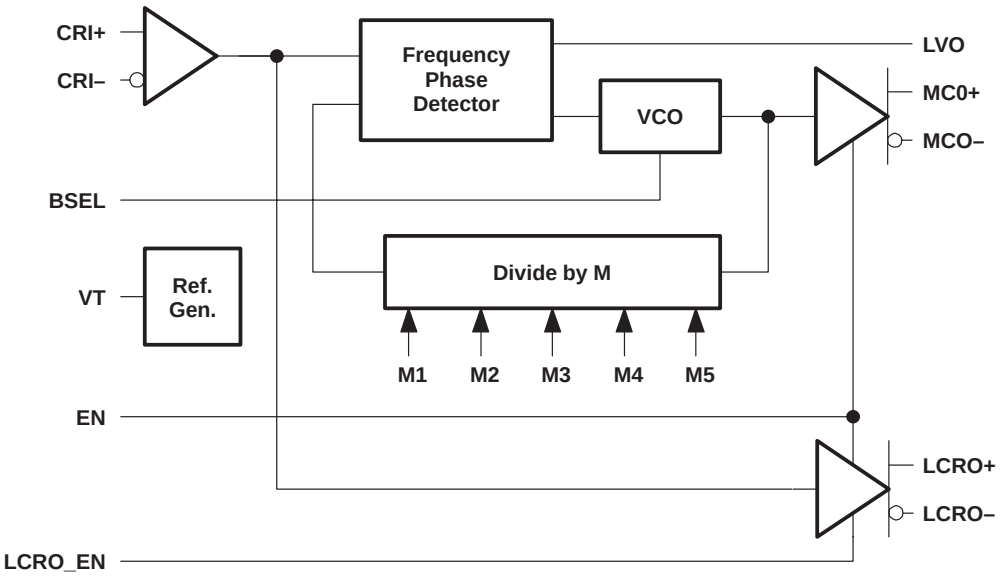


Figure 5. SN65LVDS150 PLL-Frequency Multiplier Block Diagram

Table 1. SN65LVDS150 PLL Frequency Multiplier Multiplication Ratio Settings

MULTIPLIER	M1	M2	M3	M4	M5	RECOMMENDED f_{IN} (MHz)	
						BSel = L	BSel = H
4	L	L	L	L	L	$f_{IN} < 12.50$	$12.50 \le f_{IN}$
†	L	L	L	L	H	NA	NA
6	L	L	L	H	L	$f_{IN} < 8.33$	$8.33 \le f_{IN}$
†	L	L	L	H	H	NA	NA
8	L	L	H	L	L	$f_{IN} < 12.50$	$12.50 \le f_{IN}$
9	L	L	H	L	H	$f_{IN} < 11.11$	$11.11 \le f_{IN}$
10	L	L	H	H	L	$f_{IN} < 10.00$	$10.00 \le f_{IN}$
†	L	L	H	H	H	NA	NA
12	L	H	L	L	L	$f_{IN} < 8.3$	$8.3 \le f_{IN}$
13	L	H	L	L	H	$f_{IN} < 7.7$	$7.7 \le f_{IN}$
14	L	H	L	H	L	$f_{IN} < 7.14$	$7.14 \le f_{IN}$
15	L	H	L	H	H	$f_{IN} < 6.67$	$6.67 \le f_{IN}$
16	L	H	H	L	L	$f_{IN} < 6.25$	$6.25 \le f_{IN}$
17	L	H	H	L	H	$f_{IN} < 5.88$	$5.88 \le f_{IN}$
18	L	H	H	H	L	$f_{IN} < 5.56$	$5.56 \le f_{IN}$
19	L	H	H	H	H	$f_{IN} < 5.26$	$5.26 \le f_{IN}$
20	H	L	L	L	L	$f_{IN} = 5.00$	$5.00 \le f_{IN}$
22	H	L	L	L	H	NA	$5.00 \le f_{IN}$
24	H	L	L	H	L	NA	$5.00 \le f_{IN}$
26	H	L	L	H	H	NA	$5.00 \le f_{IN}$
28	H	L	H	L	L	NA	$5.00 \le f_{IN}$
30	H	L	H	L	H	NA	$5.00 \le f_{IN}$
32	H	L	H	H	L	NA	$5.00 \le f_{IN}$
34	H	L	H	H	H	NA	$5.00 \le f_{IN}$
36	H	H	L	L	L	NA	$5.00 \le f_{IN}$
38	H	H	L	L	H	NA	$5.00 \le f_{IN}$
40	H	H	L	H	L	NA	$5.00 \le f_{IN}$
†	H	H	L	H	H	NA	NA
†	H	H	H	L	L	NA	NA
†	H	H	H	L	H	NA	NA
†	H	H	H	H	L	NA	NA
†	H	H	H	H	H	NA	NA

NOTE: L = Low-level logic input, H = High-level logic input, † = Reserved, NA = Not Applicable

Detailed specifications for the SN65LVDS150 can be found in *MuxIt PLL Frequency Multiplier*, SLLS443.

3.2 The SN65LVDS151 Serializer-Transmitter

The SN65LVDS151, shown in Figure 6, consists of a 10-bit parallel-in/serial-out shift register, a pair of LVDS differential transmission-line drivers, plus associated input and output buffers. It accepts up to 10 bits of user data on the parallel data inputs (DI−0 → DI−9) and serializes (multiplexes) the data for transmission over an LVDS transmission line link. Two or more SN65LVDS151 units can be connected in series, or cascaded, to accommodate wider parallel data paths for higher serialization values. The data is transmitted over the LVDS serial link at M times the input parallel data clock frequency. The multiplexing ratio, M, is selected on the companion SN65LVDS150 MuxIt PLL frequency multiplier with the configuration pins (M1 → M5) as detailed in Table 1.

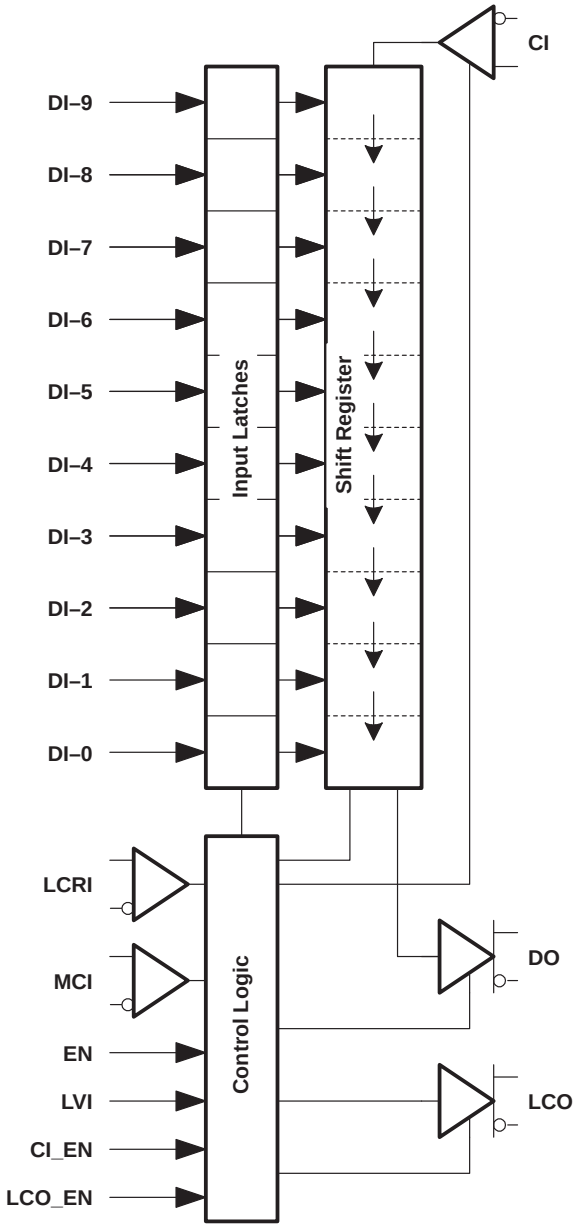


Figure 6. SN65LVDS151 Serializer-Transmitter Block Diagram

Data is parallel loaded into the SN65LVDS151 input latches on the first rising edge of the multiplied-clock-input (MCI) signal following a rising edge of the link-clock-reference input (LCRI). The data is read out serially from the SN65LVDS151 shift registers on the rising edges of the MCI signal. The lowest-order bit of parallel input data, DI−0, is output from DO on the third rising edge of the MCI signal following the rising edge of the LCRI signal. The remaining bits of parallel input data, DI−1 through DI−(M−1), are clocked out sequentially in ascending order by subsequent MCI-signal rising edges. The link-clock-output (LCO) signal's rising edge is synchronized to the data output (DO) by an internal deskewing circuit clocked by MCI. The LCO signal's rising edge follows the first rising edge of the MCI signal following the rising edge of LCRI. This operation is described in more detail in section 4.1 and is illustrated in Figure 8. Additional examples of operating waveforms for values of M of 4, 10, and 16 are provided in Figure 10 through Figure 12.

Both the LCRI and MCI signals are intended to be sourced by the SN65LVDS150 MuxIt PLL frequency multiplier. They are carried over LVDS differential connections to minimize skew and jitter. The SN65LVDS151 includes LVDS differential line drivers for both the serialized DO stream and the LCO signal. The cascade input (CI) is also an LVDS connection; when used, it is tied to the DO of the preceding SN65LVDS151.

An internal power-on-reset and an enable-input (EN) control the operation of the SN65LVDS151. When Vcc is below 1.5 V, or when EN is low, the device is in a low power disabled state and the DO and LCO differential outputs are in a high-impedance state. When V_{CC} is within the recommended operating range, and EN is high, the device and the two differential outputs are enabled and operating to specifications. The link-clock-output-enable-input (LCO_EN) is used to turn off the LCO output when it is not being used. The cascade-input-enable (CI_EN) is used to turn off the CI input when it is not being used.

Serialized data bits are output from DO in ascending order, starting with parallel input bit DI−0. The number of serialized data bits output per data clock cycle is determined by the multiplexing ratio, M. For values of M of 10 or less, the cascade input (CI±) is not used, and only the first M parallel input bits (DI−0 through DI−[M−1]) are used. For values of M greater than 10, all ten parallel input bits (DI−0 through DI−9) are used, and the cascade input is used to shift in the remaining data bits from additional SN65LVDS151 serializers. Table 2 shows which input data bits are used as a function of the multiplier M.

Table 2. SN65LVDS151 Serializer-Transmitter Bit Map

	M = 4	M = 6	M = 8	M = 9	M = 10	M >10
1st bit output	DI–0	DI–0	DI–0	DI–0	DI–0	DI–0
2nd bit output	DI–1	DI–1	DI–1	DI–1	DI–1	DI–1
3rd bit output	DI–2	DI–2	DI–2	DI–2	DI–2	DI–2
4th bit output	DI–3	DI–3	DI–3	DI–3	DI–3	DI–3
5th bit output	Invalid	DI–4	DI–4	DI–4	DI–4	DI–4
6th bit output	Invalid	DI–5	DI–5	DI–5	DI–5	DI–5
7th bit output	Invalid	Invalid	DI–6	DI–6	DI–6	DI–6
8th bit output	Invalid	Invalid	DI–7	DI–7	DI–7	DI–7
9th bit output	Invalid	Invalid	Invalid	DI–8	DI–8	DI–8
10th bit output	Invalid	Invalid	Invalid	Invalid	DI–9	DI–9
11th + bits output	Invalid	Invalid	Invalid	Invalid	Invalid	CI bits

Detailed specifications for the SN65LVDS151 are in *MuxIt Serializer–Transmitter*, SLLS444.

3.3 The SN65LVDS152 Receiver-Deserializer

The SN65LVDS152, shown in Figure 7, consists of three LVDS differential transmission line receivers, an LVDS differential transmission line driver, a 10-bit serial-in/parallel-out shift register, and associated input and output buffers. It receives serialized data over an LVDS transmission line link, deserializes (demultiplexes) it, and delivers it on the parallel data outputs, DO−0 through DO−9. The data received over the link is clocked in at a factor of M times the original parallel data frequency. The multiplexing ratio, M, is selected with the configuration pins (M1 → M5) on the companion SN65LVDS150 MuxIt PLL frequency multiplier, as detailed in Table 1. Up to 10 bits of data may be deserialized and output by each SN65LVDS152. Two or more SN65LVDS152 units may be connected in series, or cascaded, to accommodate higher values of M for wider parallel data paths.

Data is serially shifted into the SN65LVDS152 shift registers on the falling edges of the MCI signal. The data is latched out in parallel from the SN65LVDS152 shift registers on the rising edges of the LCI signal. The SN65LVDS152 includes LVDS differential line receivers for the serialized link data stream (DI), the LCI signal, and the high-speed MCI signal. The output for cascaded data (CO) is carried over an LVDS differential connection to minimize skew and jitter. This operation is described in more detail in section 4.2 and is illustrated in Figure 9. Additional examples of operating waveforms for M-values of 4, 10, and 16 are provided in Figure 10 through Figure 12.

The EN input, along with the power-on-reset, controls the outputs. When V_{CC} is below 1.5 V, or when EN is low, the outputs are disabled. When V_{CC} is within the recommended operating range, and EN is high, the outputs are enabled and operating to specifications.

Parallel data bits are output from the DO-n outputs in an order that is dependent on the value of the multiplexing ratio (frequency multiplier value) M. For values of M equal to 10 or less, the cascade output (CO±) is not used, and only the higher-order M parallel outputs (DO−9 through DO−[10−M]) are used. The data bit output on DO−9 corresponds to the data bit input on DI−[M−1] of the SN65LVDS151 serializer. Likewise, the data bit output on DO−[10−M] corresponds to the data bit input on DI−0 of the SN65LVDS151 serializer.

For values of M greater than 10, the cascade output (CO±) of one (higher-ordered) SN65LVDS152 is connected the DI input of an additional SN65LVDS152 deserializer. Two or more SN65LVDS152 units may be cascaded in this fashion for parallel bit counts of 12 through 20, or higher. The parallel bit limit is set by the frequency multiplication ratio, M, which has a maximum of 40 for the SN65LVDS150. In these cascade configurations, the higher-order unit(s) each output 10 of the highest-numbered bits that were input into the SN65LVDS151 serializer(s). The lowest–numbered input bits are output on the lowest-order SN65LVDS152 deserializer in descending order from output DO−9. The number of bits is equal to M mod(10). This information is shown in Table 3, where X designates M mod(10).

Table 3. SN65LVDS152 Receiver-Deserializer Bit Map

	X = 2	X = 3†	X = 4	X = 5†	X = 6	X = 7†	X = 8	X = 9†	X = 0
DO–9 output bit	DI–1	DI–2	DI–3	DI–4	DI–5	DI–6	DI–7	DI–8	DI–9
DO–8 output bit	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5	DI–6	DI–7	DI–8
DO–7 output bit	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5	DI–6	DI–7
DO–6 output bit	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5	DI–6
DO–5 output bit	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4	DI–5
DO–4 output bit	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3	DI–4
DO–3 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2	DI–3
DO–2 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1	DI–2
DO–1 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0	DI–1
DO–0 output bit	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI–0

† Applicable only for values of M between 13 and 19.

Detailed specifications for the SN65LVDS152 are in *MuxIt Receiver-Deserializer*, SLLS445.

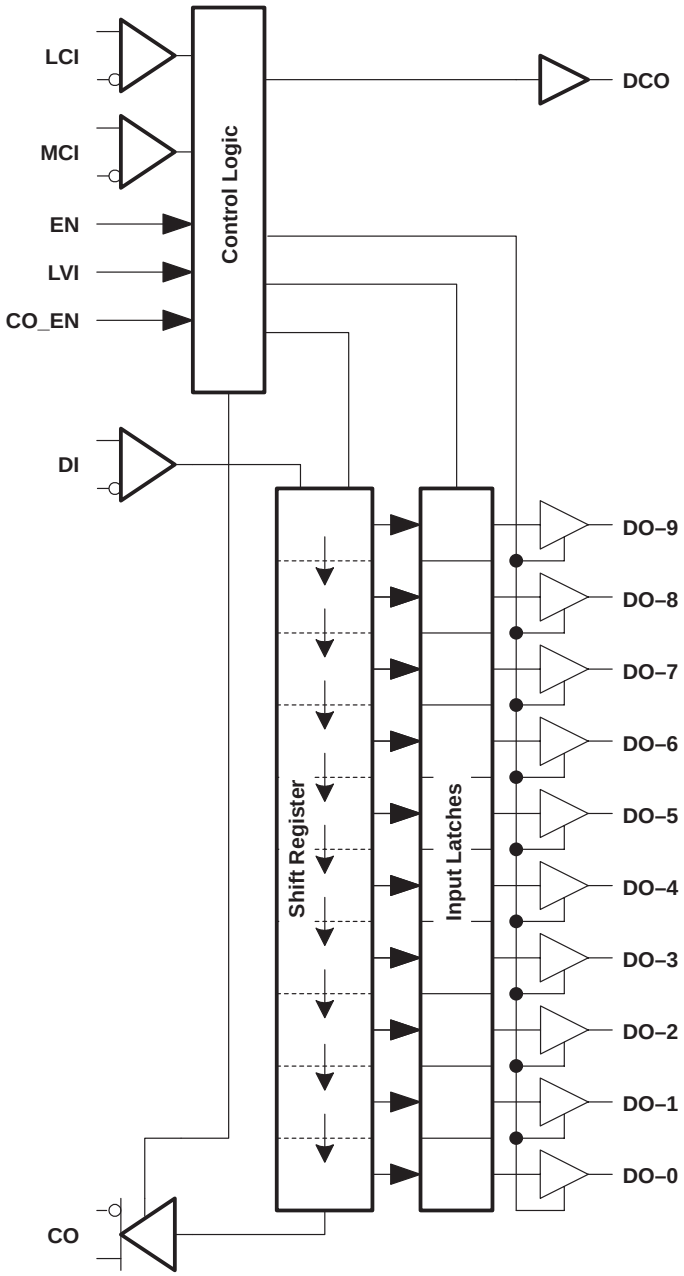


Figure 7. SN65LVDS152 Receiver-Deserializer Block Diagram

4 MuxIt-System Operating-Waveform Examples

This section provides a step-by-step walk-through of the operation and the resulting signal waveforms of a MuxIt data-transmission system. The example is based on a system having a frequency multiplication (or data multiplexing) ratio of M = 6. It uses an SN65LVDS150 PLL-frequency multiplier plus a single SN65LVDS151 serializer-transmitter chip at the source-end of the data-transmission system. An SN65LVDS150 PLL-frequency multiplier plus a single SN65LVDS152 receiver-deserializer is used at the destination end.

4.1 Source-End Operating Waveforms

The following steps are in reference to Figure 8 and illustrate the essential operating steps and signal relationships in a MuxIt source-end serializer system.

S1. Parallel data is clocked out of a source device on one edge of the data clock—in this example the falling edge. The rising edge of the data clock occurs approximately in the middle of the time interval during which the parallel data is valid. Note that reversing the connections to the CRI terminals of the SN65LVDS150 allows a data clock of the opposite polarity to be used.

S2. The rising edge of the data clock is used as the reference for the SN65LVDS 150 PLL frequency multiplier to generate the multiplied clock. The multiplied clock is applied to the SN65LVDS151 as the MCI signal.

S3. The rising edge of the data clock is also buffered, and delayed relative to the multiplied clock, by an internal repeater function in the SN65LVDS150. This signal is applied to the SN65LVDS151 as the link-clock-reference-input (LCRI) signal.

S4. Data is latched into the input registers of the SN65LVDS151 on the first rising edge of the MCI signal that follows the rising edge of the LCRI signal. The specifications of the SN65LVDS150 guarantee that the LCRI-to-MCI setup time requirement of the SN65LVDS151 is met.

S5. Data bits from the SN65LVDS151 input registers are clocked into the shift register on the third rising edge of MCI signal that follows the rising edge of the LCRI signal.

S6. Data bits are clocked out from the SN65LVDS151 shift register to the LVDS data output (DO) beginning with the third rising edge of MCI signal that follows the rising edge of the LCRI signal.

S7. The LCO signal is a delayed LCRI signal that is clocked out on a rising edge of the MCI input signal. This is done to deskew the two signals LCO and DO.

S8. The DO serial output bits are clocked out on rising edges of the MCI signal. This is done to deskew on two signals LCO and DO.

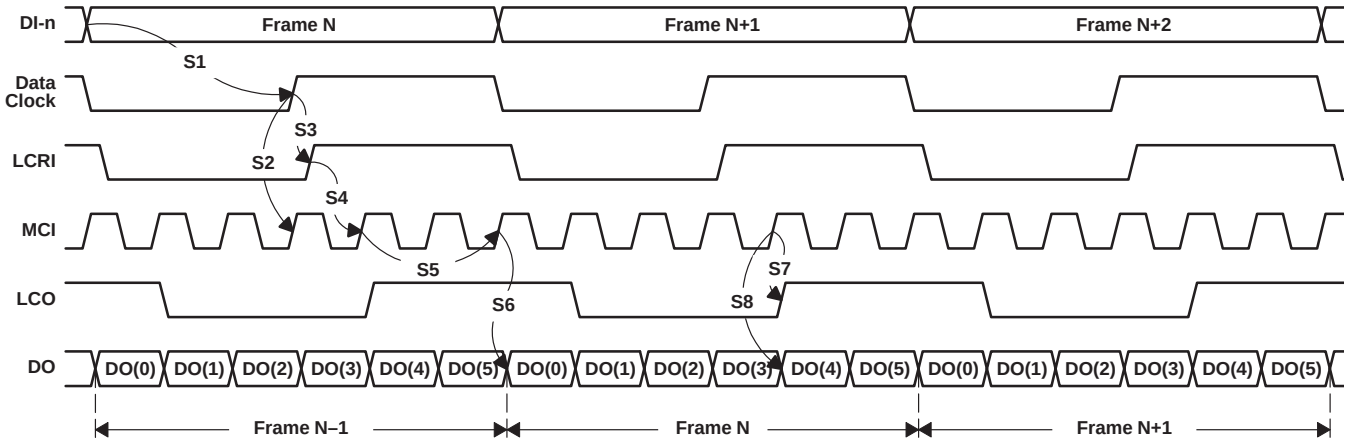


Figure 8. Operating Waveforms of a Source-End Serializer-Transmitter With M = 6

4.2 Destination-End Operating Waveforms

The following steps are in reference to Figure 9 and illustrate the essential operations and signal relationships in a MuxIt destination-end deserializer.

D1. Rising edges of the incoming link clock signal are used by the SN65LVDS150 PLL-frequency multiplier to reconstruct the high-speed multiplied clock signal. This is applied to the SN65LVDS152 receiver-deserializer as the multiplied clock input.

D2. High-speed incoming serial data bits are clocked into the SN65LVDS152 on the falling edges of the MCI signal.

D3. As a result of the deskewing function in the SN65LVDS151 serializer-transmitter, the rising edges of the incoming link clock signal are in synchronization with the transitions of the incoming serial data (DI).

D4. The first falling edge of the MCI signal that follows the rising edge of the LCI signal initiates an internal counter for synchronizing the parallel output data frame.

D5. The second falling edge of the MCI signal after the rising edge of the LCI signal clocks in the last serial bit in the data frame.

D6. The MCI signal's rising edge that follows two MCI falling edges after the rising edge of the LCI signal is used to latch out the parallel data frame.

D7. The data clock output, DCO, is used to indicate a valid parallel output data frame. It is a delayed LCI signal.

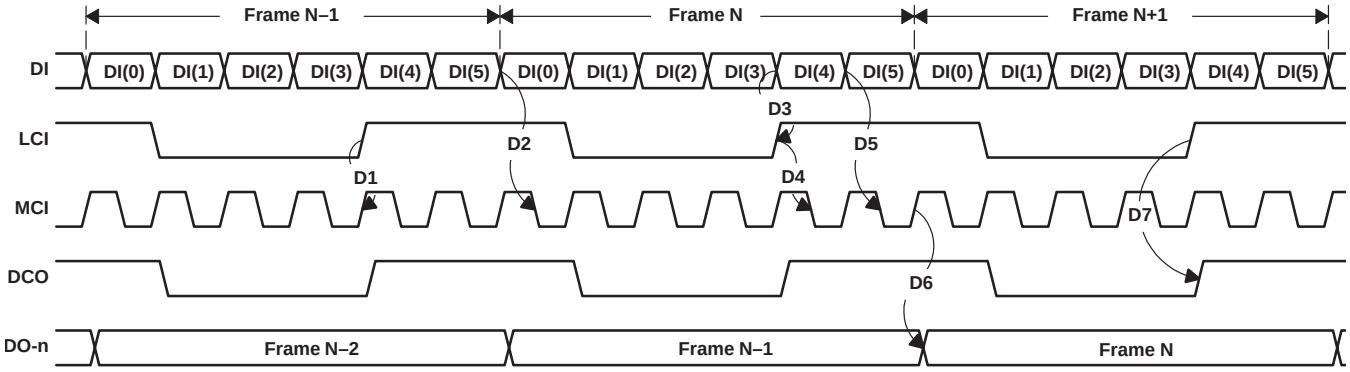


Figure 9. Operating Waveforms of a Destination-End Receiver-Deserializer With M = 6

4.3 Additional Waveform Examples

Figure 10 through Figure 12 shows additional examples of source and destination system waveforms for M = 4, 10, and 16, respectively.

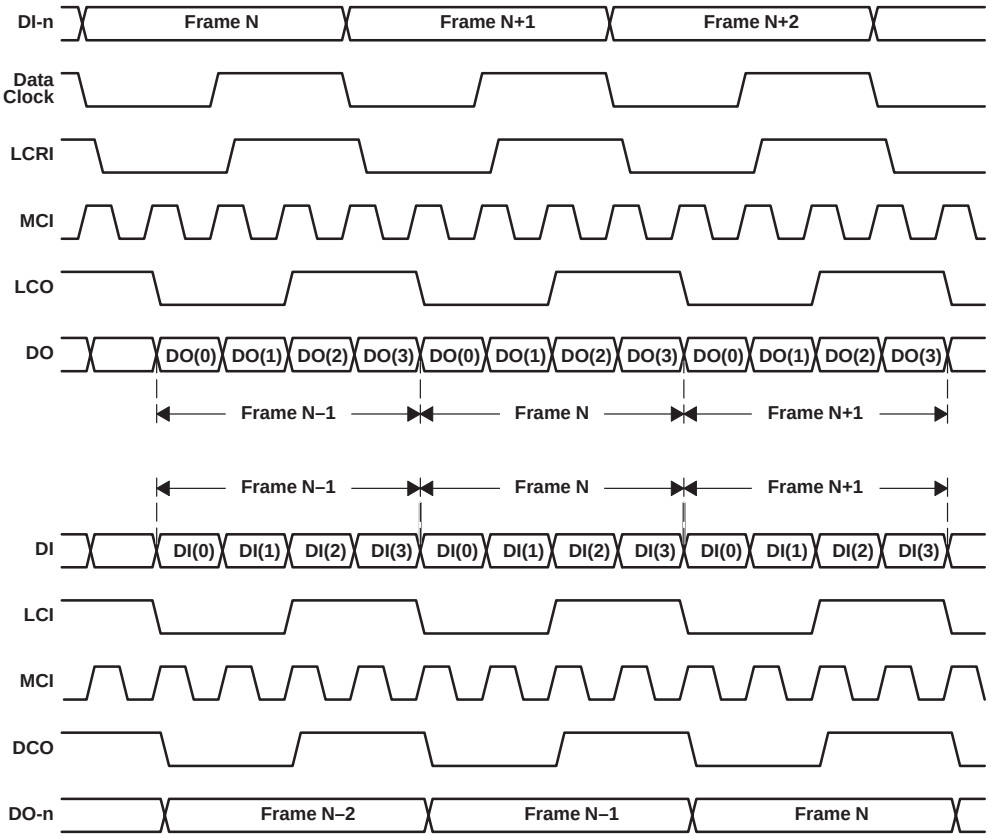


Figure 10. Serializer-Transmitter and Receiver-Deserializer Operating Waveforms for M = 4

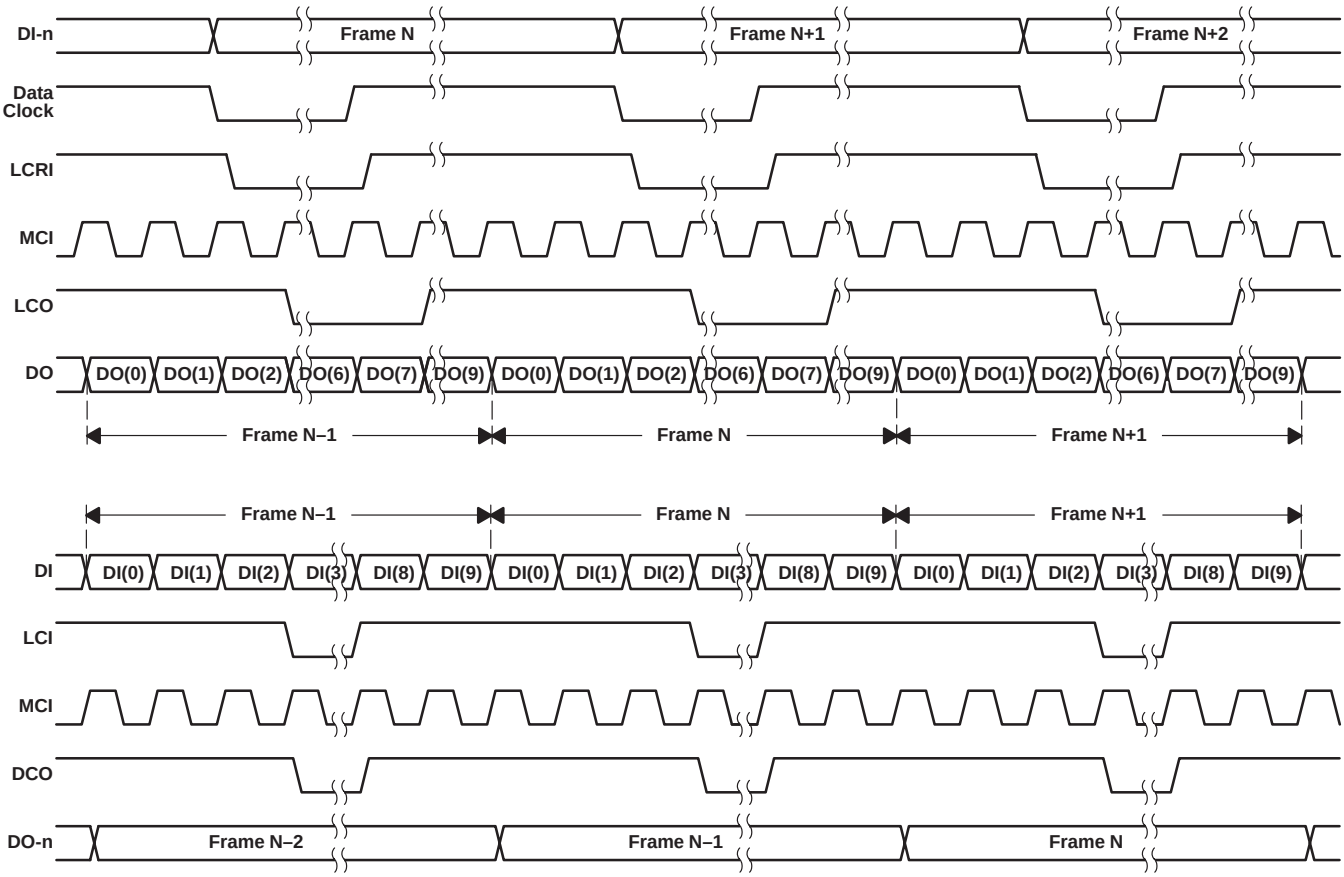


Figure 11. Serializer-Transmitter and Receiver-Deserializer Operating Waveforms for M = 10

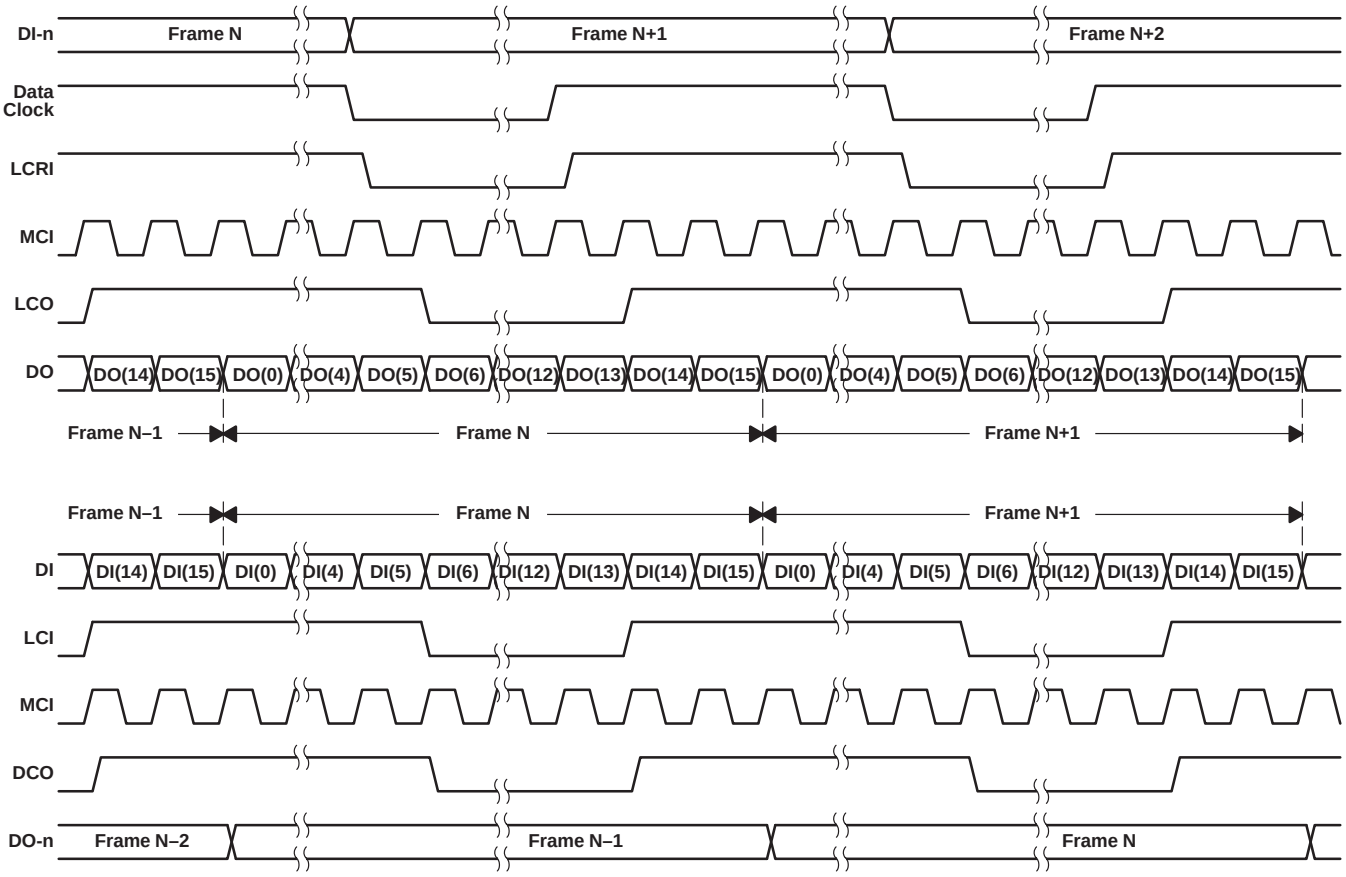


Figure 12. Serializer-Transmitter and Receiver-Deserializer Operating Waveforms for M = 16

5 MuxIt Layout Considerations

The LVDS signals routed between the MuxIt chips require special care during PC board layout. In general, the MuxIt chips must be located as close as possible to each other to minimize the signal propagation delays and skews between them. Termination resistors must be supplied for all LVDS lines, except for the CI input of the SN65LVDS151. Additional MuxIt-specific details are provided in the following. For general PCB layout guidelines, *Low-Voltage Differential Signaling (LVDS) Design Notes*, Texas Instruments literature number SLLA014.

5.1 PC-Board LVDS Trace Matching

There are several important signal-timing constraints that need to be observed for correct operation of the MuxIt system. These fall into two categories: (i) the chip-to-chip interface at the source and destination ends of the link, and (ii) the source-to-destination interface. These topics are addressed in order, and a number of implementation examples are provided. The configuration flexibility of the MuxIt system makes it difficult to cover every possible implementation, but this information covers the majority of applications.

Dynamic operation of source-end SN65LVDS151 serializer-transmitter functions are controlled by the multiplied-clock-input (MCI), and the link-clock-reference-input (LCRI) signals. The SN65LVDS150 PLL-frequency multiplier ensures the proper timing relationship between these two signals when it is used as their source.

The propagation delay of the signal path from the LCRO output on the SN65LVDS150 to the LCRI input on the SN65LVDS151 must match the propagation delay of the signal path from the MCO output on the SN65LVDS150 to the MCI input of the SN65LVDS151. This is illustrated in Figure 13 through Figure 17 by the equal-length constraints on LS1 and LS2. Length, rather than time, is being used in these examples because it relates more practically to board layouts than time constraints. It is also noted that the diagrams in these figures are not to scale, nor do they represent actual routing paths. An example of an actual layout for the LVDS interconnect traces, extracted from a PC-board plot file, is shown in Figure 18.

Additionally, it is important to maintain the timing relationship between these two signals in configurations that have multiple SN65LVDS151 devices. This means that the incremental delays between successive SN65LVDS151 serializer–transmitter units must be matched to limit skew between these two signals. This is illustrated for configurations with two SN65LVDS151 serializer–transmitter units in Figure 13 through Figure 16 by the equal-length constraints on LS3 and LS4. Figure 17 illustrates this principle extended to a triple SN65LVDS151 serializer-transmitter configuration with the addition of an equal-length constraint on LS5 and LS6.

At the destination end of the link, the dynamic operation of the SN65LVDS152 receiver-deserializer is controlled by the MCI and LCI signals.

The propagation delay of the signal path to the LCI input on the SN65LVDS152 must match the sum of the propagation delays to the SN65LVDS150 CRI input and the propagation delay from the MCO output of the SN65LVDS150 to the MCI input of the SN65LVDS152. In this case the link-clock-signal propagation delays are being referenced to the link interface connector point before the signals split between the SN65LVDS150 and the SN65LVDS152. This is illustrated in Figure 13 through Figure 17 by the equal-length constraints on LD0, LD1 and LD2. Again, lengths rather than times are used in these examples because they relate more practically to PCB layout.

As with the source end of the link, it is important to maintain the timing relationship between signals in configurations that have multiple SN65LVDS152 devices. The incremental delays between successive SN65LVDS152 receiver-deserializer unit signals must be matched to limit skew between them. This is illustrated for configurations with two SN65LVDS152 receiver-deserializer units in Figure 13 through Figure 16 by the equal-length constraints on LD3 and LD4. Figure 17 illustrates this principle extended to a triple SN65LVDS152 receiver-deserializer configuration with the addition of an equal-length constraint on LD5 and LD6.

The source-to-destination link interface timing constraints are described here using two somewhat different approaches, referred to here as *compensated* and *noncompensated* LVDS link line lengths, respectively. The compensated configurations shown in Figure 13 and Figure 14 have signals at the link interfaces that are in phase with each other. The noncompensated configurations shown in Figure 15 and Figure 16 have signals at the link interface that are skewed in time with respect to each other. The noncompensated configuration introduces additional end-to-end, or side-to-side, matching requirements so that the chip-to-chip skews introduced at the source match the chip-to-chip skews at the destination. The choice of configuration is discretionary because both work. With the exception of Figure 15 and Figure 16 all the examples in this report are of the compensated variety.

The compensated configuration is probably an easier choice for cable-connected systems where all the signals run though a single multipin connector. The noncompensated configuration is appropriate for backplane systems where the LVDS signal pairs are not on adjacent connector pins or backplane traces.

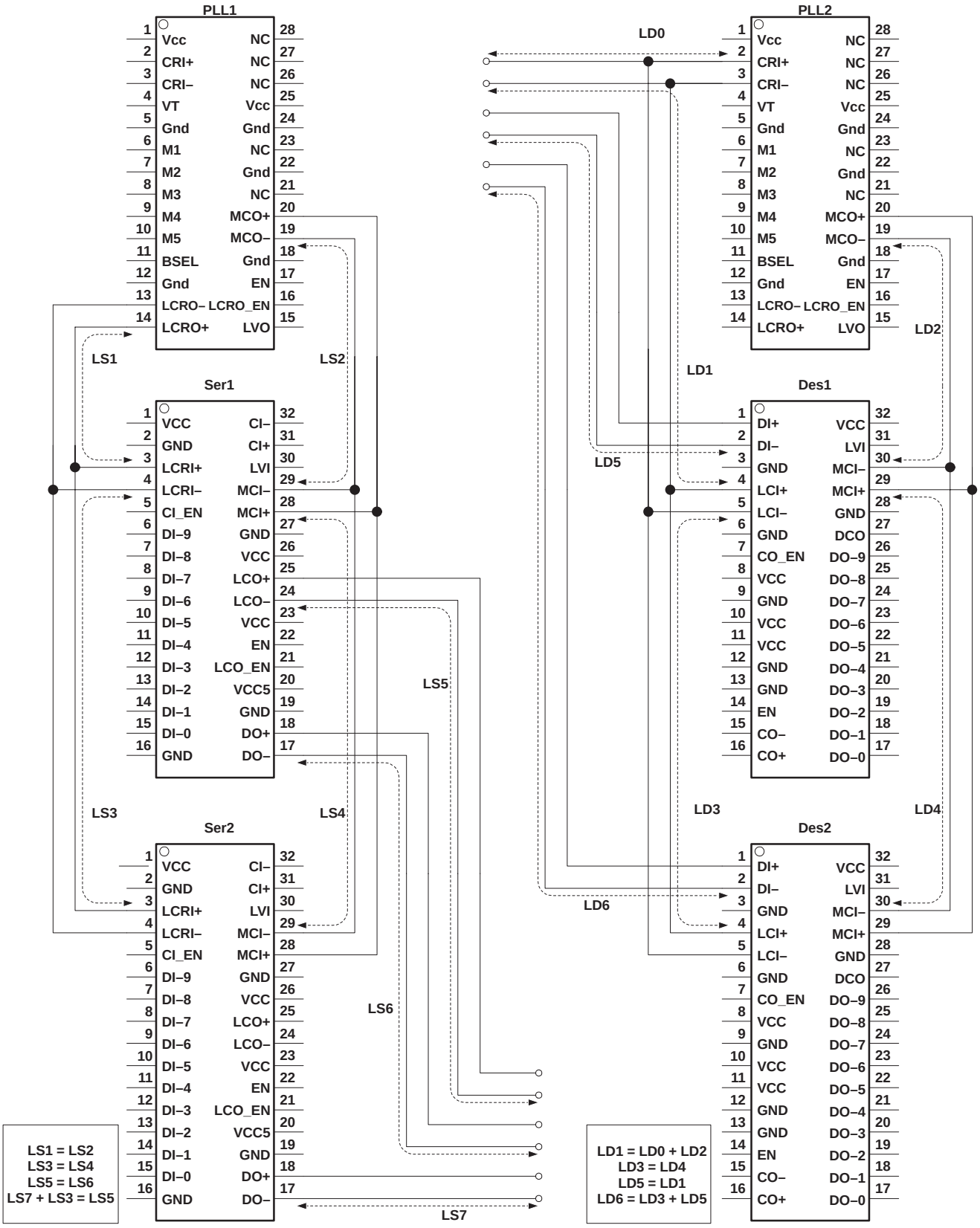


Figure 13. Parallel-Mode Configuration With Compensated LVDS Transmission Line Lengths

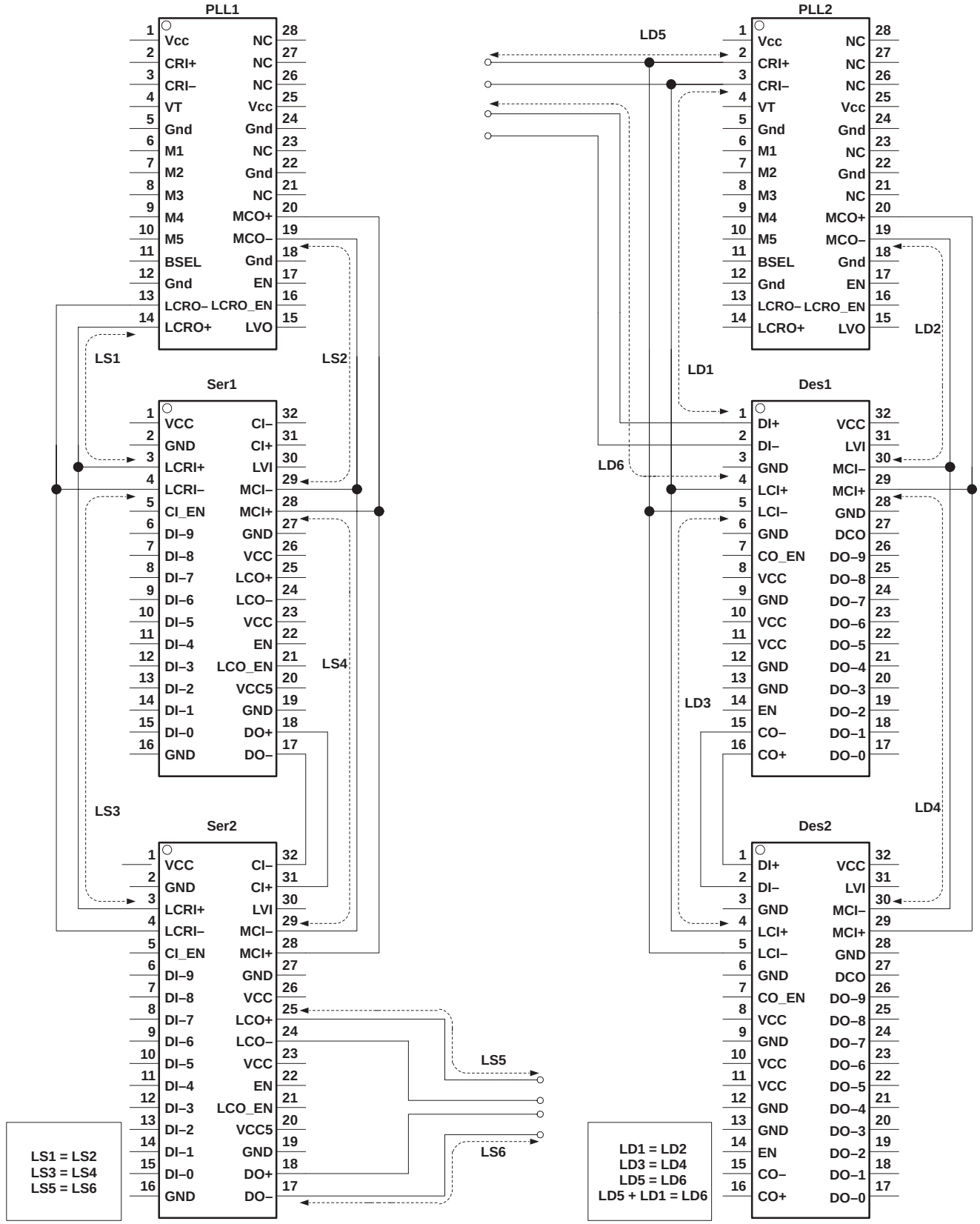


Figure 14. Cascade-Mode Configuration With Compensated LVDS Transmission Line Lengths

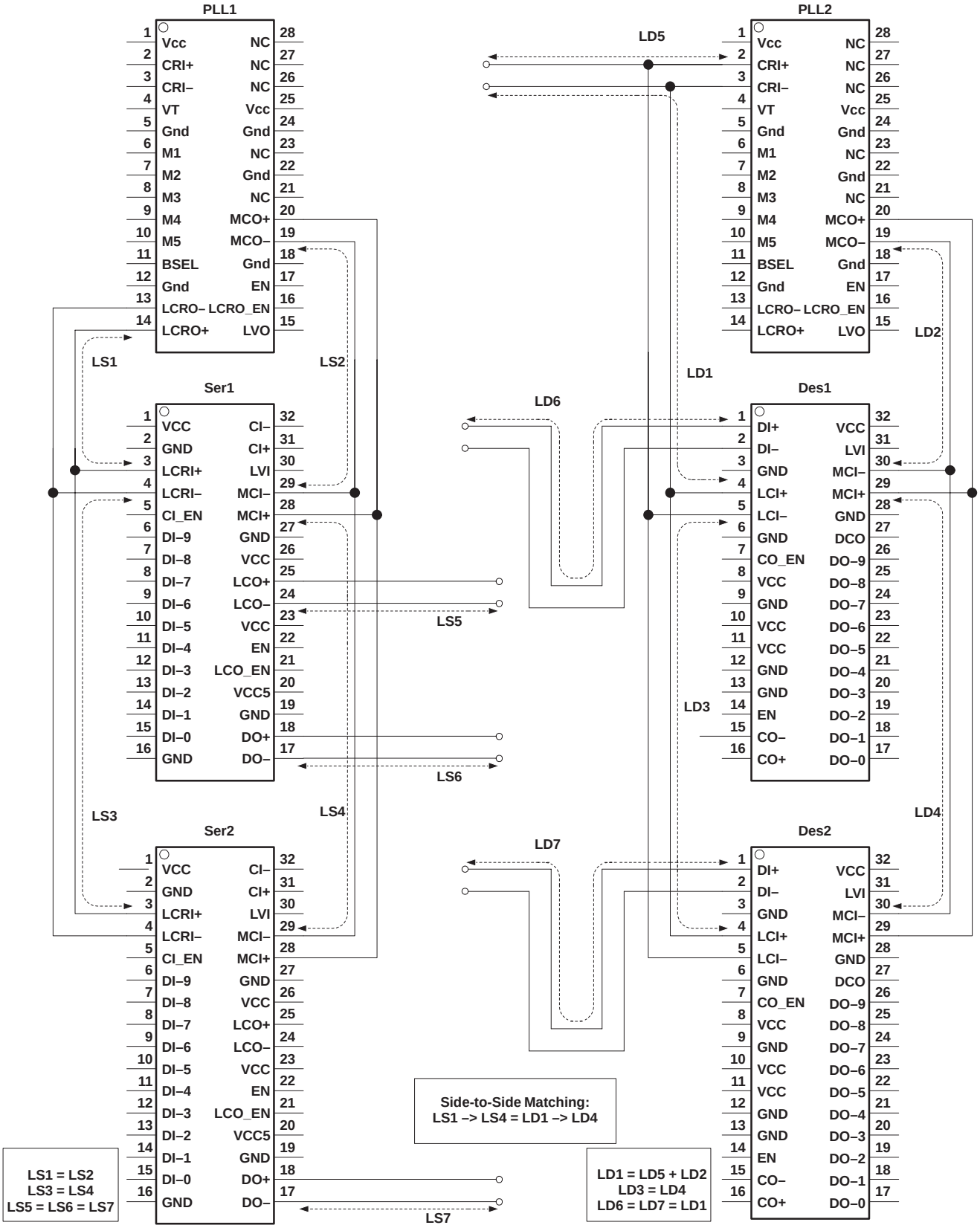


Figure 15. Parallel-Mode Configuration With Noncompensated LVDS Transmission Line Lengths

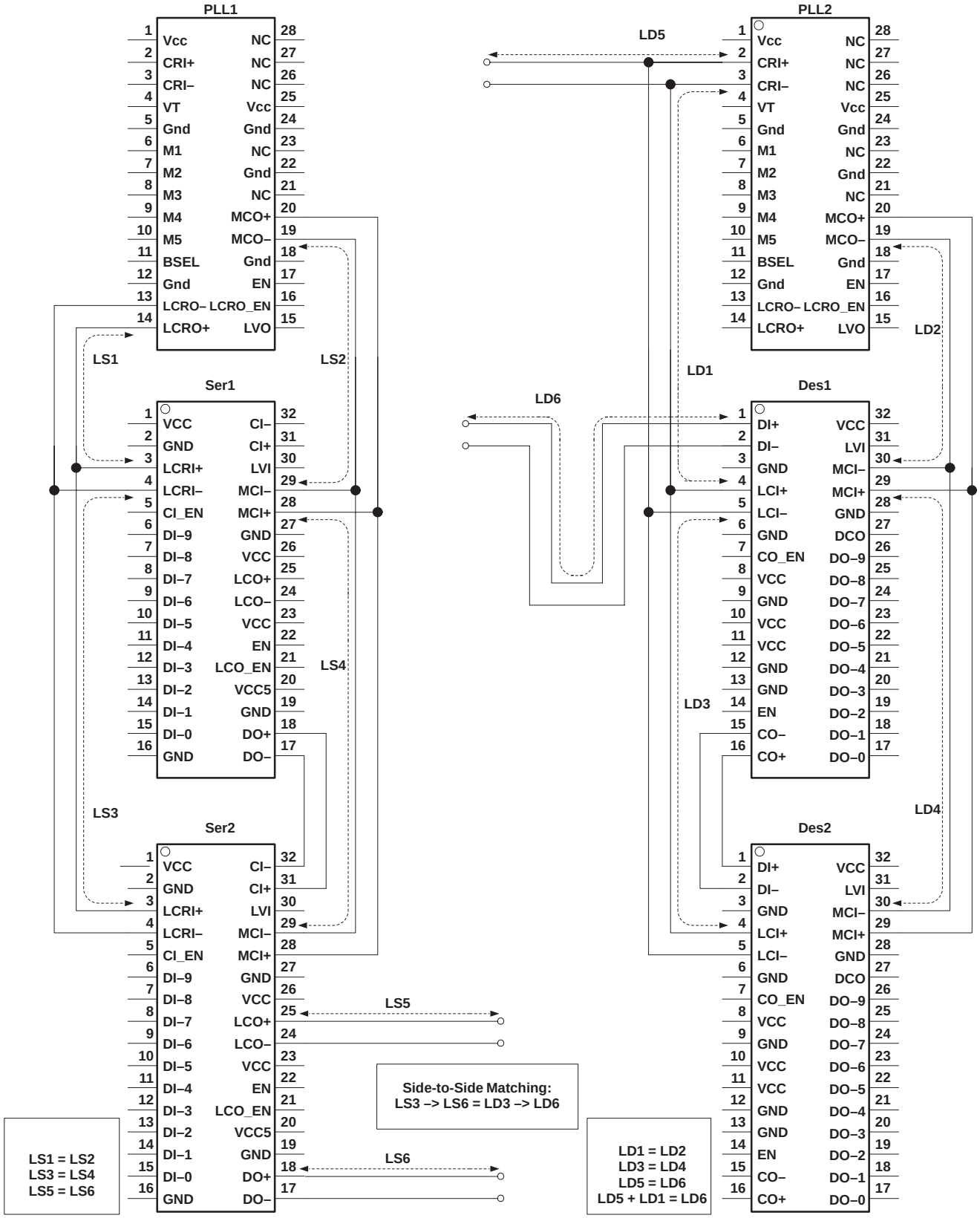


Figure 16. Cascade-Mode Configuration With Noncompensated LVDS Transmission Line Lengths

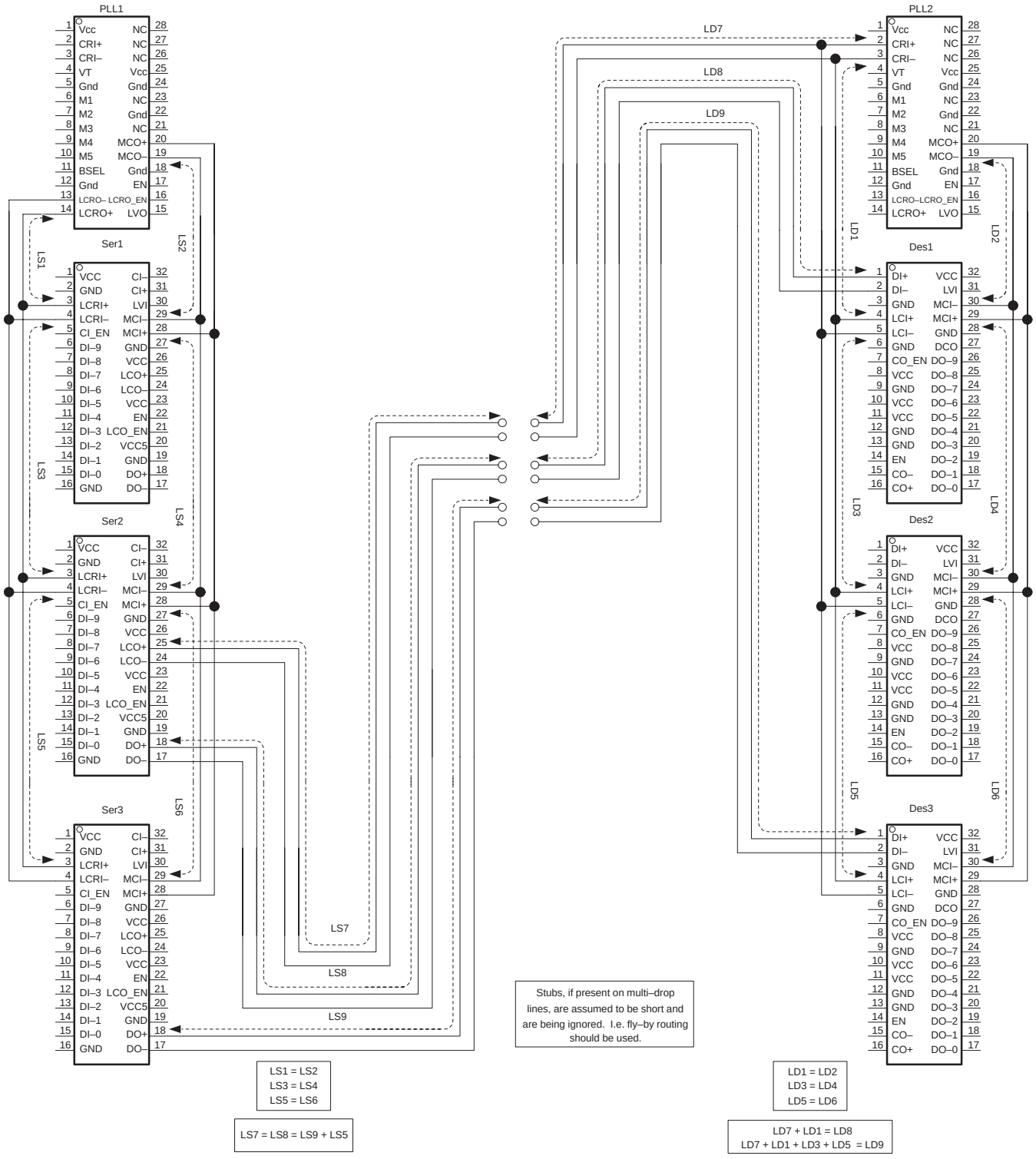


Figure 17. LVDS Signal Routing Matching Requirements Implemented on the MuxIt Customer Evaluation Kit, Which Uses Compensated LVDS Link Line Lengths

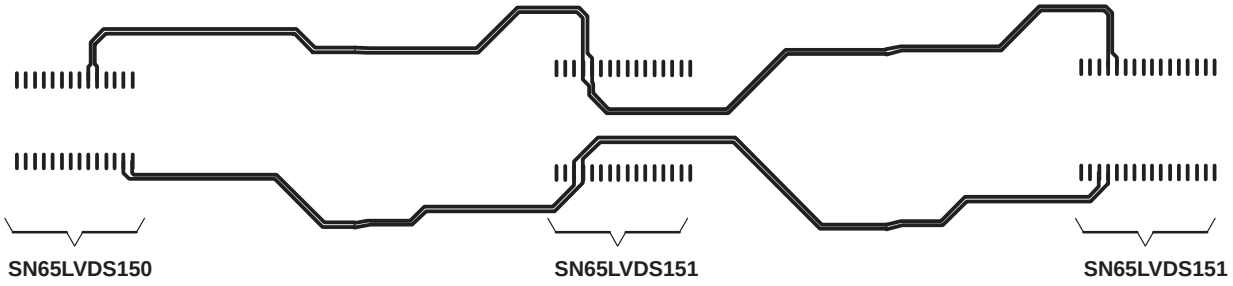
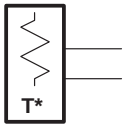


Figure 18. Example of LVDS Signal Interchip Routing Without Stubs or Vias

5.2 Terminations

All the LVDS signals used in MuxIt systems require proper termination. The terminator consists of a single external 100-Ω nominal resistor connected between the two conductors of the LVDS transmission line. The termination resistor must be located as close to the receiver as possible to minimize stub length. The following symbol is used throughout this document to represent the termination:



Several of the MuxIt system signals are distributed to multiple receivers, particularly when cascading or paralleling is used. These multidrop signals must be terminated with a single resistor at the end of the signal distribution chain. In Figure 19 the incoming link-clock and multiplied-clock signals are both distributed in a multidrop configuration. Single termination resistors are shown at the (left, downstream) ends of the multidrop-connected transmission line.

The cascade interface and data input signals in Figure 19 are single-point connected, rather than multidrop. Single termination resistors are also required at the receiver end of those transmission lines.

One exception to the need for external termination resistors is the CI input of the SN65LVDS151. An internal termination resistor has been provided on that LVDS receiver's input because it is the one MuxIt LVDS interface signal that is always singly connected.

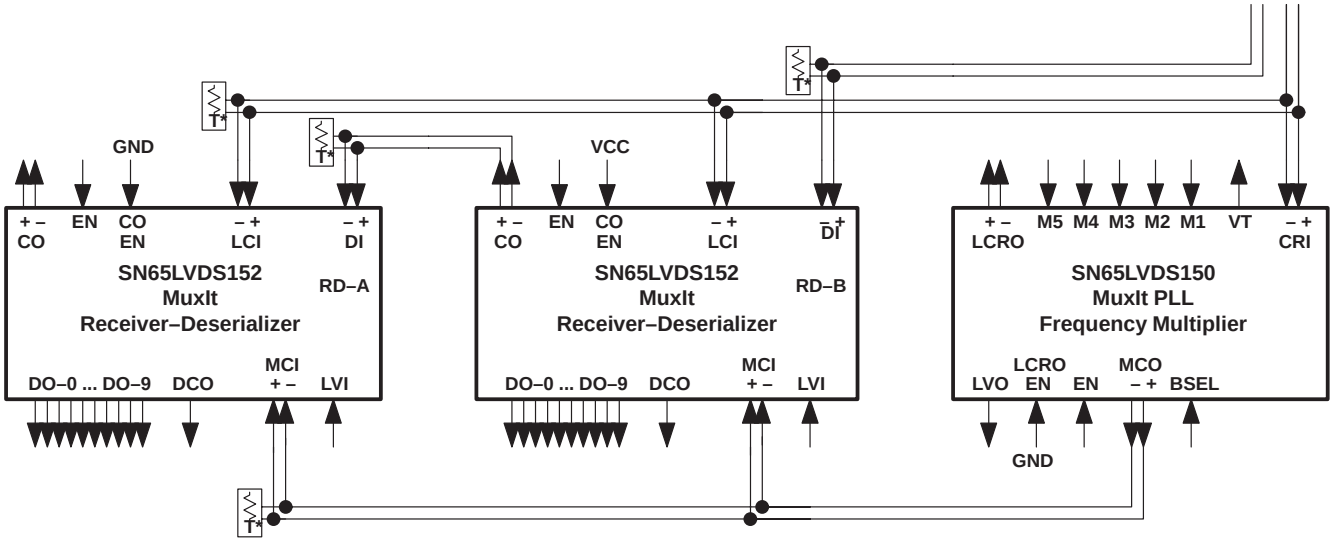


Figure 19. Termination Examples Showing Both Point-to-Point and Multidrop LVDS Signals

6 MuxIt Timing Considerations

This section looks at the details of the interfaces that may be present in a MuxIt system. For simplicity, it is being assumed that the recommended LVDS trace-matching guidelines have been followed, and that chip-to-chip signal skews are negligible. Actual signal skews need to be accounted for in the margins analyzed in this section. The signal-waveform diagrams presented in this section are not generally drawn to scale.

6.1 Source-End PLL-Frequency Multiplier-to-Serializer Interface

The SN65LVDS150 PLL-frequency multiplier is specified to provide the rising edge of the multiplied-clock-output (MCO) signal between 0.5 and 4.5 ns before the rising edge of the link-clock-reference-output (LCRO) signal when operating at 200 MHz. This is the $t_{(1)}$ specification in the SN65LVDS150 data sheet.

The SN65LVDS151 serializer-transmitter has a timing requirement that the rising edge of the link-clock-reference-input (LCRI) signal occurs at least 0.5 ns before, or 0.3 ns after, the rising edge of the multiplied-clock-input (MCI) signal. These are the $t_{su(1)}$ and $t_{h(1)}$ timing requirements listed in *SN65LVDS151 MuxIt Serializer/Transmitter,* (SLLS444).

The relationship between these timing requirements defines the timing margins available for these two clocking signals at the source end of a MuxIt system. The difference between the $t_{(1)}$ minimum of the SN65LVDS150 and the $t_{h(1)}$ minimum of the SN65LVDS151 is the set-up margin for LCRI signal after MCI signal's rising edge. This is illustrated in Figure 20 and calculated as:

$$\begin{aligned} \text{MCI}\uparrow \text{ before LCRI}\uparrow \text{ margin} &= t_{(1)}\ (\text{min}) - t_{h(1)}\ (\text{min}) \\ &= 0.5\ \text{ns} - 0.3\ \text{ns} \\ &= 0.2\ \text{ns} \end{aligned}$$

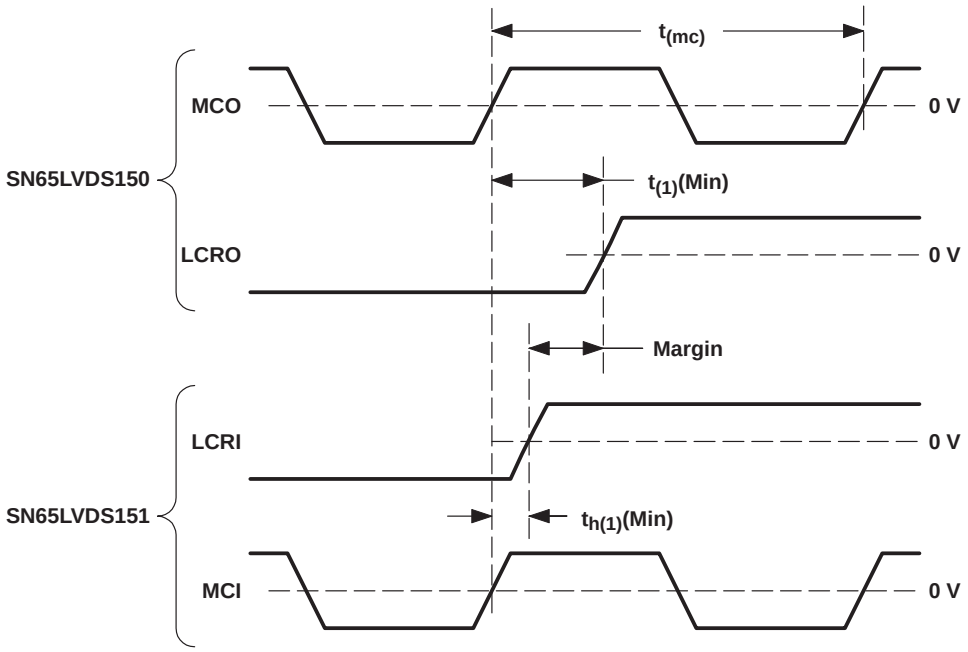


Figure 20. LCRI↑ After MCI↑ Clock Timing at the Source End

The difference between the $t_{(1)}$ maximum of the SN65LVDS150 and the $t_{su(1)}$ minimum of the SN65LVDS151 is the set-up margin for the LCRI before MCI rising edges. At a multiplied clock frequency of 200 MHz, the period $t_{(mc)}$, is 5.0 nanoseconds. This is illustrated in Figure 21 and calculated as:

MCI↑ following LCRI↑ margin $= t_{mc}\ \{t_{(1)}\ (max) + t_{su(1)}\ (min)\}$
$= 5.0\ ns\ \{4.5 + 0.5\}\ ns$
$= 0.0\ ns$

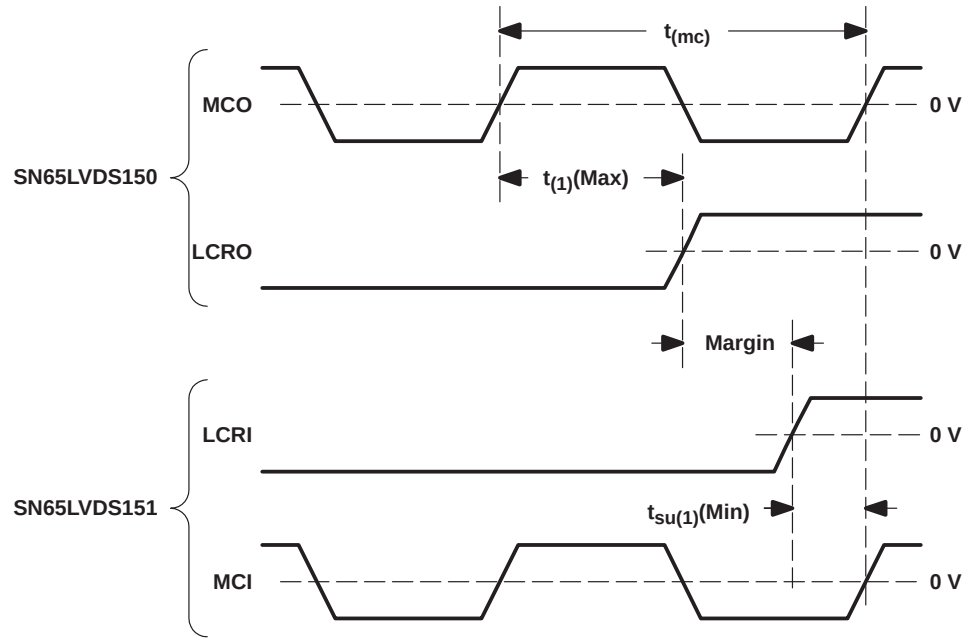


Figure 21. LCRI↑ Before MCI↑ Clock Timing at the Source End

6.2 Source-End Cascade Interface

When two SN65LVDS151 serializer-transmitters are connected in cascade for serializing more than 10 data bits, the critical timing requirement is that the time required to get a data bit transferred between the two units must be less than the period of the multiplied clock. The relevant parameters are the MCI signal period, $t_{(mc)}$, the MCI to DO signal delay, $t_{d(1)}$, and the CI to MCI setup time, $t_{su(3)}$. This is illustrated in Figure 22. The sum of the delay plus setup time, ($t_{d(1)} + t_{su(3)}$), determine the upper limit on MCI in cascade mode. At the data sheet conditions of f_{IN} = 5 MHz, M = 40, and T_A = 85°C, the values of $t_{d(1)}$ and $t_{su(3)}$ are 6.1 ns and –1.1 ns, respectively. At the data sheet conditions of f_{IN} = 5 MHz, M = 40, and $T_A \leq 25°C$ the values of $t_{d(1)}$ and $t_{su(3)}$ are respectively 5.8 ns and –0.8 ns. In both cases the sum $t_{d(1)} + t_{su(3)}$ is 5.0 ns maximum. This gives a minimum for $t_{(mc)}$ of 5.0 ns, or a maximum MCI signal frequency of 200 MHz. At an MCI frequency of 150 MHz, or a period $t_{(mc)}$ of 6.7 ns, the timing margin is:

Source-end cascade interface timing margin = $t_{(mc)} – (t_{d(1)} + t_{su(3)})$
= 6.7 ns – (0.5)
= 0.7 ns

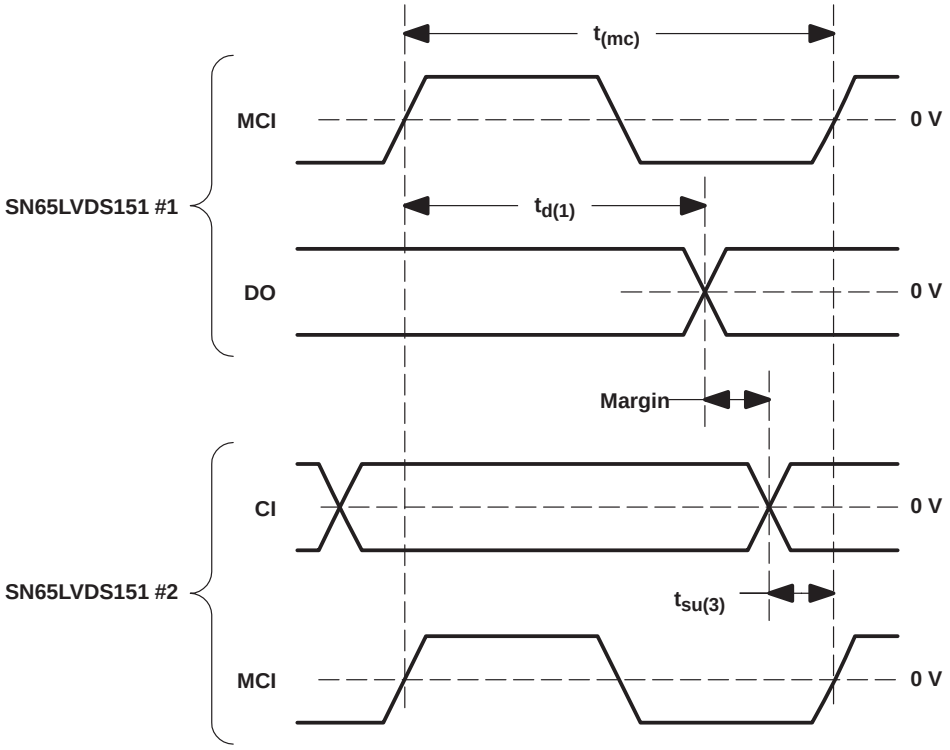


Figure 22. Cascade-Interface Timing at the Source End

6.3 Destination-End PLL-Frequency Multiplier-to-Deserializer Interface

At the destination end of the link, the link-clock signal drives both the SN65LVDS150 PLL-frequency multiplier for regenerating the multiplied clock, and the SN65LVDS152 receiver-deserializer for output data block synchronization. The relevant parameters are the CRI↑ to MCO↑ offset, or t_{OS}, of the SN65LVDS150, and the LCI↑ setup time before and after MCI↓, or $t_{su(1)}$ and $t_{su(2)}$, of the SN65LVDS152. These are ±1.65 ns, 0.0 ns, and 0.7 ns, respectively. Note that the DI setup and hold times are with respect to the falling edge of the MCI signal. At a multiplied-clock frequency of 200 MHz, the period is 5.0 ns; the half period is 2.5 ns.

The relationship between these values defines the timing margins available for these two clocking signals at the destination end of a MuxIt system. Subtracting the clock-reference-to-multiplied-clock offset and the multiplied-clock-before-link-clock setup times from the half period gives the setup margins. This is illustrated in Figure 23 and calculated as:

$$\text{MCI}\downarrow \text{ before LCI}\downarrow \text{ setup margin} = t_{(mc)}/2 - \{t_{os}(\text{max}) + t_{su(1)}(\text{min})\}$$
$$= 2.5 \text{ ns} - \{1.65 + 0.0\} \text{ ns}$$
$$= 0.85 \text{ ns}$$

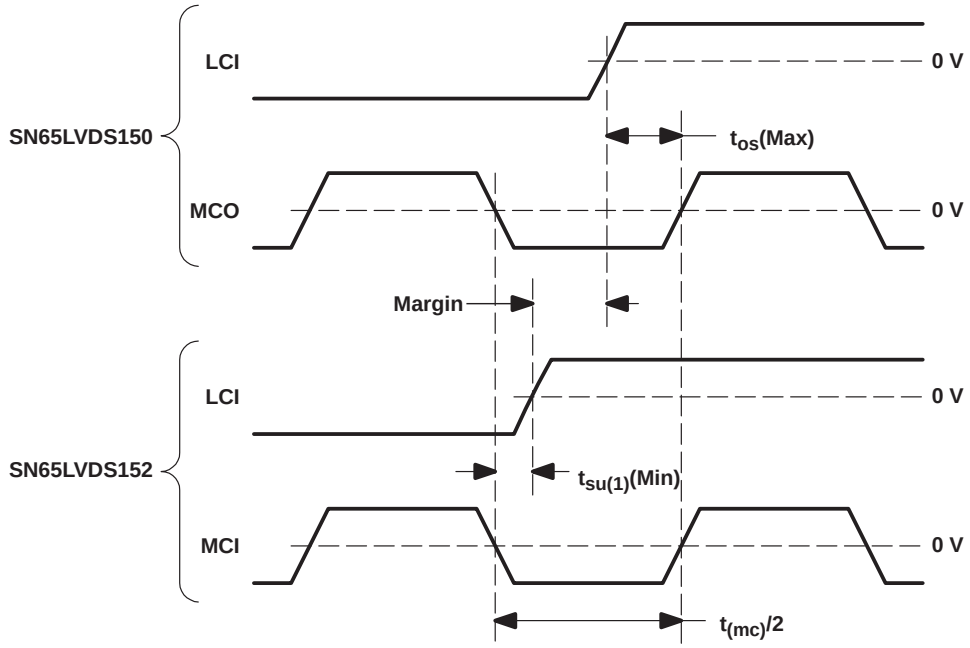


Figure 23. MCI↓ After LCI↓ Setup Timing at the Destination End

Subtracting the clock-reference-to-multiplied-clock offset and the link-clock-before-multiplied setup times from the half period gives the setup margins. This is illustrated in Figure 24 and calculated as:

$$\text{LCI}\downarrow \text{ before MCI}\downarrow \text{ setup margin} = t_{(mc)}/2 - \{t_{os}(\text{min}) + t_{su(2)}\}$$
$$= 2.5 \text{ ns} - \{1.65 + 0.7\} \text{ ns}$$
$$= 0.15 \text{ ns}$$

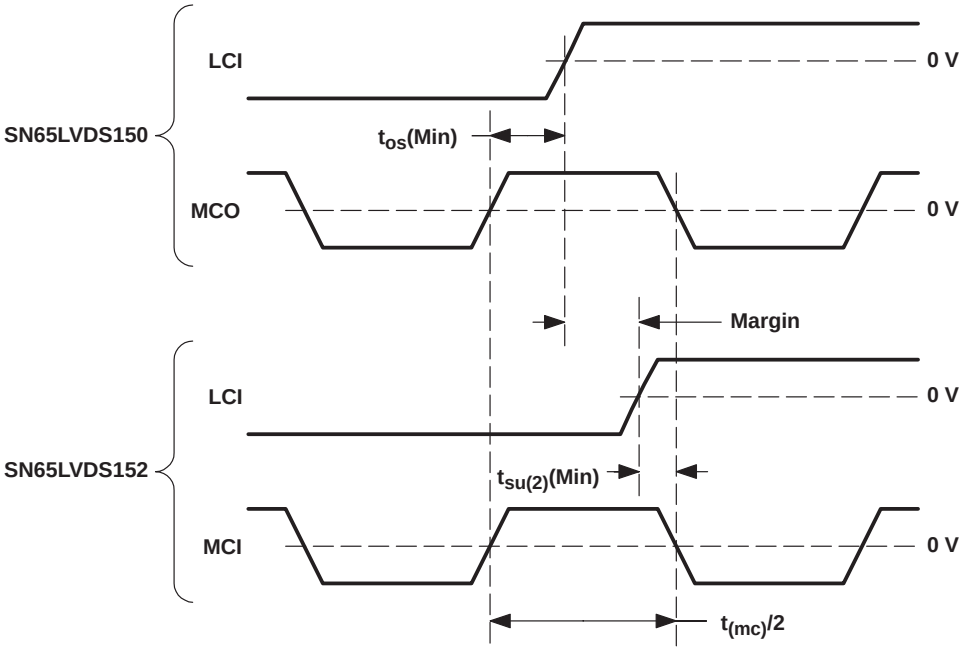


Figure 24. LCI↑ Before MCI↓ Setup Timing at the Destination End

6.4 Destination-End Cascade Interface

When two SN65LVDS 152 receiver-deserializers are connected in cascade for deserializing more than 10 data bits, the critical timing requirement is that the period of the multiplied clock frequency must be longer than the time required to get a data bit transferred between the two units. The relevant parameters are the MCI period $t_{(mc)}$, the MCI to CO delay $t_{d(3)}$, and the DI to MCI setup time $t_{su(3)}$. This is illustrated in Figure 25. The sum of the delay and setup times, ($td_{(3)}$ + $t_{su(3)}$), determine the maximum limit on MCI in cascade mode. The data sheet limits for the values of $t_{d(3)}$ and $t_{su(3)}$ are 4.5 ns and 0.3 ns, respectively. This gives a minimum for $t_{(mc)}$ of 4.8 ns, or a maximum MCI signal frequency of 208 MHz. This is higher than the maximum supported by the source-end cascade interface, so it is not a system performance limitation.

At an MCI signal frequency of 200 MHz, or a period $t_{(mc)}$ of 5.0 ns, the timing margin is:

Destination-end cascade interface timing margin $= t_{(mc)} – (t_{d(3)} + t_{su(3)})$
$= 5.0 \text{ ns} – (4.5 + 0.3) \text{ ns}$
$= 0.2 \text{ ns}$

At an MCI frequency of 150 MHz, or a period $t_{(mc)}$ of 6.7 ns, the timing margin is:

Destination-end cascade interface timing margin $= t_{(mc)} – (t_{d(3)} + t_{su(3)})$
$= 6.7 \text{ ns} – (4.5 + 0.3) \text{ ns}$
$= 1.9 \text{ ns}$

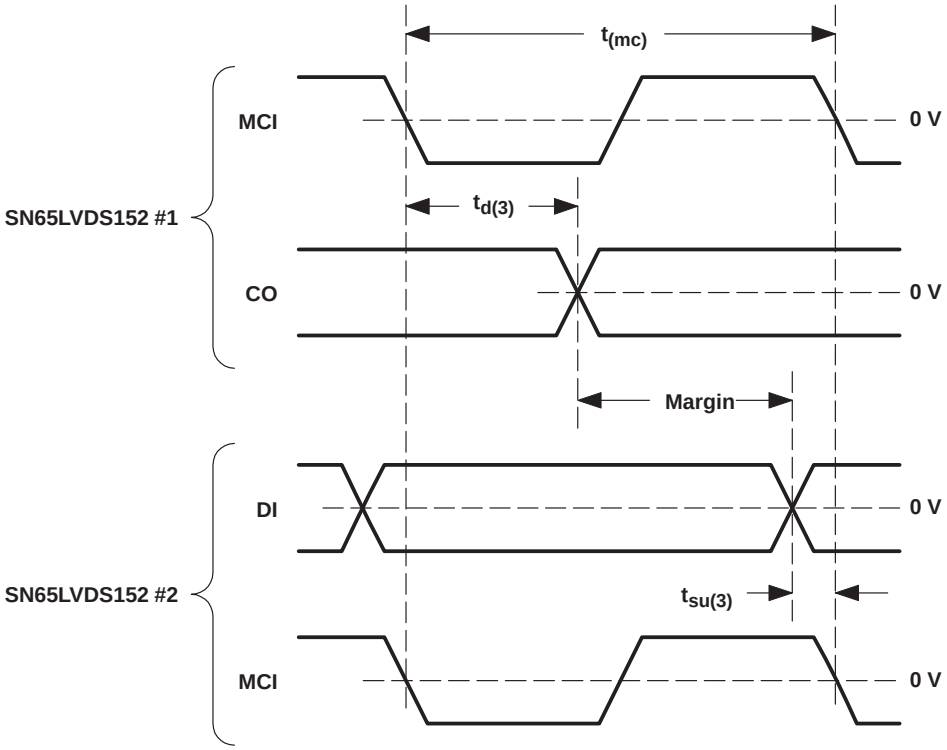


Figure 25. Cascade Interface Timing at the Destination End

6.5 Source-to-Destination Link Data Interface, Single Link Data Line (Basic and Cascade Modes)

At the source end of the link, both the link-clock and link-data signals are clocked from the SN65LVDS151 serializer-transmitter by the MCI signal. An internal deskewing circuit minimizes the time displacement between these signals. The relevant specifications are the multiple-frequency skew between the rising edge of the LCO signal and either edge of the DO signal, or $t_{sk(\omega)}$, which is ±250 ps.

At the destination end of the link, The link-clock signal drives the SN65LVDS150 PLL-frequency multiplier as the reference for regenerating the multiplied clock. The link-data signal drives the SN65LVDS152 receiver-deserializer. The relevant parameters are the CRI↑ to MCO↑ offset, or t_{os}, of the SN65LVDS150, and the DI setup and hold time to MCI↓, or $t_{su(3)}$ and $t_{h(3)}$, of the SN65LVDS152. These are ±1.65 ns, 0.3 ns, and 0.5 ns, respectively. Note that the DI setup and hold times are with respect to the falling edge of the MCI signal. At a multiplied clock frequency of 200 MHz, the period is 5.0 ns, and the half period is 2.5 ns.

The relationship between these values defines the timing margins available for the incoming link-data signal at this destination end of the MuxIt system. The worst case for data-input setup time occurs when the incoming link-data signal is late relative to the link-clock signal, and when the multiplied-clock signal is early relative to the link-clock signal. This is illustrated in Figure 26. It is evaluated relative to the link-data signal as:

$$\begin{aligned}\text{DI setup margin} &= -t_{sk(\omega)}(\text{min}) - t_{os}(\text{min}) + t_{(mc)}/2 - t_{su(3)}(\text{min})\\ &= -0.25\text{ ns} - 1.65\text{ ns} + 2.5\text{ ns} - 0.3\text{ ns}\\ &= 0.3\text{ ns}\end{aligned}$$

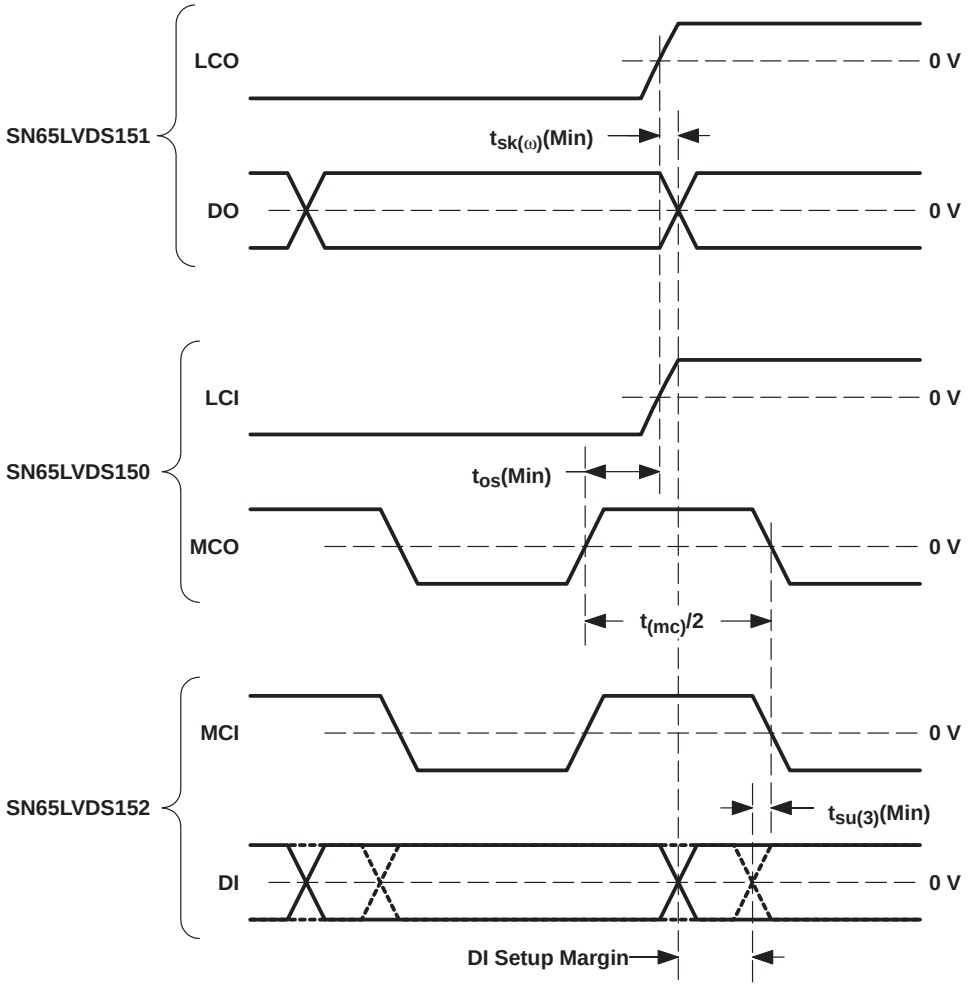


Figure 26. Source-to-Destination Data Input Setup Timing

The worst case for data-input hold time occurs when the incoming link-data signal is early relative to the link-clock signal, and when the multiplied-clock signal is late relative to the link-clock signal. This is illustrated in Figure 27. It is evaluated relative to the link-data signal as:

$$\text{DI hold margin} = t_{(mc)} - \{t_{sk(\omega)}(\max) + t_{os}(\max) + t_{(mc)}/2 + t_{h(3)}(\min)\}$$
$$= 5.0\text{ ns} - \{0.25 + 1.65 + 2.5 + 0.5\}\text{ ns}$$
$$= 0.1\text{ ns}$$

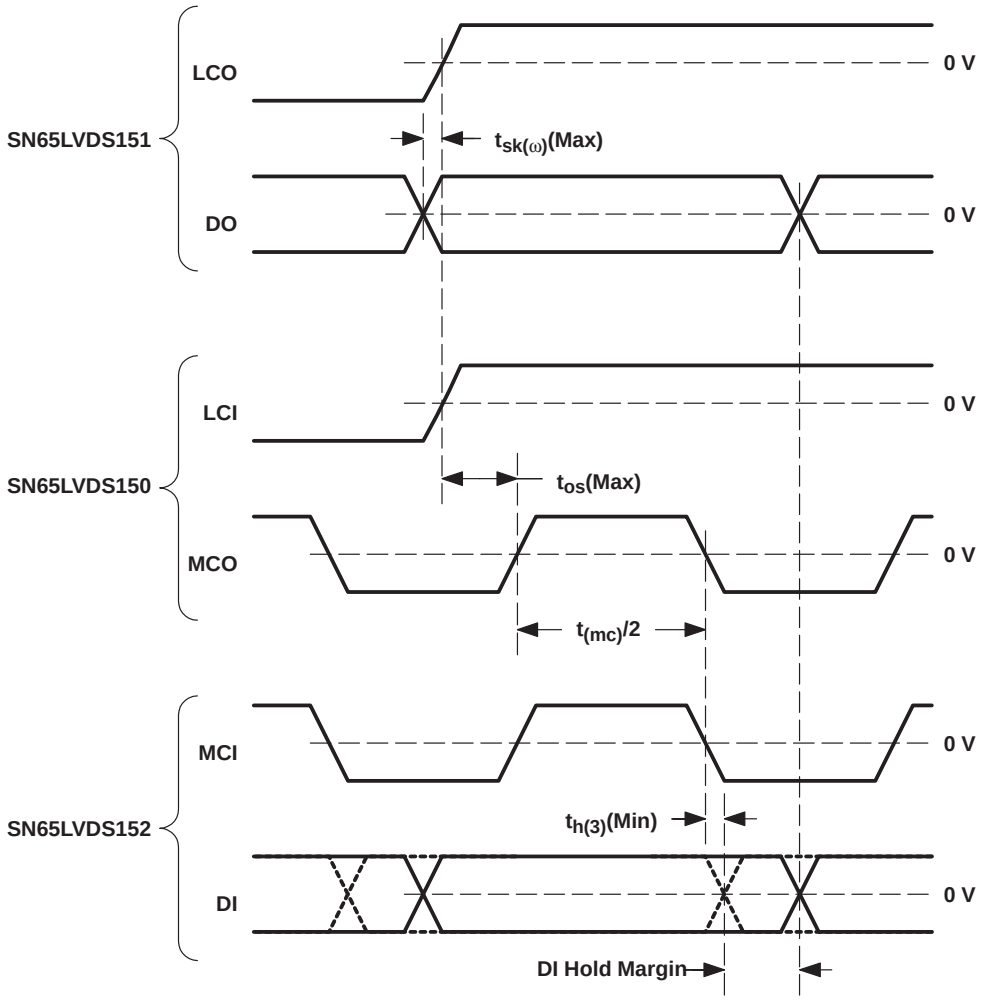


Figure 27. Source-to-Destination Data Input Hold Timing

6.6 Source-to-Destination Link Interface, Multiple Link Data Lines (Parallel Mode)

Adding one or more serializer-transmitter and receiver-deserializer units to the basic configuration, and operating them in the parallel mode, introduces additional timing constrains. In particular, the additional parallel-mode SN65LVDS151 serializer-transmitter units introduce a chip-to-chip skew between the Link Data outputs. The Link Data outputs of the additional parallel-mode units do not benefit from the deskewing function in the SN65LVDS151 serializer-transmitter that is sourcing the link-clock signal.

The worst case for parallel input data setup time occurs when the link-clock-output signal leads the primary (#1) link-data output signal, and when the parallel-mode (#2) data-output signal lags the primary (#1) link-data output signal. This is illustrated in Figure 28 and calculated relative to the LCO signal as a function of the multiplied-clock period, $t_{(mc)}$, as:

$$\begin{aligned}\text{DI \#2 setup margin} &= [-t_{os}(\text{min}) + t_{(mc)}/2 - t_{su(3)}(\text{min})] - [t_{sk(\omega)}(\text{min}) + t_{sk(pp)}(\text{max})] \\ &= [-1.65 + t_{(mc)}/2 - 0.3]\ \text{ns} - [0.25 + 2.3]\ \text{ns} \\ &= [t_{(mc)}/2 - 4.5]\ \text{ns}\end{aligned}$$

The minimum for $t_{(mc)}$ is 9.0 ns, or a multiplied-clock frequency of 111 MHz. At a multiplied-clock frequency of 100 MHz, or $t_{(mc)}$ = 10 ns, the DI #2 setup time margin is 0.5 ns.

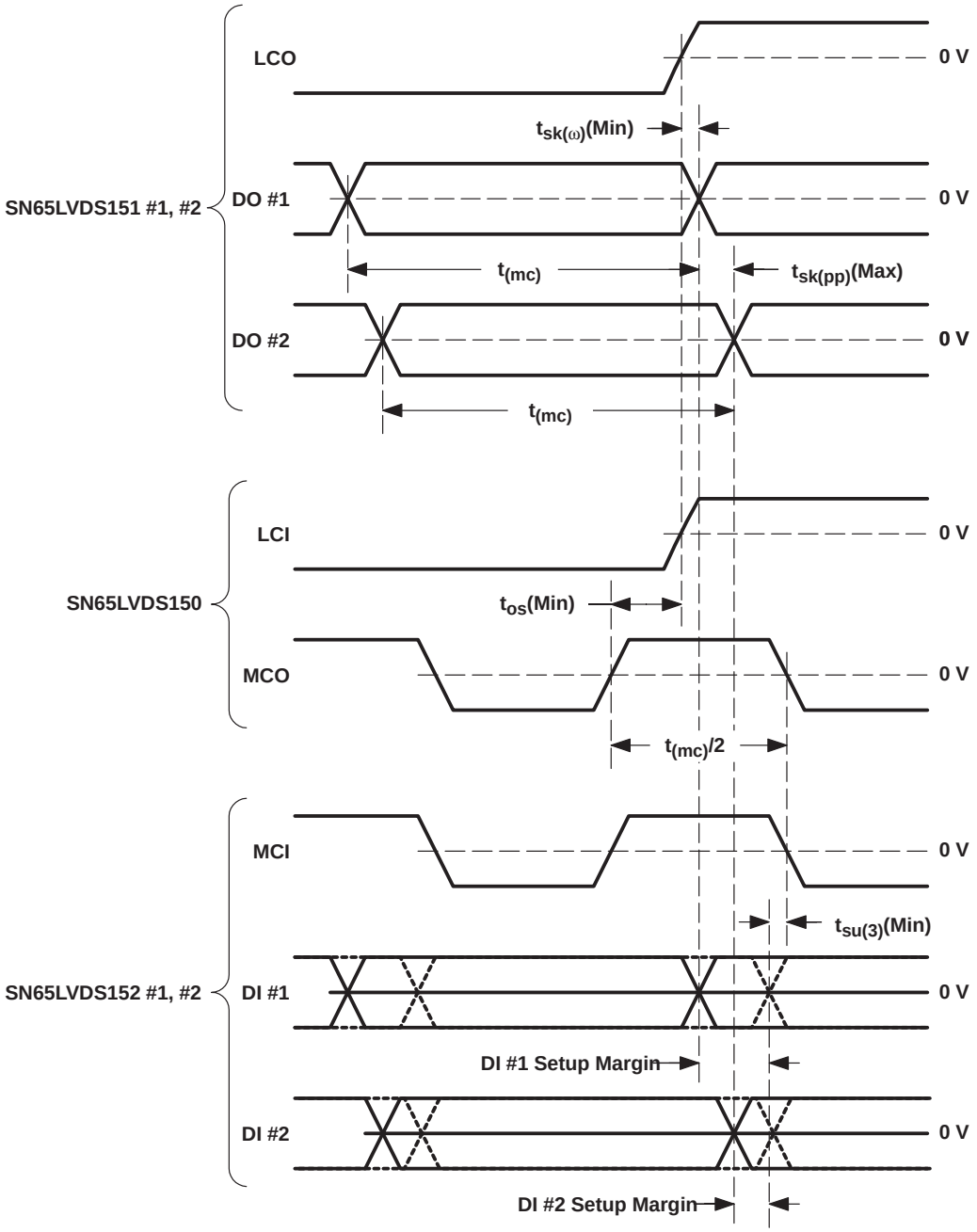


Figure 28. Source-to-Destination Parallel-Mode Data Input Setup Timing

The worst case for parallel input data hold time occurs when the link-clock-output signal lags the primary (#1) link-data output signal, and when the parallel-mode (#2) data output signal leads the primary (#1) link-data output signal. This is illustrated in Figure 29 and calculated relative to the LCO signal as a function of the multiplied clock period, $t_{(mc)}$, as:

$$\begin{aligned}\text{DI \#2 hold margin} &= [- t_{sk(\omega)}(\max) - t_{sk(pp)}(\min) + t_{(mc)}] - [t_{os}(\max) + t_{(mc)}/2 + t_{h(3)}(\min)] \\ &= [- 0.25 - 2.3 + t_{(mc)}] \text{ ns} - [1.65 + t_{(mc)}/2 + 0.5] \text{ ns} \\ &= [t_{(mc)}/2 - 4.7] \text{ ns}\end{aligned}$$

At a multiplied clock frequency of 100 MHz, or $t_{(mc)}$ = 10 ns, the DI #2 hold-time margin is 0.3 ns.

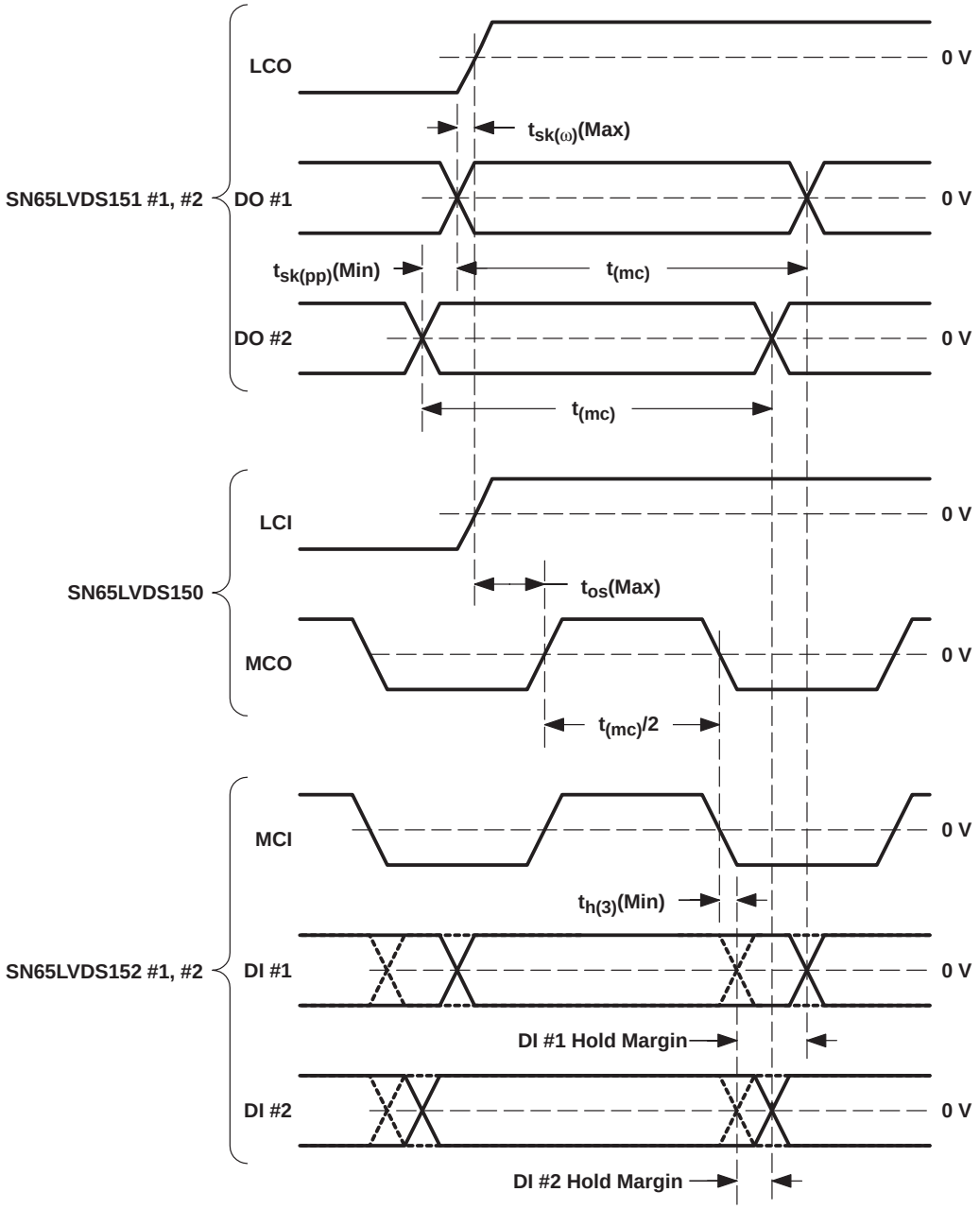
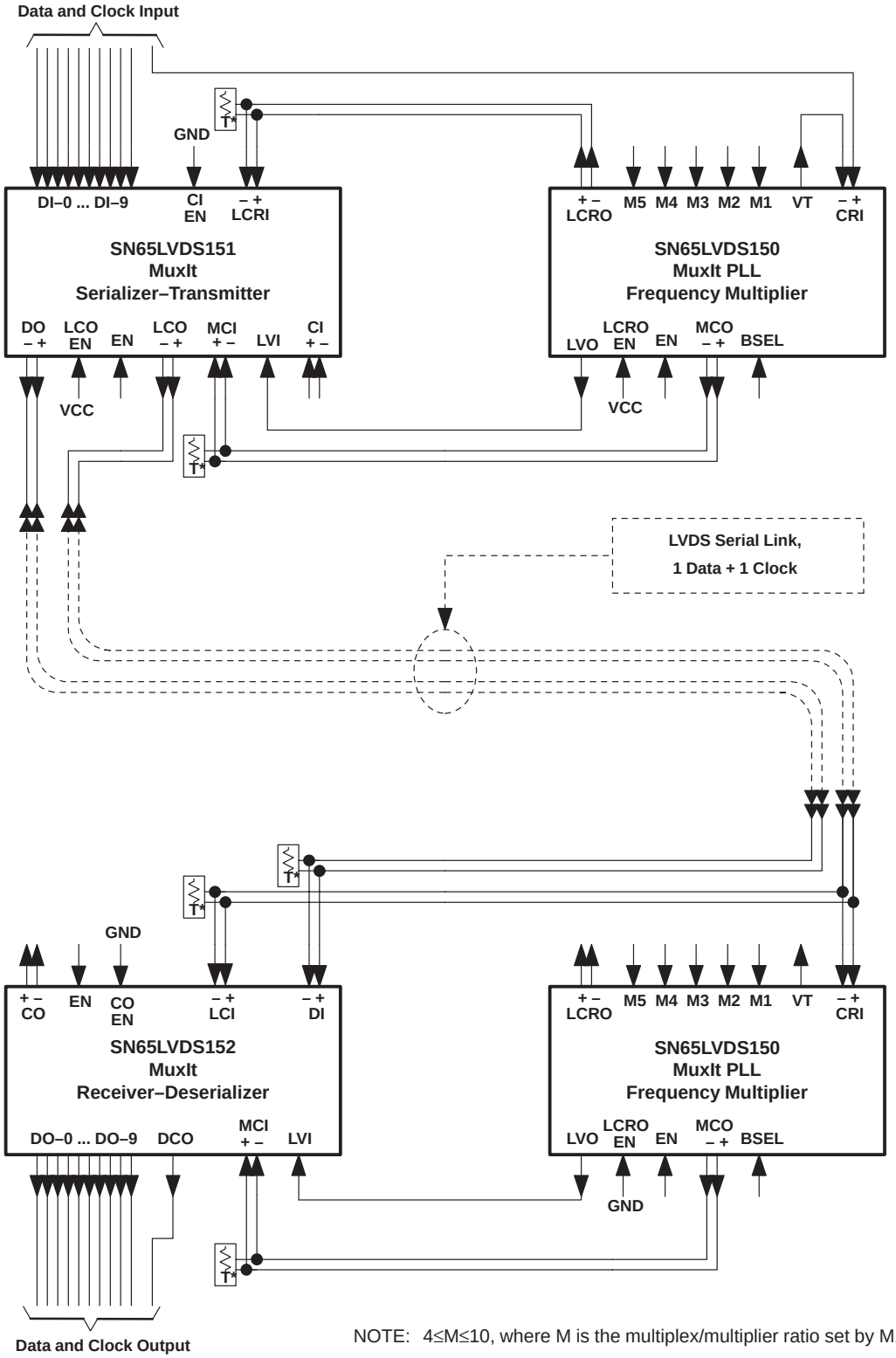


Figure 29. Source-to-Destination Parallel-Mode Data Input Hold Timing

7 MuxIt Application Examples

This section presents details on implementing several MuxIt configurations.

7.1 A Basic System With 4 to 10 Parallel I/O Lines, All Data Carried Over One LVDS Serial Link



NOTE: 4≤M≤10, where M is the multiplex/multiplier ratio set by M1 through M5.

Figure 30. Basic MuxIt Configuration for up to 10 Bits of Parallel Data on One Link

Table 4. Input-to-Output BIt Map for Basic Configuration

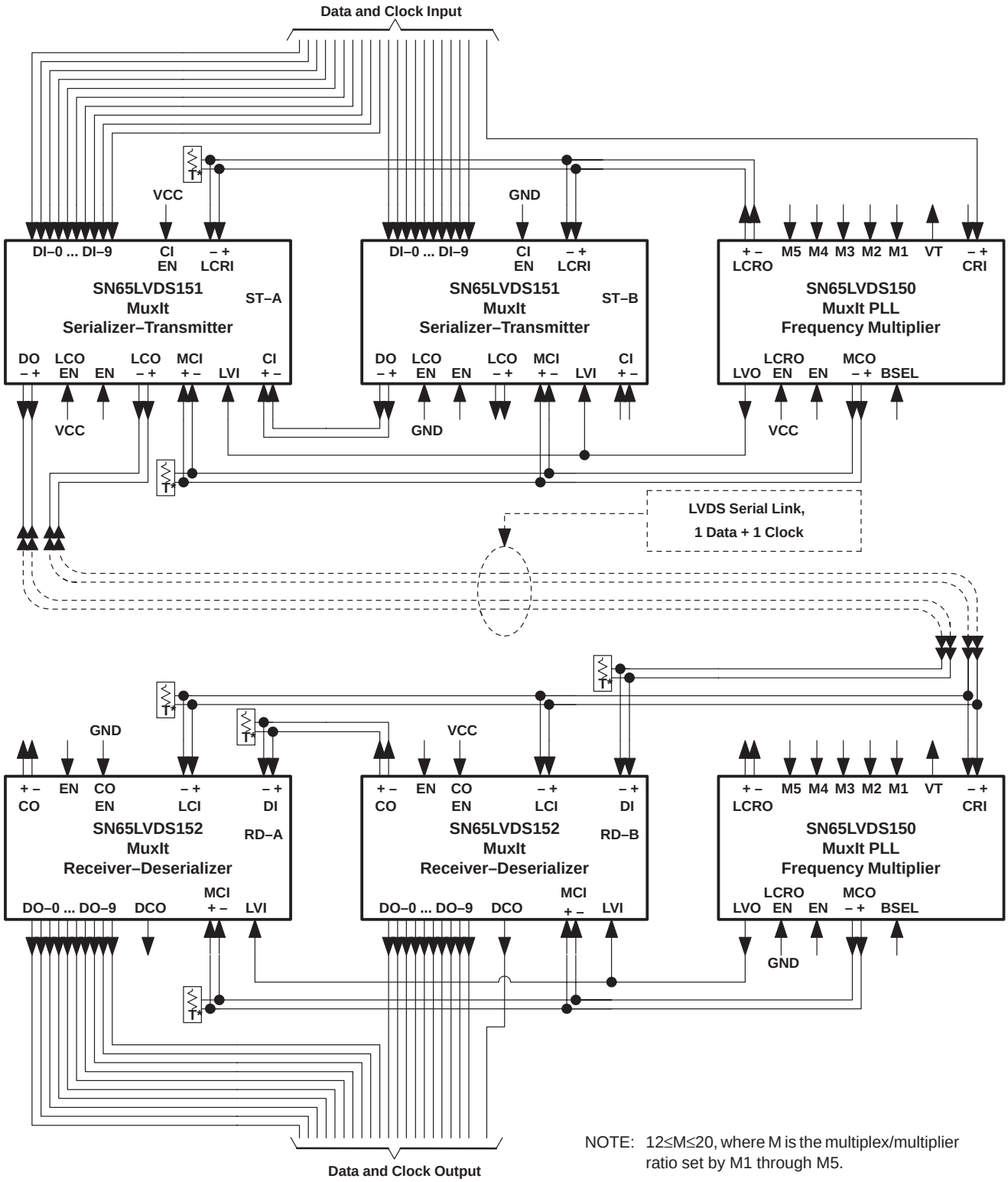
INPUTS	OUTPUTS				
	M = 4	M = 6	M = 8	M = 9	M = 10
DI-0	DO-6	DO-4	DO-2	DO-1	DO-0
DI-1	DO-7	DO-5	DO-3	DO-2	DO-1
DI-2	DO-8	DO-6	DO-4	DO-3	DO-2
DI-3	DO-9	DO-7	DO-5	DO-4	DO-3
DI-4	Invalid	DO-8	DO-6	DO-5	DO-4
DI-5	Invalid	DO-9	DO-7	DO-6	DO-5
DI-6	Invalid	Invalid	DO-8	DO-7	DO-6
DI-7	Invalid	Invalid	DO-9	DO-8	DO-7
DI-8	Invalid	Invalid	Invalid	DO-9	DO-8
DI-9	Invalid	Invalid	Invalid	Invalid	DO-9

7.1.1 Simplest Configuration

The simplest configuration consists of:

- 4 to 10 parallel data I/O lines
- Select matching PLL multiplier ratio (M) between 4 and 10
- Parallel data input clock rates from 5 MHz, up to 20 MHz (at M = 10) to 50 MHz (at M = 4)
- 2 LVDS link lines, 1 for data + 1 for clock timing reference
- Aggregate data rate up to 200 Mb/s

7.2 A System With 12 to 20 Parallel I/O Lines, All Data Carried Over One LVDS Serial Link



NOTE: 12≤M≤20, where M is the multiplex/multiplier ratio set by M1 through M5.

Figure 31. MuxIt Configuration for 12 to 20 Bits of Parallel Data on One Link

Table 5. Input-to-Output Bit Map for Wide Fast System, 12 to 20 Parallel I/O Lines, All Data Carried Over One LVDS Serial Link

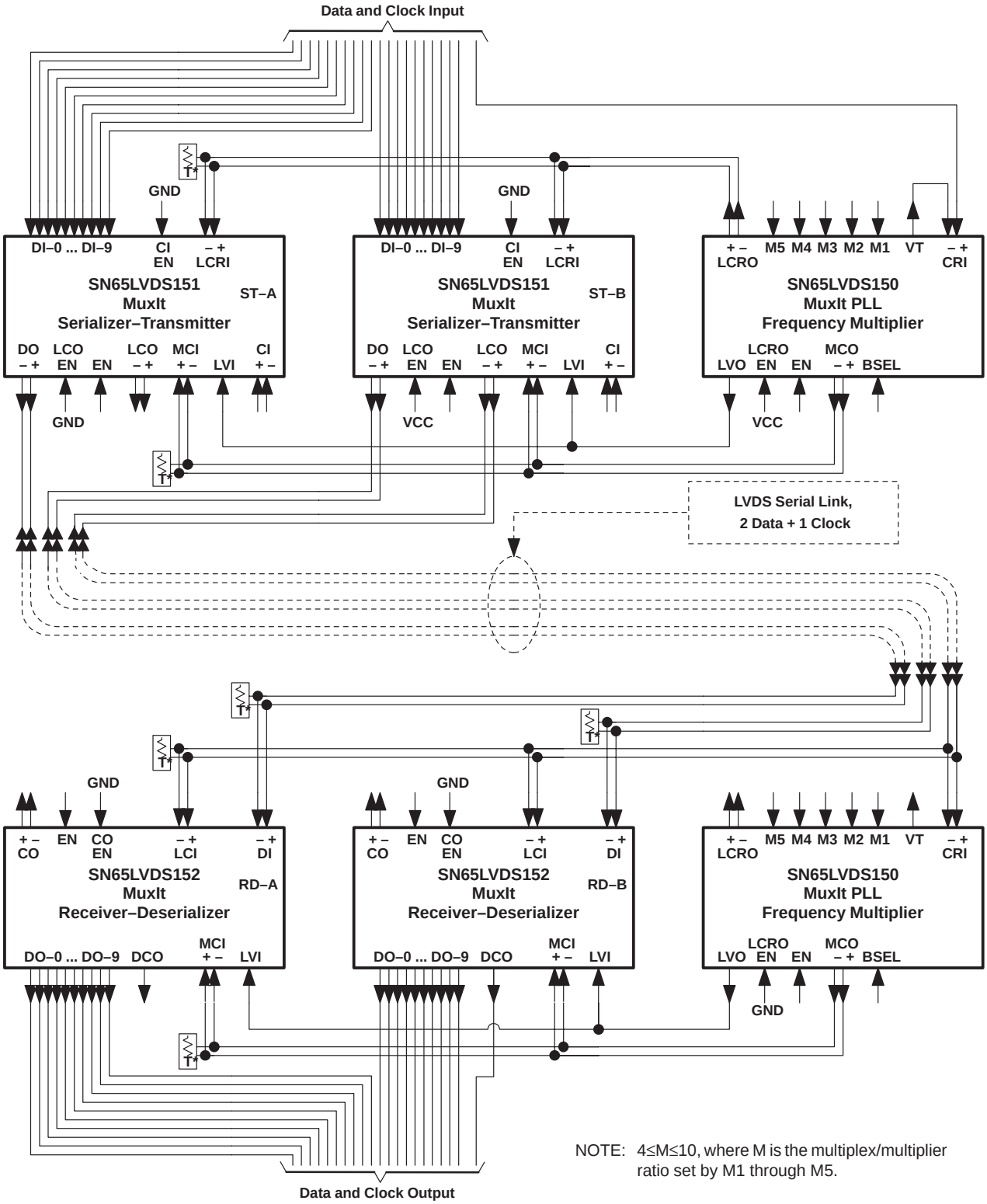
INPUTS	OUTPUTS								
	M = 12	M = 13	M = 14	M = 15	M = 16	M = 17	M = 18	M = 19	M = 20
DI-0A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A	DO-3A	DO-2A	DO-1A	DO-0A
DI-1A	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A	DO-3A	DO-2A	DO-1A
DI-2A	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A	DO-3A	DO-2A
DI-3A	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A	DO-3A
DI-4A	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A
DI-5A	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A
DI-6A	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A
DI-7A	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A
DI-8A	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A
DI-9A	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A
DI-0B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B
DI-1B	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B
DI-2B	Invalid	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B
DI-3B	Invalid	Invalid	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B
DI-4B	Invalid	Invalid	Invalid	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B
DI-5B	Invalid	Invalid	Invalid	Invalid	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B
DI-6B	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9B	DO-8B	DO-7B	DO-6B
DI-7B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9B	DO-8B	DO-7B
DI-8B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9B	DO-8B
DI-9B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9B

7.2.1 Cascaded Serial Units at Each End of the Link

This setup consists of the following:

- 12 to 20 parallel data I/O lines
- Select matching PLL multiplier ratio (M) between 12 and 20
- Parallel data input clock rates from 5 MHz, up to 10 MHz (at M = 20) to 16.7 MHz (at M = 12)
- Two DS link lines, one for data and one for clock timing reference
- Aggregate data rate up to 200 Mbps

7.3 System With 8 to 20 Parallel I/O Lines, All Data Carried Over Two LVDS Serial Links†



NOTE: 4≤M≤10, where M is the multiplex/multiplier ratio set by M1 through M5.

Figure 32. MuxIt Configuration for 8 to 20 Bits of Parallel Data on Two Links

† The aggregate data rate (data clock × parallel width) is too high for a single LVDS link.

Table 6. Input-to-Output Bit Map for Wide Fast System, 4 to 10 Parallel I/O Lines, All Data Carried Over One LVDS Serial Link

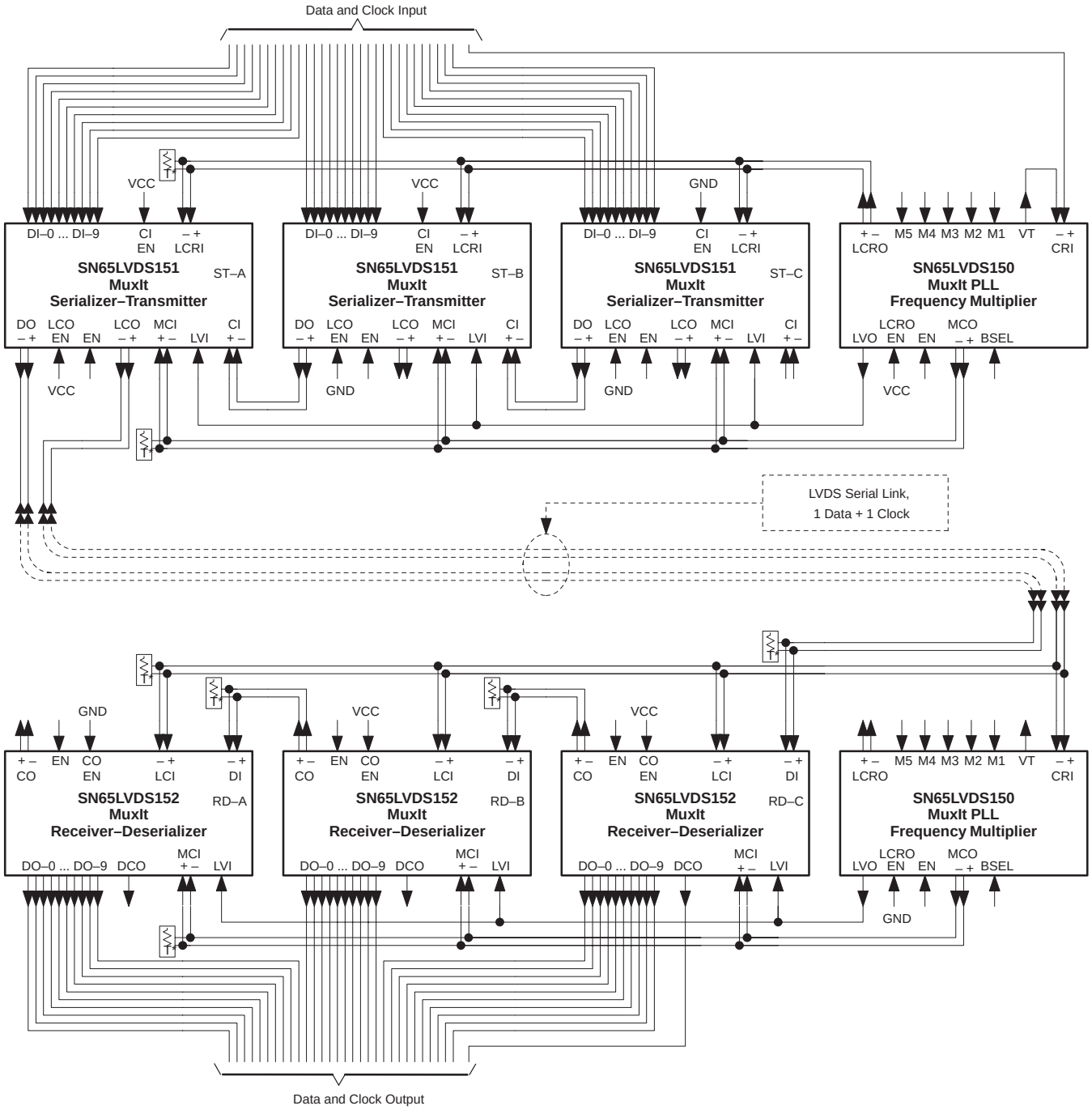
INPUTS	OUTPUTS				
	M = 4	M = 6	M = 8	M = 9	M = 10
DI-0A	DO-6A	DO-4A	DO-2A	DO-1A	DO-0A
DI-1A	DO-7A	DO-5A	DO-3A	DO-2A	DO-1A
DI-2A	DO-8A	DO-6A	DO-4A	DO-3A	DO-2A
DI-3A	DO-9A	DO-7A	DO-5A	DO-4A	DO-3A
DI-4A	Invalid	DO-8A	DO-6A	DO-5A	DO-4A
DI-5A	Invalid	DO-9A	DO-7A	DO-6A	DO-5A
DI-6A	Invalid	Invalid	DO-8A	DO-7A	DO-6A
DI-7A	Invalid	Invalid	DO-9A	DO-8A	DO-7A
DI-8A	Invalid	Invalid	Invalid	DO-9A	DO-8A
DI-9A	Invalid	Invalid	Invalid	Invalid	DO-9A
DI-0B	DO-6B	DO-4B	DO-2B	DO-1B	DO-0B
DI-1B	DO-7B	DO-5B	DO-3B	DO-2B	DO-1B
DI-2B	DO-8B	DO-6B	DO-4B	DO-3B	DO-2B
DI-3B	DO-9B	DO-7B	DO-5B	DO-4B	DO-3B
DI-4B	Invalid	DO-8B	DO-6B	DO-5B	DO-4B
DI-5B	Invalid	DO-9B	DO-7B	DO-6B	DO-5B
DI-6B	Invalid	Invalid	DO-8B	DO-7B	DO-6B
DI-7B	Invalid	Invalid	DO-9B	DO-8B	DO-7B
DI-8B	Invalid	Invalid	Invalid	DO-9B	DO-8B
DI-9B	Invalid	Invalid	Invalid	Invalid	DO-9B

7.3.1 Paralleled Serial Units at Each End of the Link

This setup consists of:

- Up to 20 parallel data I/O lines divided equally between two pairs of serial units
- Select matching PLL multiplier ratio (M) between 4 and 10
- Parallel data input clock rates from 5 MHz, up to 20 MHz (at M = 10) to 25 MHz (at M = 4)
- Three LVDS link lines, two for data and one for clock timing reference
- Aggregate data rate up to 2 x 100 Mbps = 200 Mbps

7.4 A System With 22 to 30 Parallel I/O Lines, Data Carried Over One LVDS Serial Link†



NOTE: 22≤M≤30, where M is the multiplex/multiplier ratio set by M1 through M5.

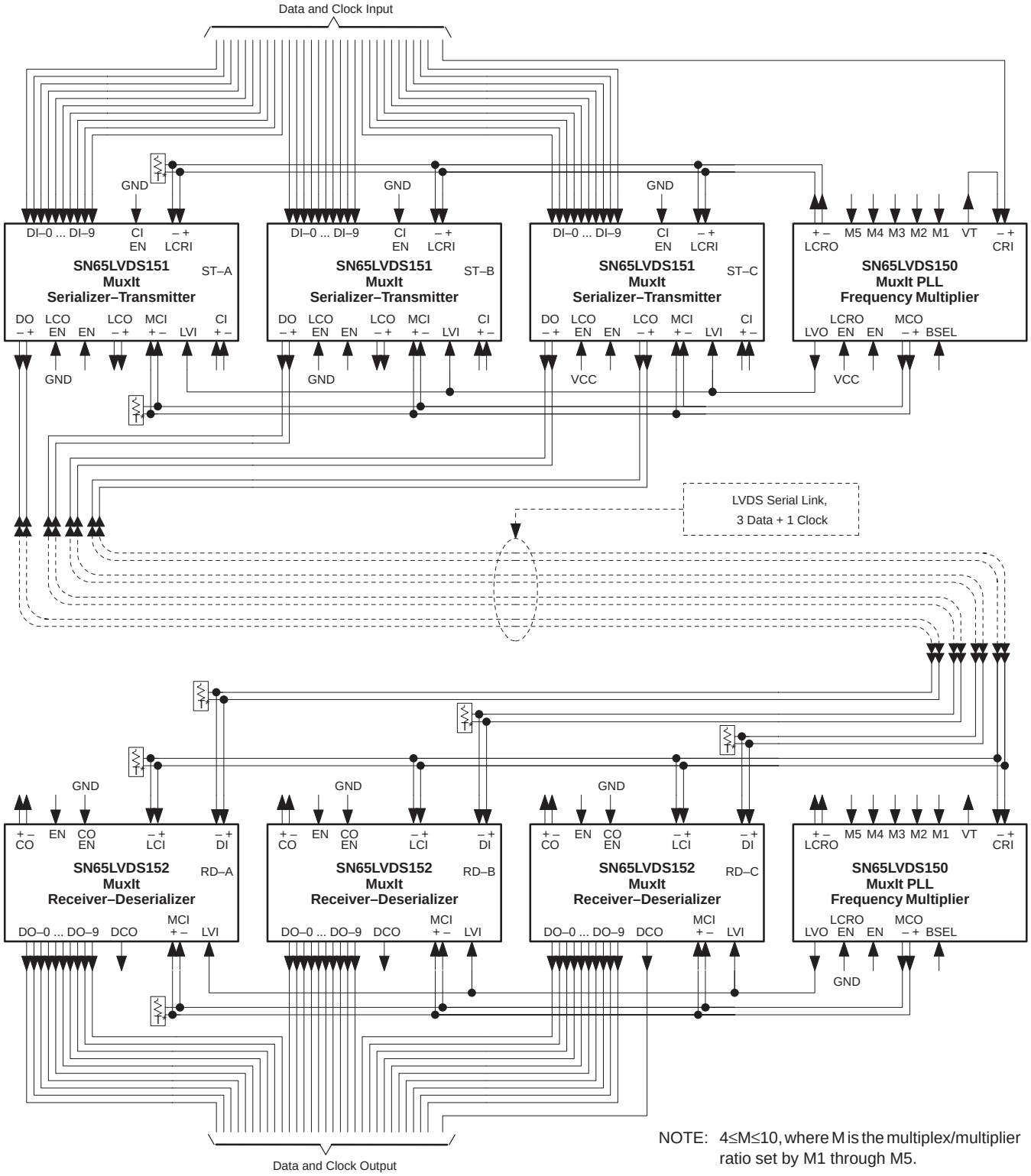
Figure 33. MuxIt Configuration for 22 to 30 Bits of Parallel Data on One Link

† The aggregate data rate (data clock × parallel width) is too high for a single LVDS link.

Table 7. Input-to-Output Bit Map for Very-Wide Moderate-Speed System, 22 to 30 Parallel I/O Lines, Data Carried Over One LVDS Serial Link

INPUTS	OUTPUTS				
	M = 22	M = 24	M = 26	M = 28	M = 30
DI-0A	DO-8A	DO-6A	DO-4A	DO-2A	DO-0A
DI-1A	DO-9A	DO-7A	DO-5A	DO-3A	DO-1A
DI-2A	DO-0B	DO-8A	DO-6A	DO-4A	DO-2A
DI-3A	DO-1B	DO-9A	DO-7A	DO-5A	DO-3A
DI-4A	DO-2B	DO-0B	DO-8A	DO-6A	DO-4A
DI-5A	DO-3B	DO-1B	DO-9A	DO-7A	DO-5A
DI-6A	DO-4B	DO-2B	DO-0B	DO-8A	DO-6A
DI-7A	DO-5B	DO-3B	DO-1B	DO-9A	DO-7A
DI-8A	DO-6B	DO-4B	DO-2B	DO-0B	DO-8A
DI-9A	DO-7B	DO-5B	DO-3B	DO-1B	DO-9A
DI-0B	DO-8B	DO-6B	DO-4B	DO-2B	DO-0B
DI-1B	DO-9B	DO-7B	DO-5B	DO-3B	DO-1B
DI-2B	DO-0C	DO-8B	DO-6B	DO-4B	DO-2B
DI-3B	DO-1C	DO-9B	DO-7B	DO-5B	DO-3B
DI-4B	DO-2C	DO-0C	DO-8B	DO-6B	DO-4B
DI-5B	DO-3C	DO-1C	DO-9B	DO-7B	DO-5B
DI-6B	DO-4C	DO-2C	DO-0C	DO-8B	DO-6B
DI-7B	DO-5C	DO-3C	DO-1C	DO-9B	DO-7B
DI-8B	DO-6C	DO-4C	DO-2C	DO-0C	DO-8B
DI-9B	DO-7C	DO-5C	DO-3C	DO-1C	DO-9B
DI-0C	DO-8C	DO-6C	DO-4C	DO-2C	DO-0C
DI-1C	DO-9C	DO-7C	DO-5C	DO-3C	DO-1C
DI-2C	Invalid	DO-8C	DO-6C	DO-4C	DO-2C
DI-3C	Invalid	DO-9C	DO-7C	DO-5C	DO-3C
DI-4C	Invalid	Invalid	DO-8C	DO-6C	DO-4C
DI-5C	Invalid	Invalid	DO-9C	DO-7C	DO-5C
DI-6C	Invalid	Invalid	Invalid	DO-8C	DO-6C
DI-7C	Invalid	Invalid	Invalid	DO-9C	DO-7C
DI-8C	Invalid	Invalid	Invalid	Invalid	DO-8C
DI-9C	Invalid	Invalid	Invalid	Invalid	DO-9C

7.5 A System With 12 to 30 Parallel I/O Lines, Data Carried Over Three LVDS Serial Links†



NOTE: 4≤M≤10, where M is the multiplex/multiplier ratio set by M1 through M5.

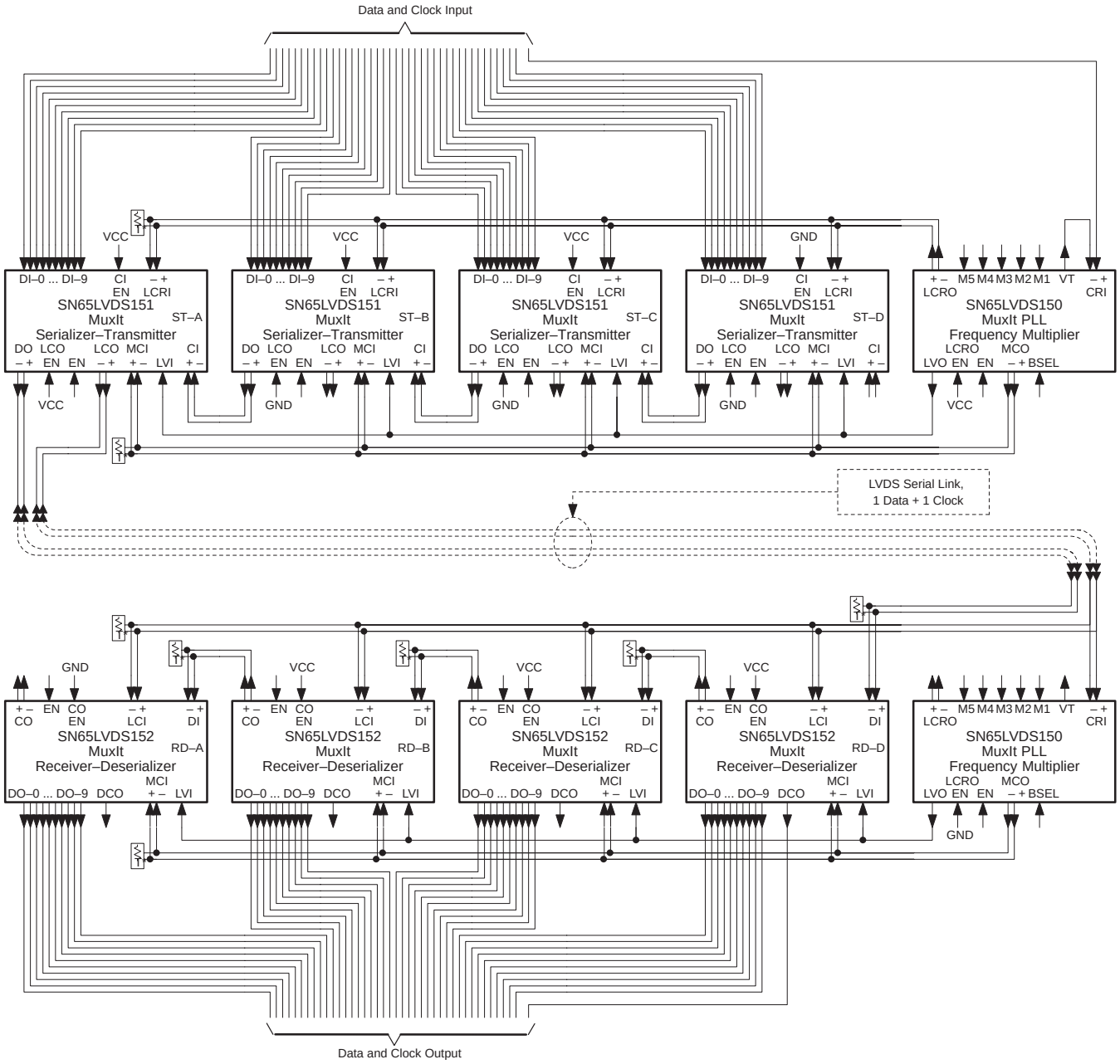
Figure 34. MuxIt Configuration for 12 to 30 Bits of Parallel Data on Three Links

† The aggregate data rate (data clock × parallel width) is too high for a single LVDS link.

Table 8. Input-to-Output Bit Map for Very-Wide Very-Fast System, 4 to 10 Parallel I/O Lines, Data Carried Over Three LVDS Serial Links

INPUTS	OUTPUTS				
	M = 4	M = 6	M = 8	M = 9	M = 10
DI-0A	DO-6A	DO-4A	DO-2A	DO-1A	DO-0A
DI-1A	DO-7A	DO-5A	DO-3A	DO-2A	DO-1A
DI-2A	DO-8A	DO-6A	DO-4A	DO-3A	DO-2A
DI-3A	DO-9A	DO-7A	DO-5A	DO-4A	DO-3A
DI-4A	Invalid	DO-8A	DO-6A	DO-5A	DO-4A
DI-5A	Invalid	DO-9A	DO-7A	DO-6A	DO-5A
DI-6A	Invalid	Invalid	DO-8A	DO-7A	DO-6A
DI-7A	Invalid	Invalid	DO-9A	DO-8A	DO-7A
DI-8A	Invalid	Invalid	Invalid	DO-9A	DO-8A
DI-9A	Invalid	Invalid	Invalid	Invalid	DO-9A
DI-0B	DO-6B	DO-4B	DO-2B	DO-1B	DO-0B
DI-1B	DO-7B	DO-5B	DO-3B	DO-2B	DO-1B
DI-2B	DO-8B	DO-6B	DO-4B	DO-3B	DO-2B
DI-3B	DO-9B	DO-7B	DO-5B	DO-4B	DO-3B
DI-4B	Invalid	DO-8B	DO-6B	DO-5B	DO-4B
DI-5B	Invalid	DO-9B	DO-7B	DO-6B	DO-5B
DI-6B	Invalid	Invalid	DO-8B	DO-7B	DO-6B
DI-7B	Invalid	Invalid	DO-9B	DO-8B	DO-7B
DI-8B	Invalid	Invalid	Invalid	DO-9B	DO-8B
DI-9B	Invalid	Invalid	Invalid	Invalid	DO-9B
DI-0C	DO-6C	DO-4C	DO-2C	DO-1C	DO-0C
DI-1C	DO-7C	DO-5C	DO-3C	DO-2C	DO-1C
DI-2C	DO-8C	DO-6C	DO-4C	DO-3C	DO-2C
DI-3C	DO-9C	DO-7C	DO-5C	DO-4C	DO-3C
DI-4C	Invalid	DO-8C	DO-6C	DO-5C	DO-4C
DI-5C	Invalid	DO-9C	DO-7C	DO-6C	DO-5C
DI-6C	Invalid	Invalid	DO-8C	DO-7C	DO-6C
DI-7C	Invalid	Invalid	DO-9C	DO-8C	DO-7C
DI-8C	Invalid	Invalid	Invalid	DO-9C	DO-8C
DI-9C	Invalid	Invalid	Invalid	Invalid	DO-9C

7.6 A System With 32 to 40 Parallel I/O Lines, Data Carried Over One LVDS Serial Link



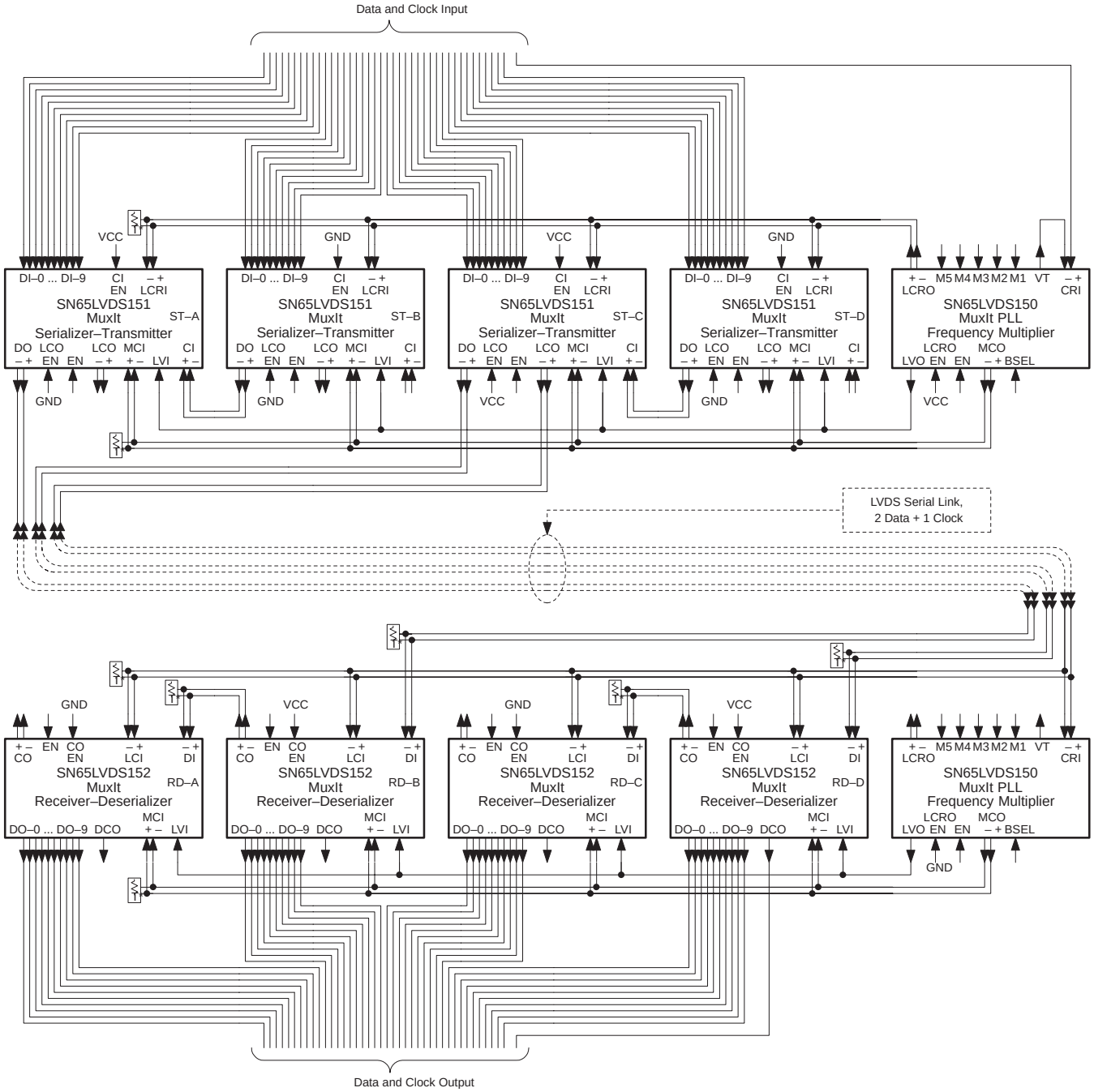
NOTE: 32≤M≤40, where M is the multiplex/multiplier ratio set by M1 through M5.

Figure 35. MuxIt Configuration for 32 to 40 Bits of Parallel Data on One Link

Table 9. Input-to-Output Bit Mapping for Very-Very-Wide Slow-Speed System, 32 to 40 Parallel I/O Lines, Data Carried Over One LVDS Serial Link

INPUTS	OUTPUTS				
	M = 32	M =34	M = 36	M = 38	M = 40
DI-0A	DO-8A	DO-6A	DO-4A	DO-2A	DO-0A
DI-1A	DO-9A	DO-7A	DO-5A	DO-3A	DO-1A
DI-2A	DO-0B	DO-8A	DO-6A	DO-4A	DO-2A
DI-3A	DO-1B	DO-9A	DO-7A	DO-5A	DO-3A
DI-4A	DO-2B	DO-0B	DO-8A	DO-6A	DO-4A
DI-5A	DO-3B	DO-1B	DO-9A	DO-7A	DO-5A
DI-6A	DO-4B	DO-2B	DO-0B	DO-8A	DO-6A
DI-7A	DO-5B	DO-3B	DO-1B	DO-9A	DO-7A
DI-8A	DO-6B	DO-4B	DO-2B	DO-0B	DO-8A
DI-9A	DO-7B	DO-5B	DO-3B	DO-1B	DO-9A
DI-0B	DO-8B	DO-6B	DO-4B	DO-2B	DO-0B
DI-1B	DO-9B	DO-7B	DO-5B	DO-3B	DO-1B
DI-2B	DO-0C	DO-8B	DO-6B	DO-4B	DO-2B
DI-3B	DO-1C	DO-9B	DO-7B	DO-5B	DO-3B
DI-4B	DO-2C	DO-0C	DO-8B	DO-6B	DO-4B
DI-5B	DO-3C	DO-1C	DO-9B	DO-7B	DO-5B
DI-6B	DO-4C	DO-2C	DO-0C	DO-8B	DO-6B
DI-7B	DO-5C	DO-3C	DO-1C	DO-9B	DO-7B
DI-8B	DO-6C	DO-4C	DO-2C	DO-0C	DO-8B
DI-9B	DO-7C	DO-5C	DO-3C	DO-1C	DO-9B
DI-0C	DO-8C	DO-6C	DO-4C	DO-2C	DO-0C
DI-1C	DO-9C	DO-7C	DO-5C	DO-3C	DO-1C
DI-2C	DO-0D	DO-8C	DO-6C	DO-4C	DO-2C
DI-3C	DO-1D	DO-9C	DO-7C	DO-5C	DO-3C
DI-4C	DO-2D	DO-0D	DO-8C	DO-6C	DO-4C
DI-5C	DO-3D	DO-1D	DO-9C	DO-7C	DO-5C
DI-6C	DO-4D	DO-2D	DO-0D	DO-8C	DO-6C
DI-7C	DO-5D	DO-3D	DO-1D	DO-9C	DO-7C
DI-8C	DO-6D	DO-4D	DO-2D	DO-0D	DO-8C
DI-9C	DO-7D	DO-5D	DO-3D	DO-1D	DO-9C
DI-0D	DO-8D	DO-6D	DO-4D	DO-2D	DO-0D
DI-1D	DO-9D	DO-7D	DO-5D	DO-3D	DO-1D
DI-2D	Invalid	DO-8D	DO-6D	DO-4D	DO-2D
DI-3D	Invalid	DO-9D	DO-7D	DO-5D	DO-3D
DI-4D	Invalid	Invalid	DO-8D	DO-6D	DO-4D
DI-5D	Invalid	Invalid	DO-9D	DO-7D	DO-5D
DI-6D	Invalid	Invalid	Invalid	DO-8D	DO-6D
DI-7D	Invalid	Invalid	Invalid	DO-9D	DO-7D
DI-8D	Invalid	Invalid	Invalid	Invalid	DO-8D
DI-9D	Invalid	Invalid	Invalid	Invalid	DO-9D

7.7 A System With 24 to 40 Parallel I/O Lines, Data Carried Over Two LVDS Serial Links†



NOTE: 12≤M≤20, where M is the multiplex/multiplier ratio set by M1 through M5.

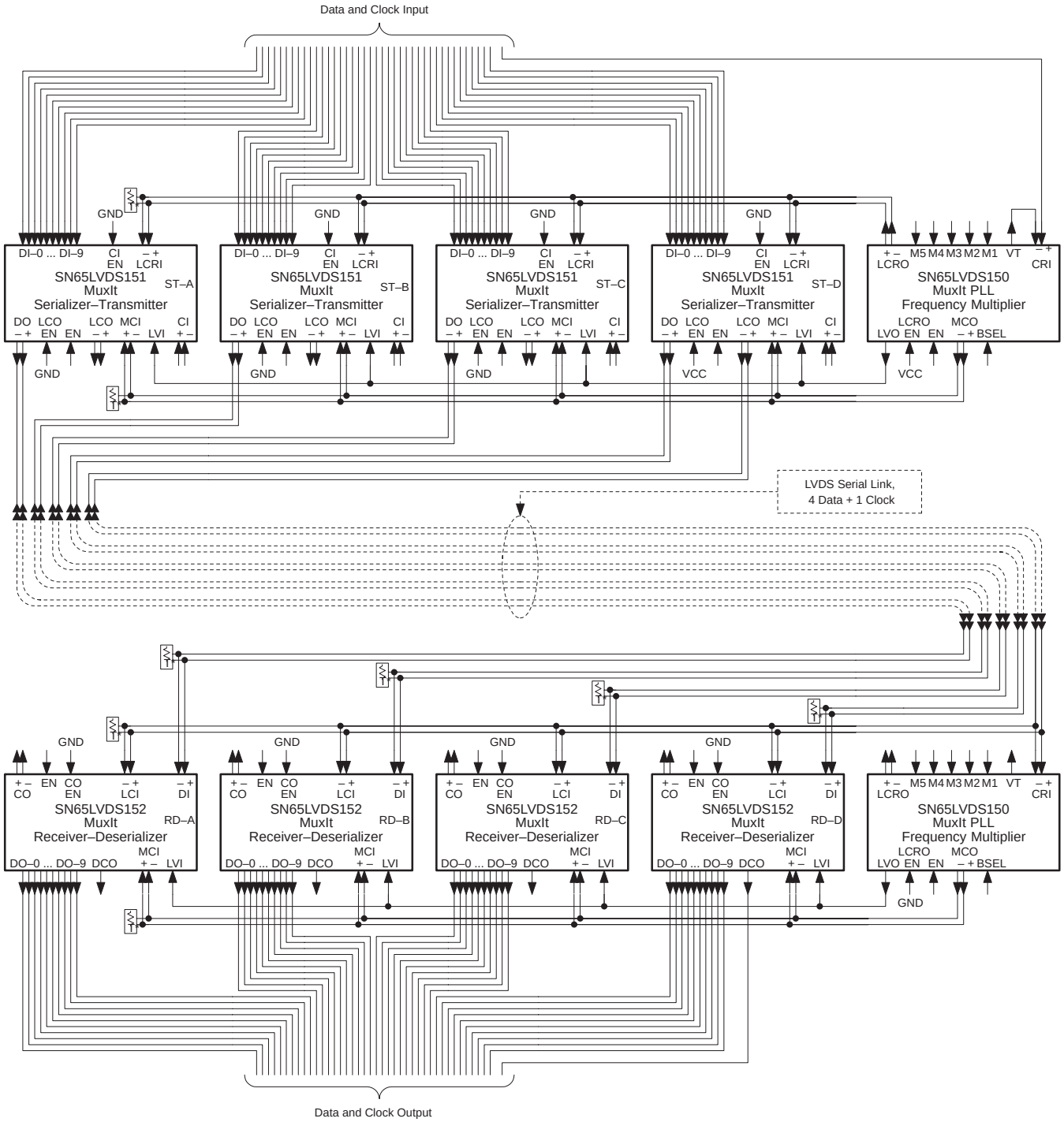
Figure 36. MuxIt Configuration for 24 to 40 Bits of Parallel Data on Two Links

† The aggregate data rate (data clock × parallel width) is too high for one LVDS link.

Table 10. Input-to-Output Bit Mapping for Very-Very-Wide Moderate-Speed System, 12 to 20 Parallel I/O Lines, Data Carried Over Two LVDS Serial Links

INPUTS	OUTPUTS								
	M = 12	M = 13	M = 14	M = 15	M = 16	M = 17	M = 18	M = 19	M = 20
DI-0A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A	DO-3A	DO-2A	DO-1A	DO-0A
DI-1A	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A	DO-3A	DO-2A	DO-1A
DI-2A	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A	DO-3A	DO-2A
DI-3A	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A	DO-3A
DI-4A	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A	DO-4A
DI-5A	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A	DO-5A
DI-6A	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A	DO-6A
DI-7A	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A	DO-7A
DI-8A	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A	DO-8A
DI-9A	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B	DO-9A
DI-0B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B	DO-0B
DI-1B	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B	DO-1B
DI-2B	Invalid	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B	DO-2B
DI-3B	Invalid	Invalid	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B	DO-3B
DI-4B	Invalid	Invalid	Invalid	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B	DO-4B
DI-5B	Invalid	Invalid	Invalid	Invalid	DO-9B	DO-8B	DO-7B	DO-6B	DO-5B
DI-6B	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9B	DO-8B	DO-7B	DO-6B
DI-7B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9B	DO-8B	DO-7B
DI-8B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9B	DO-8B
DI-9B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9B
DI-0A	DO-8C	DO-7C	DO-6C	DO-5C	DO-4C	DO-3C	DO-2C	DO-1C	DO-0C
DI-1A	DO-9C	DO-8C	DO-7C	DO-6C	DO-5C	DO-4C	DO-3C	DO-2C	DO-1C
DI-2A	DO-0D	DO-9C	DO-8C	DO-7C	DO-6C	DO-5C	DO-4C	DO-3C	DO-2C
DI-3A	DO-1D	DO-0D	DO-9C	DO-8C	DO-7C	DO-6C	DO-5C	DO-4C	DO-3C
DI-4A	DO-2D	DO-1D	DO-0D	DO-9C	DO-8C	DO-7C	DO-6C	DO-5C	DO-4C
DI-5A	DO-3D	DO-2D	DO-1D	DO-0D	DO-9C	DO-8C	DO-7C	DO-6C	DO-5C
DI-6A	DO-4D	DO-3D	DO-2D	DO-1D	DO-0D	DO-9C	DO-8C	DO-7C	DO-6C
DI-7A	DO-5D	DO-4D	DO-3D	DO-2D	DO-1D	DO-0D	DO-9C	DO-8C	DO-7C
DI-8A	DO-6D	DO-5D	DO-4D	DO-3D	DO-2D	DO-1D	DO-0D	DO-9C	DO-8C
DI-9A	DO-7D	DO-6D	DO-5D	DO-4D	DO-3D	DO-2D	DO-1D	DO-0D	DO-9C
DI-0B	DO-8D	DO-7D	DO-6D	DO-5D	DO-4D	DO-3D	DO-2D	DO-1D	DO-0D
DI-1B	DO-9D	DO-8D	DO-7D	DO-6D	DO-5D	DO-4D	DO-3D	DO-2D	DO-1D
DI-2B	Invalid	DO-9D	DO-8D	DO-7D	DO-6D	DO-5D	DO-4D	DO-3D	DO-2D
DI-3B	Invalid	Invalid	DO-9D	DO-8D	DO-7D	DO-6D	DO-5D	DO-4D	DO-3D
DI-4B	Invalid	Invalid	Invalid	DO-9D	DO-8D	DO-7D	DO-6D	DO-5D	DO-4D
DI-5B	Invalid	Invalid	Invalid	Invalid	DO-9D	DO-8D	DO-7D	DO-6D	DO-5D
DI-6B	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9D	DO-8D	DO-7D	DO-6D
DI-7B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9D	DO-8D	DO-7D
DI-8B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9D	DO-8D
DI-9B	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DO-9D

7.8 A System With 16 to 40 Parallel I/O Lines, Data Carried Over Four LVDS Serial Links†



NOTE: 4≤M≤10, where M is the multiplex/multiplier ratio set by M1 through M5.

Figure 37. MuxIt Configuration for 16 to 40 Bits of Parallel Data on Four Links

† The aggregate data rate (data clock × parallel width) is too high for fewer than four LVDS links.

Table 11. Input-to-Output Bit Map for Very-Very-Wide High-Speed System, 16 to 40 Parallel I/O Lines, Data Carried Over Four LVDS Serial Links

INPUTS	OUTPUTS				
	M = 4	M = 6	M = 8	M = 9	M = 10
DI-0A	DO-6A	DO-4A	DO-2A	DO-1A	DO-0A
DI-1A	DO-7A	DO-5A	DO-3A	DO-2A	DO-1A
DI-2A	DO-8A	DO-6A	DO-4A	DO-3A	DO-2A
DI-3A	DO-9A	DO-7A	DO-5A	DO-4A	DO-3A
DI-4A	Invalid	DO-8A	DO-6A	DO-5A	DO-4A
DI-5A	Invalid	DO-9A	DO-7A	DO-6A	DO-5A
DI-6A	Invalid	Invalid	DO-8A	DO-7A	DO-6A
DI-7A	Invalid	Invalid	DO-9A	DO-8A	DO-7A
DI-8A	Invalid	Invalid	Invalid	DO-9A	DO-8A
DI-9A	Invalid	Invalid	Invalid	Invalid	DO-9A
DI-0B	DO-6B	DO-4B	DO-2B	DO-1B	DO-0B
DI-1B	DO-7B	DO-5B	DO-3B	DO-2B	DO-1B
DI-2B	DO-8B	DO-6B	DO-4B	DO-3B	DO-2B
DI-3B	DO-9B	DO-7B	DO-5B	DO-4B	DO-3B
DI-4B	Invalid	DO-8B	DO-6B	DO-5B	DO-4B
DI-5B	Invalid	DO-9B	DO-7B	DO-6B	DO-5B
DI-6B	Invalid	Invalid	DO-8B	DO-7B	DO-6B
DI-7B	Invalid	Invalid	DO-9B	DO-8B	DO-7B
DI-8B	Invalid	Invalid	Invalid	DO-9B	DO-8B
DI-9B	Invalid	Invalid	Invalid	Invalid	DO-9B
DI-0C	DO-6C	DO-4C	DO-2C	DO-1C	DO-0C
DI-1C	DO-7C	DO-5C	DO-3C	DO-2C	DO-1C
DI-2C	DO-8C	DO-6C	DO-4C	DO-3C	DO-2C
DI-3C	DO-9C	DO-7C	DO-5C	DO-4C	DO-3C
DI-4C	Invalid	DO-8C	DO-6C	DO-5C	DO-4C
DI-5C	Invalid	DO-9C	DO-7C	DO-6C	DO-5C
DI-6C	Invalid	Invalid	DO-8C	DO-7C	DO-6C
DI-7C	Invalid	Invalid	DO-9C	DO-8C	DO-7C
DI-8C	Invalid	Invalid	Invalid	DO-9C	DO-8C
DI-9C	Invalid	Invalid	Invalid	Invalid	DO-9C
DI-0D	DO-6D	DO-4D	DO-2D	DO-1D	DO-0D
DI-1D	DO-7D	DO-5D	DO-3D	DO-2D	DO-1D
DI-2D	DO-8D	DO-6D	DO-4D	DO-3D	DO-2D
DI-3D	DO-9D	DO-7D	DO-5D	DO-4D	DO-3D
DI-4D	Invalid	DO-8D	DO-6D	DO-5D	DO-4D
DI-5D	Invalid	DO-9D	DO-7D	DO-6D	DO-5D
DI-6D	Invalid	Invalid	DO-8D	DO-7D	DO-6D
DI-7D	Invalid	Invalid	DO-9D	DO-8D	DO-7D
DI-8D	Invalid	Invalid	Invalid	DO-9D	DO-8D
DI-9D	Invalid	Invalid	Invalid	Invalid	DO-9D

8 Conclusion

This application report has described the MuxIt family of general-purpose integrated-circuit building blocks for data transmission serializer-deserializer subsystems. The individual component devices were examined, and guidelines were provided for designing MuxIt systems. System design guidelines included PC-board layout considerations, LVDS terminations, interface signal-routing constraints, timing margins, and input-output bitmapping.

9 Bibliography

There is a wide range of LVDS devices and related application materials available to assist in the design and development of LVDS interfaces. The following list contains pertinent data sheets and other application materials:

1. *MuxIt PLL Frequency Multiplier*, Data Sheet, Texas Instruments Literature Number SLLS443
2. *MuxIt Serializer/Transmitter*, Data Sheet, Texas Instruments Literature Number SLLS444
3. *MuxIt Receiver/Deserializer*, Data Sheet, Texas Instruments Literature Number SLLS445
4. *The MuxIt Evaluation Module (EVM)*, User's Guide, Texas Instruments Literature Number SLLU023
5. *Interface Circuits for TIA/EIA–644 (LVDS)*, Application Report, Texas Instruments Literature Number SLLA038
6. *Low Voltage Differential Signaling (LVDS) Evaluation Module (EVM)*, User's Guide, Texas Instruments Literature Number SLLA033
7. *Low–Voltage Differential Signaling*, Application Report, Texas Instruments Literature Number SLLA014
8. *LVDS Devices Operate With V_{CC} = 2.5 Vdc*, Application Report, Texas Instruments Literature Number SLLA046
9. *LVDS in Harsh Environments With the Next Generation Receivers From TI*, Application Report, Texas Instruments Literature Number SLLA061
10. *LVDS Multidrop Connections*, Application Report, Texas Instruments Literature Number SLLA054
11. *Measuring Crosstalk in LVDS Systems*, Application Report, Texas Instruments Literature Number SLLA064
12. *Performance of LVDS With Different Cables*, Application Report, Texas Instruments Literature Number SLLA053
13. *Slew Rate Control of LVDS Circuits*, Application Report, Texas Instruments Literature Number SLLA0

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