SN65LV1021/SN65LV1212- SN65LV1023/SN65LV1224 10:1 Serializer/Deserializer Evaluation Board (EVM)

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ABSTRACT

This application report focuses on the use and construction of a serializer/deserializer evaluation module (EVM) for evaluating the characteristics of SN65LV1021/SN65LV1212 serializers, and SN65LV1023/SN65LV1224 deserializer devices. This document provides guidance on proper use by showing possible device configurations and test modes. It also provides design, layout, and schematic information, including specific construction recommendations. Information in this guide can be used to assist the customer in choosing the optimal design methods and materials in designing a complete system.

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1 EVM Description

The BLINK EVM provides a vehicle to evaluate the operation and conduct characterization measurements of Texas Instruments SN65LVDS1021/1023 serializer and SN65LVDS1212/1224 deserializer devices.

The board is set up to permit the independent evaluation of either serializer or deserializer devices through the use of external equipment to match the requirements of each device.

Design of the board provides for easy configuration changes that permit joining the devices at either their parallel ports or serial ports, thus providing a vehicle for the evaluation of that interface between the two devices.

Standard SMA and RJ45 female connectors are provided to permit the serializing and data recovery evaluation using standard interface cables of various lengths. A patch resistor network permits selection of either set of connectors, as appropriate for evaluation and measurement of these signals.

Standard board shorting jumpers can be used on the standard board-pin headers to interconnect deserializer and serializer devices. These same headers provide a vehicle to interface with logic analyzers and pattern generators for the purpose of device evaluation.

Other configuration jumpers on the board permit the establishment of independent measurement loops for supply currents and/or injection of separate external supply sources. Figure 1 is a block diagram of the board.

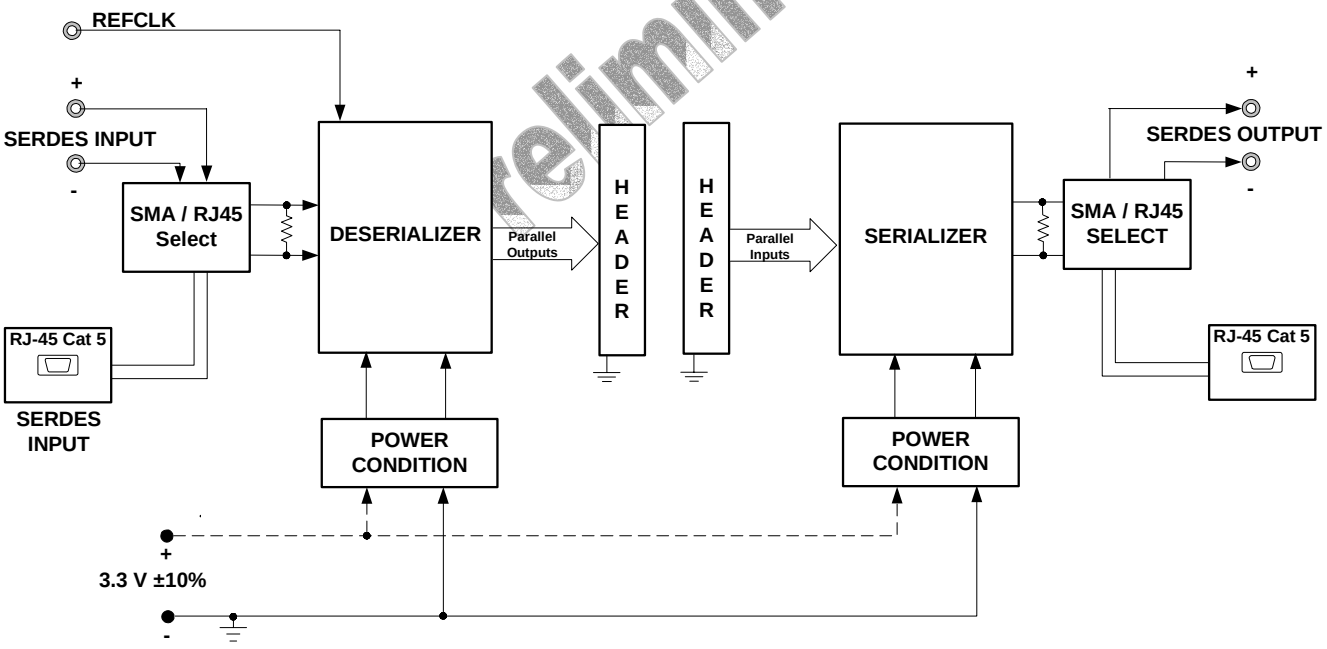


Figure 1. B LINK Evaluation Board Block Diagram

2 Board Configuration

The B LINK evaluation board can be configured to permit independent evaluation of serializer and deserializer devices, either individually or joined with each other as a pair. It is possible, through jumper configurations, to set up the board to perform dc and ac measurements such that only one of the devices is active while the other is taken totally out of the circuit without being an influence on the other. Devices can easily be interfaced with each other by joining their high-speed side through cables or their low speed side through jumpers. This feature can be used to evaluate how the devices interface with each other or to evaluate each device as a stand-alone through the use of external laboratory test equipment.

Table 1 corresponds to the way the board was configured prior to shipment from TI.

Figure 2 is a simplified pictorial representation of the EVM and can be used to locate rapidly the jumper locations on the board.

Deserializer receive outputs and serializer receive inputs are routed to terminal blocks BS3 and BS4, respectively. Figure 3 provides additional information that can be used to identify signal distribution on the BS3 and BS4 terminal blocks. These terminal blocks provide a mechanism for connection to stimulus and measurement systems for parallel data timing control and evaluation. These terminal blocks provide a means for simple interconnection of deserializer and serializer devices. The signals on these headers are set such that all pins on the outer edges of the header-group are grounds, while all signals output from the deserializer and input to the serializer are contained in the inner rows. This setup is easily connected to stimulus-measurement and data-pattern-generation hardware, and it also allows for the easy interconnect of the parallel busses through standard 0.1-inch shorting jumpers.

3 EVM Board Preparation

Prior to applying power to the board, verify that the jumpers are properly installed as shown in Table 1. Figure 2 provides a simplified top view of the EVM that can be used to assist in rapidly locating these jumpers on the board.

Table 1. Jumper Installation Table

Jumper	Default	Pin #	Function	Description
JP1	Installed	2-3	RCLK_R/F	Deserializer's RCLK strobe edge selection (high selects rising edge)
JP2	Installed	2-3	REN	Logic high input enables deserializer's parallel output bus and RCLK into low-impedance states.
JP3	Installed	2-3	/PWRDN	Deserializer power-down control. Set to high input to maintain device active.
JP5	Installed	2-3	TCLK_R/F	Serializer's TCLK strobe edge selection (high selects rising edge)
JP6	Installed	1-2	DEN	Serializer output bus three-state control. Set high enables serializer's output pair.
JP7	Installed	1-2	/PWRDN	Deserializer power-down control. Set to high input to maintain device active.
JP8	OFF		SYNC2	Logic high initiates serializer's 1024 sync patterns for rapid synchronization. May be connected to the serializer LOCK to speed synchronization.
JP9	OFF		SYNC1	
JP11	Installed	1-2	Power	Digital power in to deserializer pins 12 and 23
JP12	Installed	1-2	Power	Digital power in to serializer pins 27 and 28
JP13	Installed	1-2	Power	Analog power in to deserializer pins 4 and 11
JP14	Installed	1-2	Power	Analog power in to serializer pins 17 and 26
JP15	Installed	1-2	TITEN1	TI factory test enable 1
JP16	Installed	2-3	TITEN2	TI factory test enable 2.
BS3>BS4	Installed	BS3-26>BS4-1	Data0	ROUT0 > DIN0
BS3>BS4	Installed	BS3-25>BS4-2	Data1	ROUT1 > DIN0
BS3>BS4	Installed	BS3-24>BS4-3	Data2	ROUT2 > DIN0
BS3>BS4	Installed	BS3-23>BS4-4	Data3	ROUT3 > DIN0
BS3>BS4	Installed	BS3-22>BS4-5	Data4	ROUT4 > DIN0
BS3>BS4	Installed	BS3-21>BS4-6	Data5	ROUT5 > DIN0
BS3>BS4	Installed	BS3-20>BS4-7	Data6	ROUT6 > DIN0
BS3>BS4	Installed	BS3-19>BS4-8	Data7	ROUT7 > DIN0
BS3>BS4	Installed	BS3-18>BS4-9	Data8	ROUT8 > DIN0
BS3>BS4	Installed	BS3-17>BS4-10	Data9	ROUT9 > DIN0
BS3>BS4	OFF	BS3-16>BS4-11	Lock	Deserializer LOCK test point
BS3>BS4	Installed	BS3-15>BS4-12	Clock	ROUT0 > DIN0
BS3>BS4	OFF	BS3-14>BS4-13	Ground	Ground

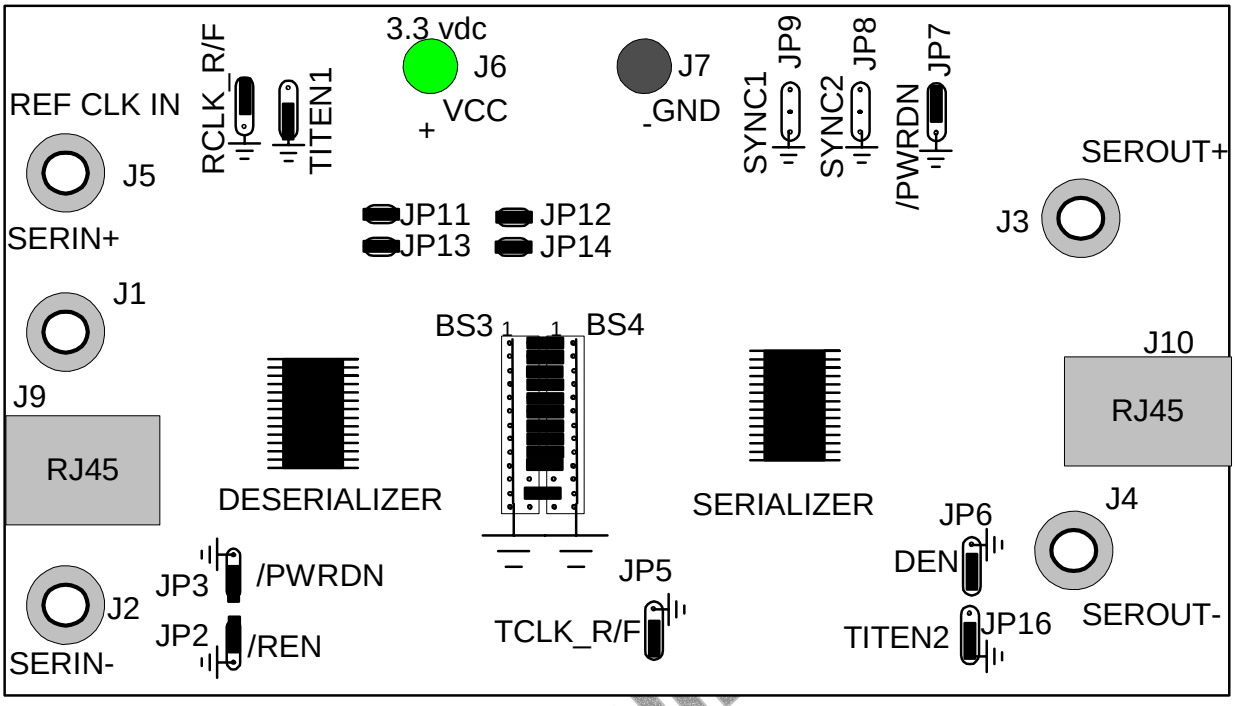


Figure 2. B LINK EVM Default Jumpers Setup

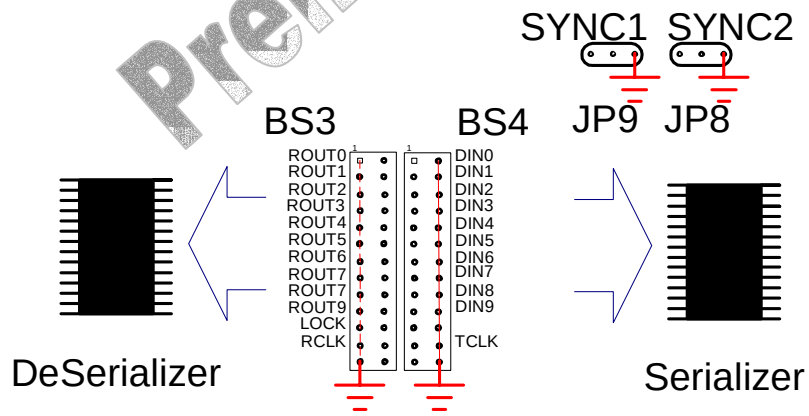


Figure 3. Deserializer-Serializer Interconnect Detail

4 Power Connections

The B LINK EVM can be powered from an ordinary dc laboratory-bench power supply using a pair of power supply cables with standard plug banana jacks.

1. Set the power supply at 3.3 Vdc ±10%.
2. It is recommended that before making the power supply connections, the power supply be turned off.
3. Connect a 3.3-V jumper plug to EVM connector J6.
4. Apply a ground connection to EVM connector J7.
5. An LED located between the terminal posts indicates the application of power.

It is advisable to keep the power supply turned off until all SMA connections are made to preclude the accidental shorting of coaxial connectors with power jacks.

5 Basic Evaluation Setup

As shipped, the board is ready for operation. Jumpers interconnecting BS3 and BS4 have been installed to connect the parallel output bus of the deserializer to the parallel input bus of the serializer. Jumpers J11-J14 provide digital and analog power to both devices. The board is configured to be in the active powered state with all data outputs enabled, and jumpers installed for selecting the rising edge of the strobe clock. Once interconnected with test equipment as shown in Figure 4, the board is ready for power application and evaluation.

The basic setup takes serial data applied from a serial BERT to the J1 and J2 SMA connectors (or alternatively to the RJ45 connector J6)[1]; data and clock, recovered at the deserializer device, are output on the BS3 header. Jumpers interconnecting BS3 and BS4 provide parallel data and clock to the serializer device, where data is serialized and output at the J3 and J4 SMA connectors.

An optional jumper wire, interconnecting the deserializer's LOCK output from BS3-12 to pin 2 on JP8 or JP9, can be used to activate the rapid sync-pattern generation option in the serializer. The LOCK signal goes active-low, indicating that the deserializer has locked onto the input data stream and commanding the serializer to resume normal data transmission.

Care should be taken to use matched-electrical-length cables for matched-pair signals from and to a BERT or scope to ensure the quality of measurements.

[1]Zero-Ω steering resistors installed in R2, R4, R19, and R21 steer data to the SMA connectors. Moving these resistors to R1, R2, R19, and R20 makes serial data available at the RJ45 connectors. Installing shorting bars in all resistor positions makes the signal available at both; however, reflections may occur on serial data streams due to stub effects.

This setup can be used to verify the functional integrity and operation of the devices, evaluate lock time, jitter transfer and most timing parameters. The setup can with little modification be converted to effect other jitter evaluation and timing measurements for both serializer and deserializer devices.

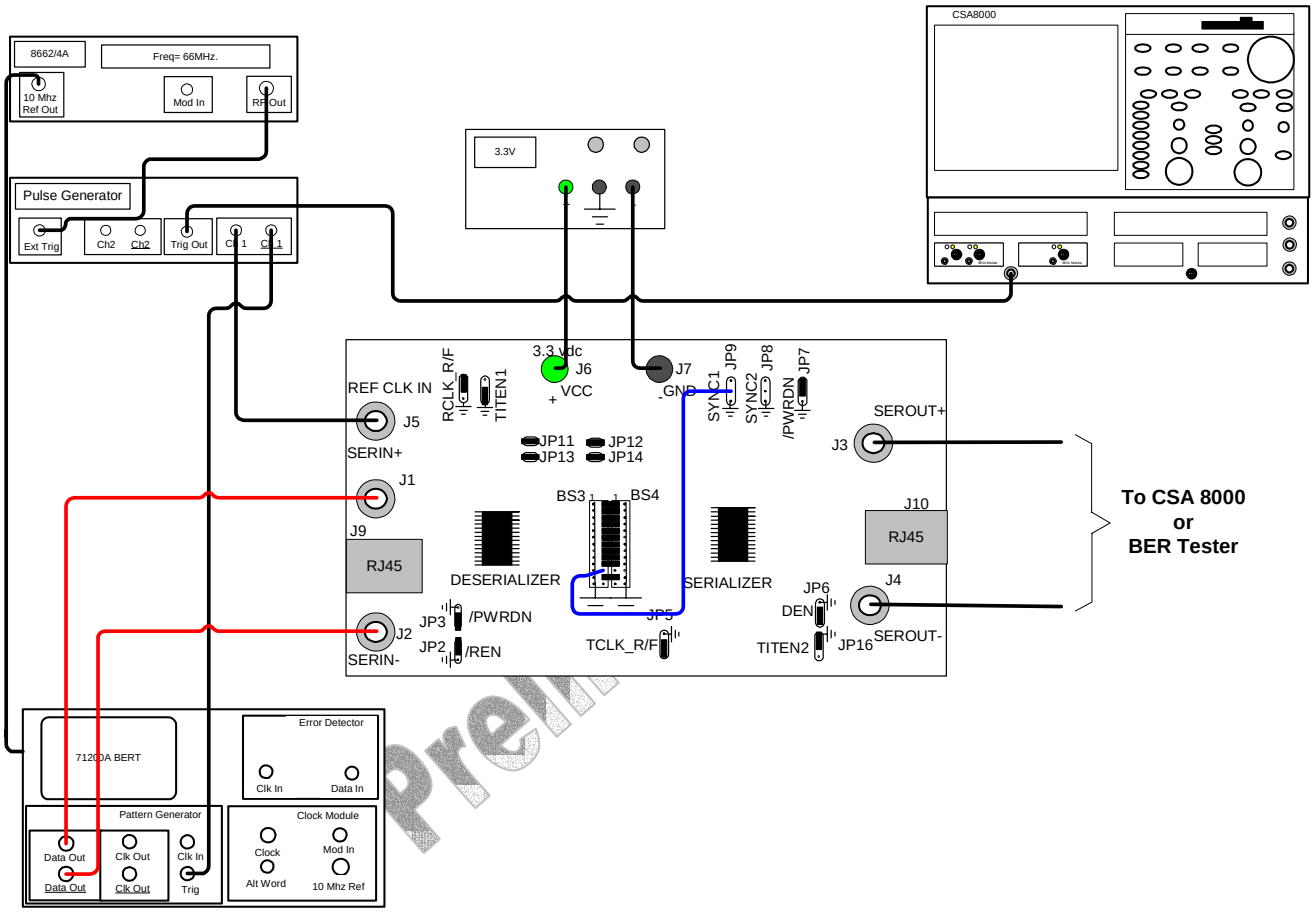


Figure 4. Basic Evaluation Setup

6 Optional Configurations and Measurements

The fact that each device operational pin is accessible at test pins or connectors facilitates the evaluation of each device as a stand-alone unit under test to evaluate other device parameters such as setup, hold, lock time, etc., without influence from the other device.

7 Parallel Input and Output Data

The jumpers that interconnect the parallel busses of deserializer and serializer devices in the as-shipped configuration are removed. Parallel data inputs to the serializer device are provided at the BS4 header by an external parallel data generator. Data is serialized by the serializer device and externally directed to the deserializer inputs through SMA or RJ45 connections. The verification loop is completed by monitoring the parallel output of the serializer at the BS3 header through a pattern verification unit that compares sent and received data.

1. Jumpers that connect BS3 to BS4 are removed.
2. BS4 parallel input data to the serializer is connected to a parallel pattern generator.
3. BS3 parallel outputs are connected to a parallel pattern verification unit, Set-up /Hold Setup
4. Loopback of the serial ports is effected by connecting J3 to J1 and J4 to J2 using matched-length 50-Ω cables.[2]

8 Serializer Jitter Measurements

Patterns can be introduced in several ways to provide input to the serializer.

- In the EVM default configuration setup, a serial data stream can be provided to create these patterns.
- If all the jumpers interconnecting the BS3 and BS4 headers are removed, data and clock can be provided at BS4.
- An alternative method of generating fixed patterns when a parallel-data generation capability is not available is to use jumpers from the data input connection to the adjacent ground posts on the BS4 header. Because all data inputs to the serializer are pulled up, only those bits where a jumper is installed to the adjacent ground become zero.

9 Average Current Measurements

Power is individually steered to serializer and deserializer devices by installed jumpers JP11-JP14 as described in Table 1. In order to make individual device current measurements, jumpers can be replaced with current probes or with small-value resistors to facilitate the current calculation. These jumpers are located on top of the board immediately below the power connectors to the EVM. Once jumpers are replaced with current-measurement hardware, appropriate data patterns and speed selection must be provided to validate those measurements.

10 PC Board Physical Layout Recommendations

Serializer and deserializer devices should be provided with separate analog and digital power planes; these can coexist within the same PWB layer and share a common ground where the analog and digital ground pins of each device are joined.

[2] Optionally, a standard Ethernet 10/100 BASE-TX NIC-to-hub cable can loop the serial stream from RJ45 connector J10 to connector J9.

In order to provide good power supply bypass and provide for the demand currents whose harmonics may reach into the multi-gigaHertz region, an appropriate power distribution system should be designed containing tantalum capacitors. High-quality local capacitors should be placed in the immediate vicinity of power pins. Good interplane capacitance should be provided on this system utilizing power cores 0.005 inches or less.

All active signals should be laid out as 50-Ω characteristic impedance traces using high-speed layout techniques.

Serial data pairs should be electrically matched to within 0.050 inches, and laid out to provide a 100-Ω differential common-mode impedance. A 100-Ω termination resistor should be placed as close as possible to the sourcing pins on the serializer and to the receiving pins of the deserializer devices.

Figure 5 provides a graphical representation of the layout requirements for these devices.

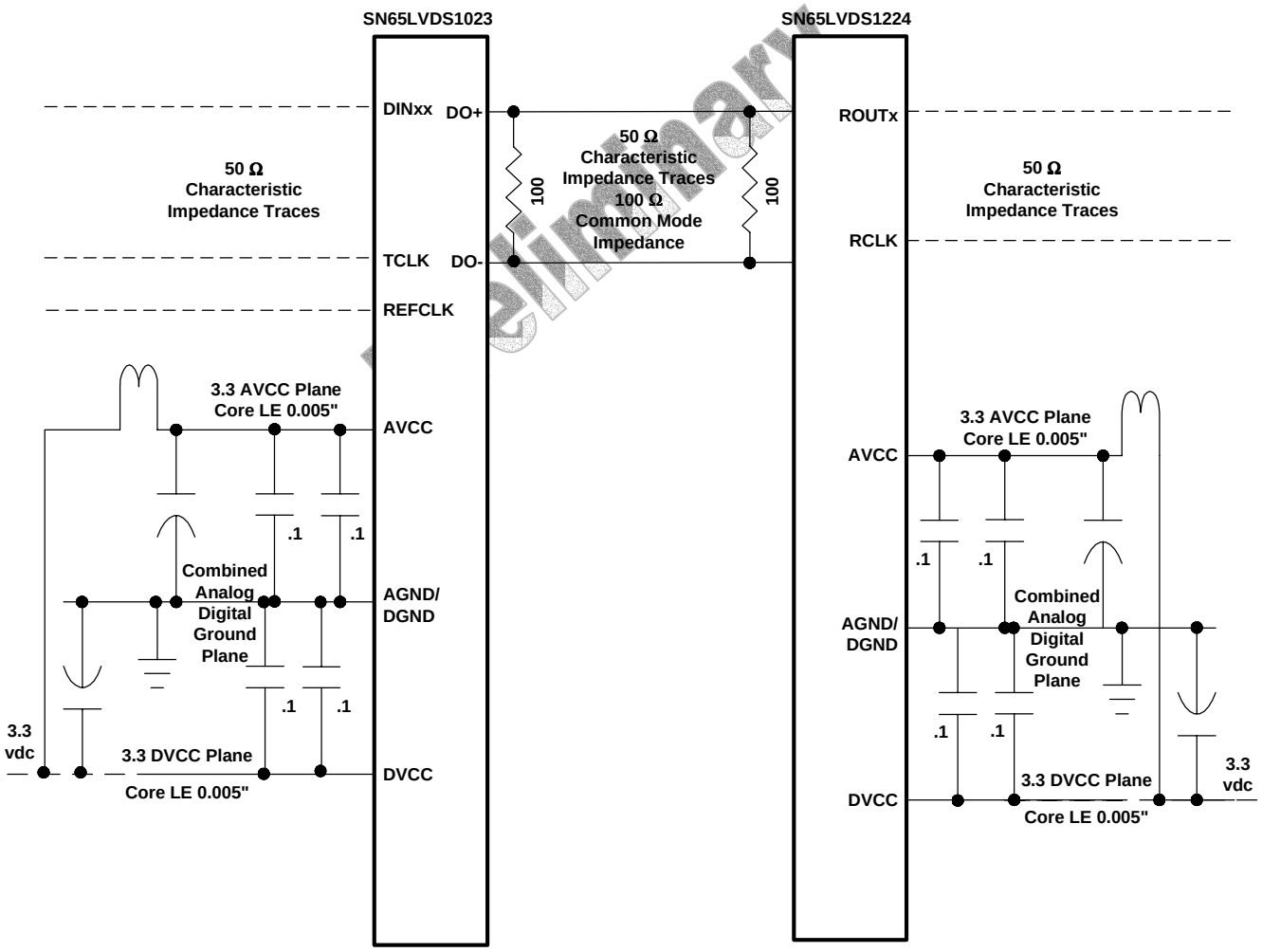
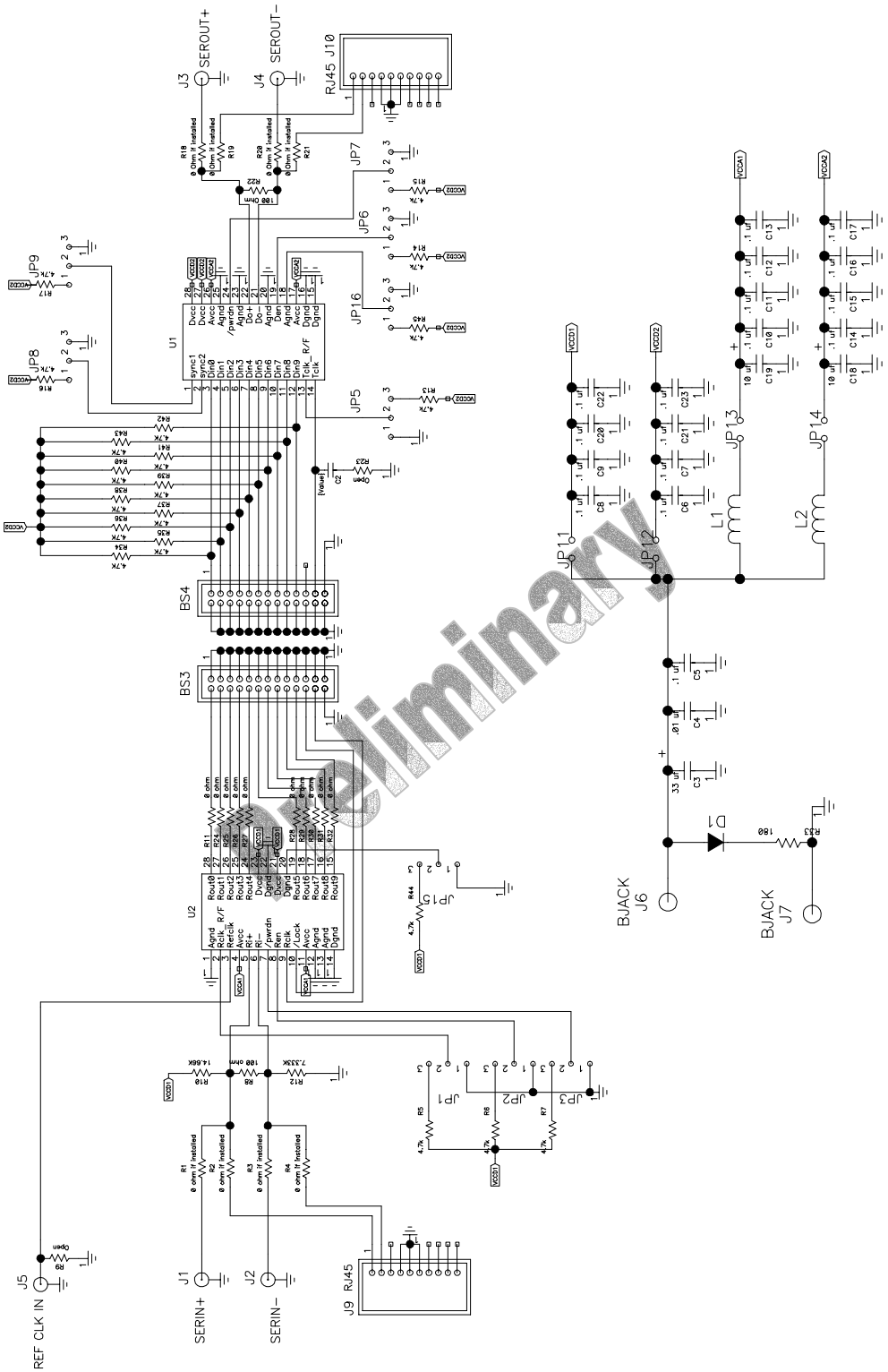


Figure 5. SN65LVDS1023/SN65LVDS1224 Layout Requirements Diagram

Appendix A. BLINK Schematics



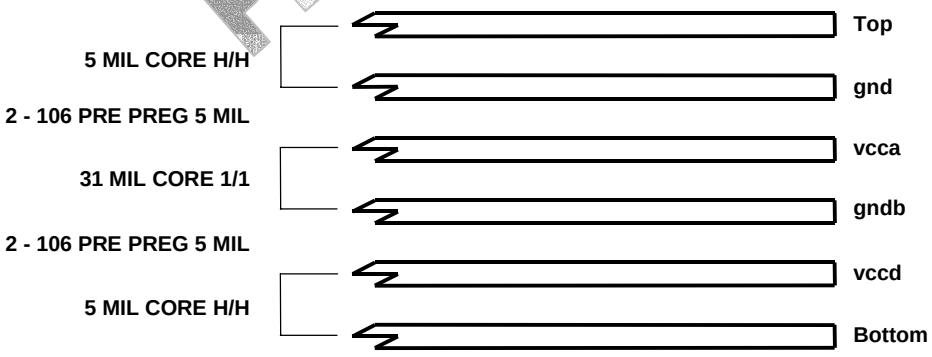
Appendix B. EVM Board Design Stackup

General Notes:

1. All fabrication items must meet or exceed best industry practice.
2. Laminate material, copper clad GETEK, E_r 3.9
3. Copper weight: 1 oz
4. Finished board thickness 0.060” ±0.005”
5. Position accuracy: ±0.0015”
6. Warp and twist not to exceed 0.020”
7. Controlled impedance layer 1: 50 Ω ±5%
8. Controlled impedance trace width: 8.6 mils

Process Notes

1. Copper plating to be 0.001”minimum in plated-through holes
2. Circuitry on outer layers to be plated with 7–12-µin gold over 50–80-µin nickel
3. Solder mask both sides: green enthoine
4. Apply white silkscreen on top and bottom side of board using separate artwork.

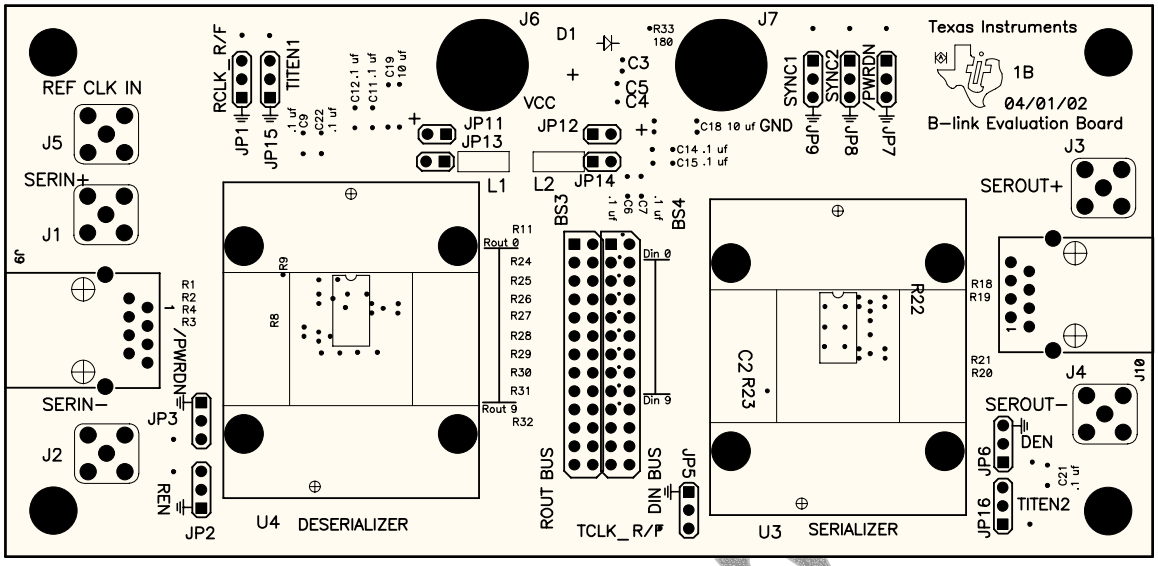


Layer Stackup

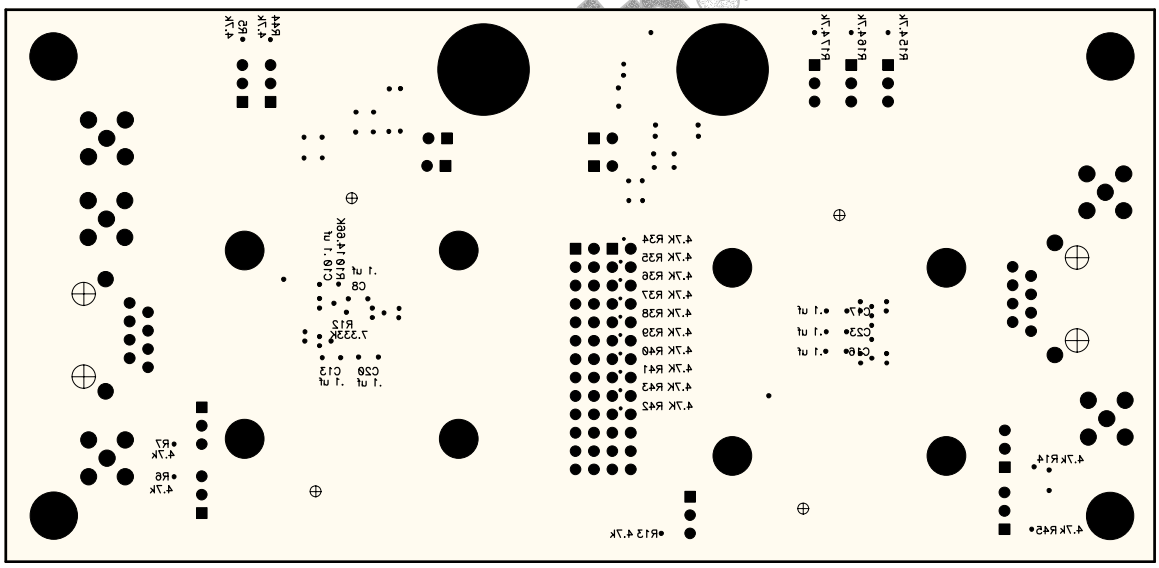
5. Top layer (layer 1) 50-Ω trace using GETEK, 5-mil-thick ½ oz. copper. W1 = 10 mil, w = 9.5 mil
6. Trace calculations contained in this drawing are solely for design purposes to establish a starting point for board requirements.

7. Board shop may adjust trace width to account for process and maintain controlled impedance where required.

EVM Board Design – Top and Bottom Silkscreens

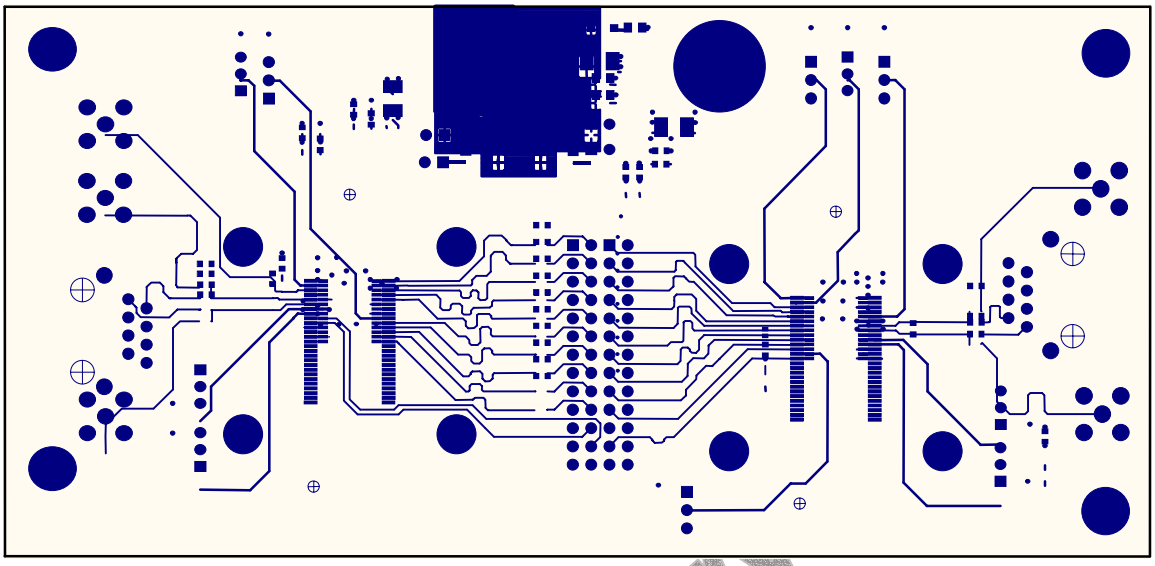


Top Silkscreen

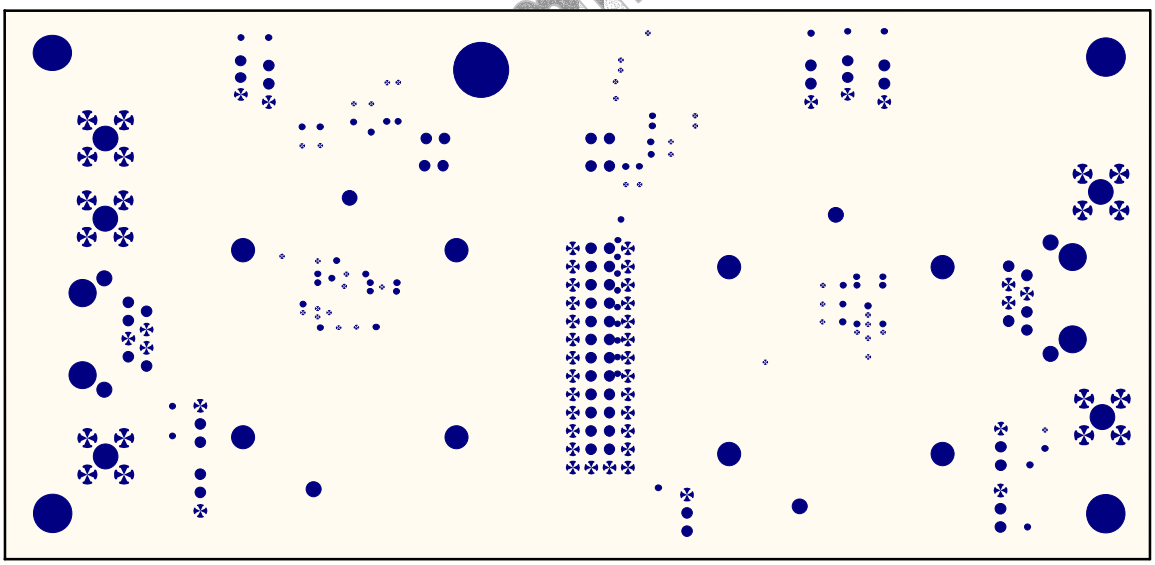


Bottom Silkscreen

EVM Board Design – Top Layer and Ground Layer

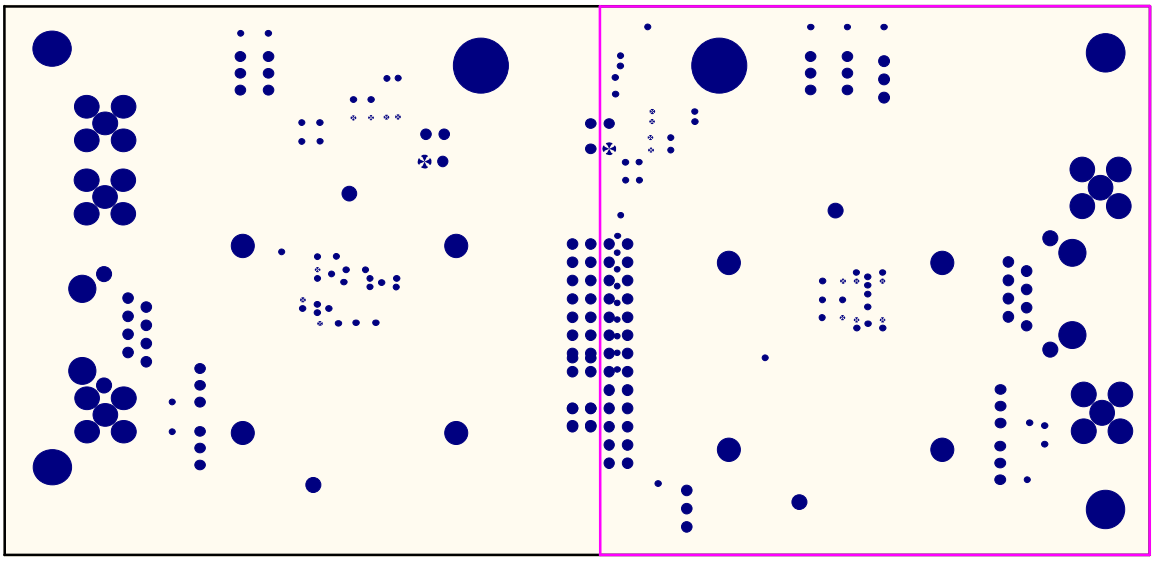


Top

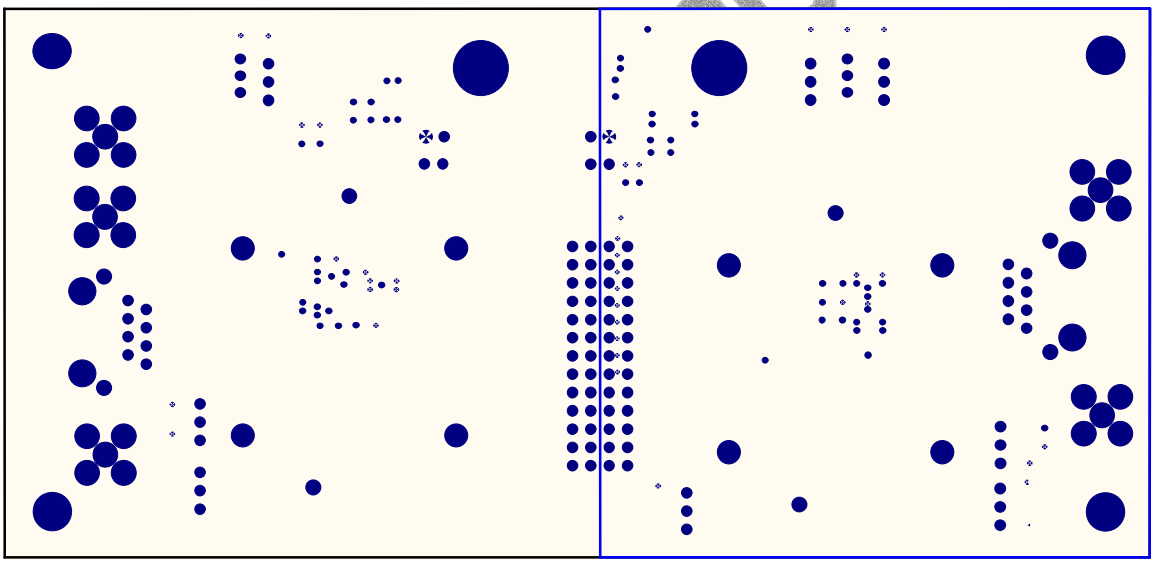


Ground

EVM Board Design Power Voltage Layers

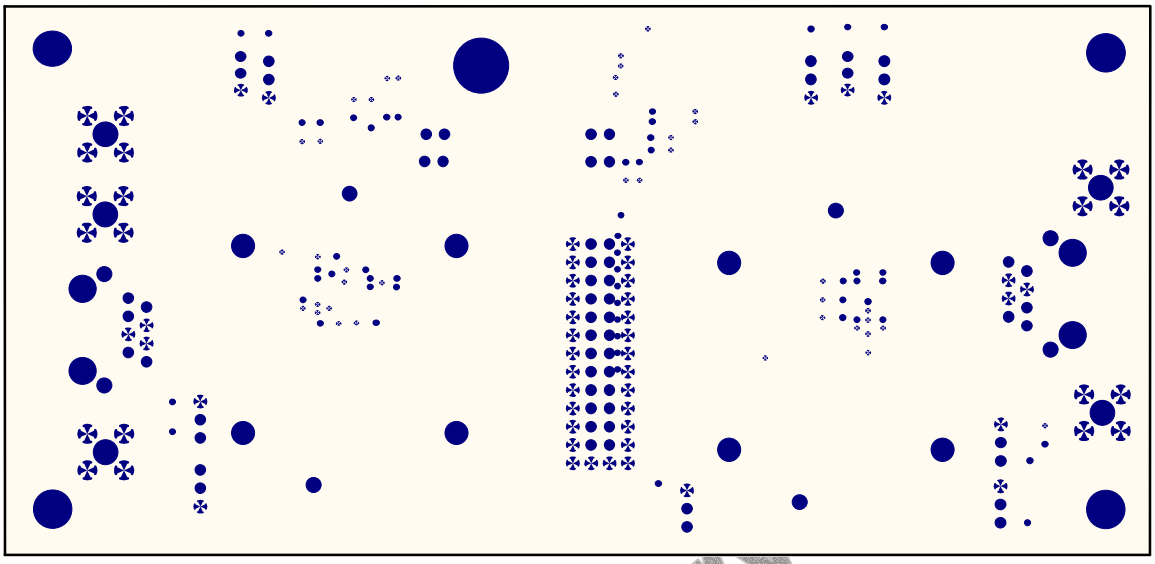


VCCA

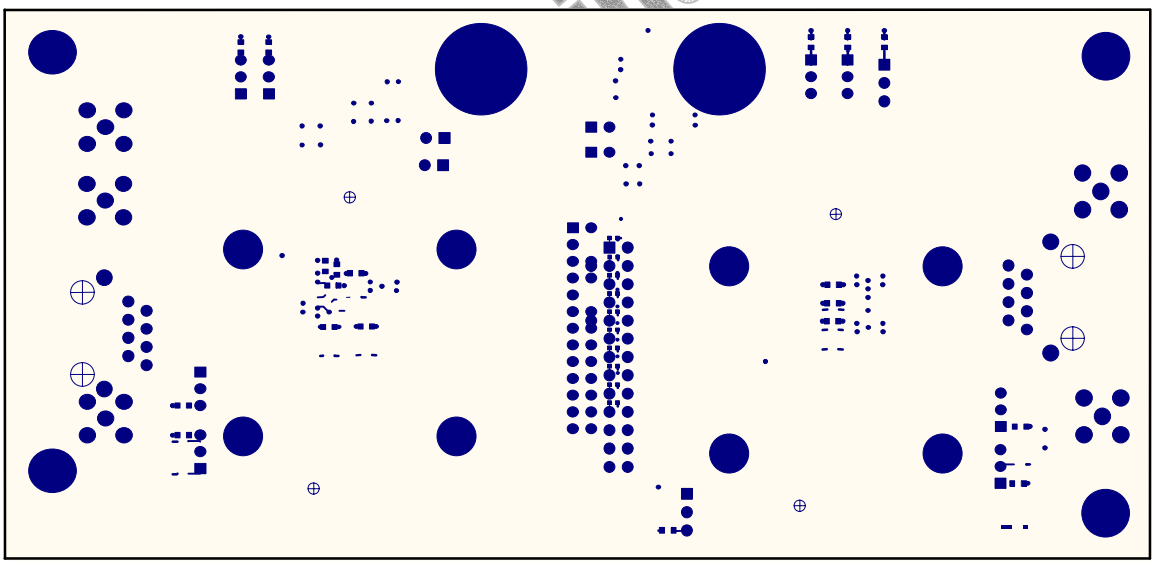


VCCD

EVM Board Design – Ground Layer and Bottom Layer



Ground Layer



Bottom Layer

Appendix C. BLINK EVM BOM

Count	Component Name	Ref. Des.	Value	Description
2	BERG13	BS3, BS4		DIN bus and ROUT bus 26-pin headers
2	C1210+	C18–C19	10 µF	
1	C0402	C2		Not installed
1	C1210+	C3	33 µF	
1	C0805	C4	0.01 µF	
1	C0805	C5	0.1 µF	
16	C0603	C6–C23	0.1 µF	0603 ceramic capacitor
1	DigiKey 160-1174-2-ND	D1		Diode, light emitting
5	SMA TOP	J1, J2, J3, J4, J5		SMA high speed male connector
2	BJACK	J6–J7		Power jacks
2	RJ45	J9, J10		
2	JUMPER3	JP1,JP2, JP5–JP9, JP15, JP16		3-pin, 0.1” × 0.025” male header material
4	JUMPER2	JP11–JP14		2-pin 0.1” × 0.025” male header material
2	DigiKey HI1806T600R-00	L1, L2		Inductor, 1806
1	R0603	R10	14.66 kΩ	
10	R0603	R11, R24–R32	0.0 Ω	Resistor, SMD 0603
1	R0603	R12	7.333 kΩ	
4	R0603	R1-R4, R18–R21	0 Ω	Resistor, SMD 0603 (*installation-specific, signal steering requirements)
1	R0805	R33	180 Ω	
10	R0402	R34–R43	4.7 kΩ	Resistor, SMD 0402
10	R603	R5-R7, R13–R17, R44, R45		
2	R0603	R8, R22	100 Ω	
2	R0603	R9, R23		No resistors installed
2		U2		SOC-B66-05-04-0 U1
1	SN65LV1021 or SN65LV1023	U3		Serializer, SN65LVD1021 100–400-MB operation. SN65LVD1023 400–660-Mb operation
1	SN65LV1212 or SN65LV1224	U4		Deserializer, SN65LVD1212 100–400-MB operation. SN65LVD1224 400–660-Mb operation

* If SMA connectors are used for serial data (preferred configuration), install 0-Ω resistors in R1, R3, R18, R20. Do not install R2, R4, R19, and R21. If RJ45 connectors are used for serial data, do not install R1, R3, R18, or R20. Install 0-Ω resistors in R2, R4, R19, and R21.

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