Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices

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ABSTRACT

Every USB high-speed application must support a data rate of 480 Mb/s within ±500 ppm (479.760 Mb/s to 480.240 Mb/s) to comply with the Universal Serial Bus Specification Revision 2.0. For Texas Instruments USB 2.0 devices, it is recommended that the clocks of the USB 2.0 devices be derived from an external crystal. Evaluation of the properties of the crystal will ensure that the selected crystal will function as expected in the system. Capacitor selection and layout can also affect the operation of the crystal. This application note details the preferred crystal properties, as well as guidelines for capacitor selection and board layout.

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Introduction

TI USB 2.0 devices require an external 24.000 MHz source connected between the X1 (XTAL1) and X2 (XTAL2) pins on the PHY or PHY portion of an integrated device to provide the reference for the internal oscillator circuit. The internal oscillator circuit drives a phase lock loop (PLL) circuit that generates all the clocks required by the device for transmission and resynchronization of data at high speed and full speed data rates. TI recommends using a crystal as the clock source.

The maximum total system tolerance is specified by the Universal Serial Bus Specification Revision 2.0 as a high speed data rate of 480.00 Mb/s nominal with a required bit rate accuracy of ±500 ppm (parts per million) or ±0.05%. This ±500 ppm includes all potential error sources: frequency tolerance, temperature, aging, crystal capacitive loading, board layout, and production run variations. When using a crystal, two potential sources of degradation in data rate accuracy mentioned in the USB 2.0 specification can be disregarded: initial (power up) frequency accuracy and supply voltage on the oscillator.

The clock input generated by the crystal must have a better accuracy rate than ±500 ppm for the PHY to function correctly. Excessive variations in the clock can result in data corruption on the USB bus. The following is a discussion of the requirements for a crystal used with TI USB 2.0 devices, as well as recommendations for board layout. Points discussed include:

- Frequency
- Mode of operation
- Crystal circuit type
- Frequency tolerance
- Frequency stability
- Aging (Long Term Stability)
- Load capacitance
- Maximum equivalent series resistance
- Layout recommendations

Crystal Specifications

Frequency

The required frequency of oscillation for the crystal is 24.000 MHz.

Mode of Operation

The recommended oscillation mode of operation for the crystal is fundamental mode. This simplifies the resonant circuit that is required for the crystal. In addition, fundamental crystals typically have lower equivalent series resistance (ESR) than third overtone crystals.

Crystal Circuit Type

The recommended type of circuit for the crystal is parallel resonance. A parallel resonant crystal is designed to operate with a specified load capacitance in the oscillator feedback loop. Since any board will have some load capacitance due to board layout, parallel resonant crystals are the obvious choice. They are also more commonly used and thus easier to find and purchase. Parallel resonant crystals depend on the combination of the reactance of the capacitors and the crystal itself to accomplish the phase shift necessary to ensure crystal oscillation at the expected load resonant frequency.

Frequency Tolerances

Frequency tolerance is the maximum allowable deviation from the nominal crystal frequency at a specified temperature, usually 25°C. The recommended frequency tolerance of the crystal over the manufacturing process is ±50 ppm. The maximum acceptable frequency tolerance of the crystal over the manufacturing process is ±100 ppm.

NOTE:

The total system frequency tolerance from the crystal, the load capacitors, the capacitive load of the board, the capacitive load of the device pins, variation over temperature, variation with age, and the circuitry of the PHY must be less than ±500 ppm. For this reason, the individual tolerance for the crystal must be ≤ ±100 ppm.

Frequency Stability

Frequency stability refers to the allowable deviation from nominal crystal frequency over a specified temperature range. This deviation is measured from the nominal frequency at 25°C. The recommended frequency stability or temperature tolerance of the crystal is ±50 ppm. The maximum acceptable frequency stability or temperature tolerance of the crystal is ±100 ppm.

Aging (Long-Term Stability)

Aging refers to the cumulative change in frequency of oscillation experienced by a crystal over time. Excessive drive level, various thermal effects, wire fatigue and frictional wear can exacerbate aging effects. Aging rates are stated in ppm per year units. The recommended value for long term stability or drift is approximately ±5 ppm.

Load Capacitance

The load capacitance refers to all capacitances in the oscillator feedback loop. It is equal to the amount of capacitance seen between the terminals of the crystal in the circuit. For parallel resonant mode circuits, the correct load capacitance is necessary to ensure the oscillation of the crystal within the expected parameters. It is important to account for all sources of capacitance when calculating the correct values for the discrete capacitor components, C_{L1} and C_{L2}, for a design.

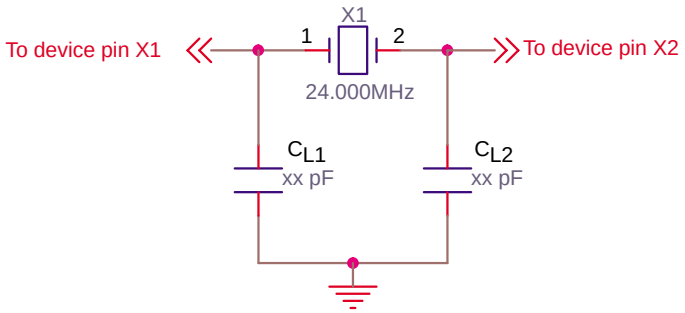

Figure 1. Parallel Resonant Mode Circuit Sample Schematic

For a parallel resonant circuit configuration, calculate the discrete capacitor values using:

$$C_{Load} = \left(\frac{C_{L1} C_{L2}}{C_{L1} + C_{L2}} \right) + C_{Board} + C_{Device}$$

Where:

C_{device} = the X1 input to X2 output capacitance of the device plus any parasitic capacitances (usually 2 pF – 5 pF).

C_{board} = the capacitance of the PCB etch (usually 3 pF – 6 pF).

$C_{L1} = C_{L2}$ = The load capacitors should be of equal value for optimum symmetry. Capacitor tolerances in the range of 5% should be sufficiently accurate for these designs.

If a lower load capacitance than that specified by the crystal specification is used, the oscillation frequency of the crystal will increase. If a higher load capacitance than the one specified is used, the oscillation frequency of the crystal will decrease. The oscillator of the USB device may have difficulty driving a large load capacitance, avoid crystals that specify large load capacitances.

Maximum Equivalent Series Resistance

Crystals can be modeled by a series circuit of an inductor, a capacitor, and a resistor along with a shunt capacitor in parallel with all three. The value of the resistor is known as the equivalent series resistance (ESR) and it relates to bulk losses inside the quartz crystal. The ESR quantifies the loading of the crystal and the resonance circuit seen at the oscillator pins of the USB device. In general, a smaller ESR is better since the oscillator of the USB device may have difficulty driving a large load. The specified maximum ESR should not be more than 50 Ohms unless a very low load capacitance, $C_{LOAD,}$ is specified (< 10 pF).

Layout Recommendations

A good layout of the crystal circuit ensures the correct frequency from the crystal, minimizes the noise introduced into the PLL, and reduces any circuit emissions.

- The crystal and the load capacitors should be located as close as possible to one another, minimizing the loop area created by the combination of the three components. Smaller loop area decreases the effect of the resonant current that flows in the circuit.
- The crystal unit should then be placed as close as possible to the PHY X1 and X2 pins to minimize etch lengths.

Summary

To summarize the crystal specifications:

- Frequency: 24.000 MHz
- Mode of operation: fundamental
- Crystal circuit type: parallel resonant
- Frequency Tolerance: ±50 ppm (maximum: ±100 ppm)
- Frequency Stability: ±50 ppm (maximum: ±100 ppm)
- Aging (Long Term Stability): ±5 ppm per year
- Maximum Equivalent Series Resistance: 50 Ω (100 Ω, if C_{L1} and C_{L2} <10 pF)

References

- Application Report: Selection and Specification of Crystal for Texas Instruments IEEE 1394 Physical Layers by Burke Henehan.
- Crystek Crystals Corporation web page (**www.crystek.com**).
- Universal Serial Bus Specification Revision 2.0

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