Differences Between the Intel 21152 and the PCI2250

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ABSTRACT

This application report describes the functional difference between the Intel 21152 and the TI PCI2250. The PCI2250 is a 32-bit PCI-to-PCI bridge that was designed to be pin-to-pin compatible with the Intel 21152. The PCI2250 can also be configured to a TI specific mode that has additional capabilities.

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1 Intel Mode

In Intel mod, the PCI2250 is functionally equivalent to the Intel 21152. The PCI2250 also has several additional configuration registers that add expanded capabilities. The PCI2250 is PCI Bus Power Management 1.0 compliant in Intel mode.

1.1 Device/Vendor ID

For the PCI2250, the device ID needs to be changed to AC23h and the vendor ID needs to be changed to 104Ch.

1.2 TI Extension Window Registers

The PCI2250 has two additional decode windows that can be programmed as either memory or I/O windows. The extension windows, unlike normal decode windows, can do positive decoding on both the primary and secondary bus. The extension windows and their control registers are listed in the Table 1.

Table 1. TI Extension Window Registers

Name	PCI Offset	Function
Extension Window Base 0	44h	Extension window 0 base address register
Extension Window Limit 0	48h	Extension window 0 limit address register
Extension Window Base 1	4Ch	Extension window 1 base address register
Extension Window Limit 1	50h	Extension window 1 limit address register
Extension Window Enable	54h	Used to enable or disable the extension windows
Extension Window Map	55h	Used to control whether the extension window is positively decoded on the primary or secondary interface

1.3 Decode Control Registers

The Primary Decode Control Register (offset 57h) and the Secondary Decode Control Register (offset 56h) are used to control how the PCI2250 decodes unclaimed transactions. These registers can be used to enable subtractive decoding, which causes the PCI2250 to claim all unclaimed transactions.

1.4 Port Decode Registers

The port decode registers allow the PCI2250 to claim or ignore transactions to commonly used I/O ports. The Port Decode Enable Register (offset 58h) is used to select which COM and LPT ports the PCI2250 will claim. The Port Decode Map Register (offset 5Ah) is used to select whether the COM and LPT ports selected in the Port Decode Enable Register are claimed or ignored.

1.5 Control and Diagnostic Registers

The PCI2250 has several additional control and diagnostic registers that can be used to control and monitor different functions. These registers are the Buffer Control Register (offset 59h), the Clockrun Control Register (offset 5B h), the Diagnostic Register (offset 5Ch), the Diagnostic Status Register (offset 5Eh), the Arbiter Request Mask (offset 62h) and the Arbiter Time-out Status Register (offset 63h). The Clockrun Control Register has no function in Intel mode.

1.6 Delayed Transaction Support

The PCI2250, unlike the Intel 21152, does not support multiple delayed transactions.

1.7 Dual Address Cycle

The PCI2250 does not support dual address cycle transactions.

1.8 Memory Write and Invalidate

The PCI2250 always converts memory write and invalidate transactions to memory write transactions. The Intel 21152 will only covert memory write and invalidate transaction to memory writes when it can not ensure that the bridge will be able to complete the entire transaction.

2 TI Mode

The TI mode of the PCI2250 allows designers additional flexibility by providing the ability to select between either compact PCI Hot-Swap support or Clockrun support. In TI mode the PCI2250 is PCI Bus Power Management 1.1 compliant.

2.1 Compact PCI Hot-Swap

When in Compact PCI Hot-Swap mode the Hot-Swap Control and Status Register (offset E6h) can be used to control the Hot-Swap functionality of the PCI2250. The PCI2250 can be set up to signal ENUM# when in this mode.

2.2 Clockrun

Clockrun is a protocol used in mobile applications that allows the PCI clock to be stopped. When in Clockrun mode, the Clockrun Control Register (offset 5Bh) is used to control how the PCI2250 handles Clockrun.

References

1. *Advanced Configuration and Power Interface (ACPI) Revision 1.0*
2. *PCI Local Bus Specification Revision 2.2*
3. *PCI Mobile Design Guide, Revision 1.0*
4. *PCI-to-PCI Bridge Architecture Specification Revision 1.1*
5. *PCI Bus Power Management Interface Specification Revision 1.1*
6. *PICMG Compact-PCI Hot Swap Specification Revision 1.0*

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