

DVI on the Motherboard Using the TFP410

Connectivity Solutions

ABSTRACT

Digital visual interface (DVI) may be thought of as a plug in card interface with significant size and complexity. It can however, be easy to implement DVI on a motherboard using the Intel 865G chipset and the TFP410 DVI transmitter. This application brief describes some considerations for designers when implementing DVI on the 865G motherboard with the TFP410.

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General Description

The Texas Instruments TFP410 is one device in a family of TI *PanelBus*[™] digital display products that simplifies digital display systems design by offering value-added flexibility and reliability to the system designer. The TFP410 is a DVI 1.0 compliant digital transmitter that supports display resolutions ranging from VGA to UXGA in 24-bit, true-color pixel format. The TFP410 can be configured to support 12-bit (dual edge) input mode for connection to the graphics chipset DVO (Intel® Digital Video Output) port. Support is provided for the TFP410 in Intel drivers.

The TFP410 combines *PanelBus*[™] circuit innovation with TI's advanced 0.18-um EPIC-5[™] CMOS process technology along with TI PowerPAD[™] package technology to achieve a reliable, low-powered, low-noise, high-speed digital solution to digital visual interfacing.

Fundamental Operation

The TFP410 is a DVI (digital visual interface) compliant digital transmitter that is used in PC and consumer electronics applications to encode and transmit T.M.D.S. encoded RGB pixel data streams. In a digital display system, a host PC or workstation contains a DVI compliant transmitter, like the TFP410. The TFP410 receives 24-bit pixel data along with appropriate control signals from the DVO port of the graphics chipset and encodes them into a high-speed low-voltage differential serial bit stream fit for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor or digital projector, requires a DVI compliant receiver like the TI TFP401 to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the display drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred. Configuration of the TFP410 is provided by I2C from the chipset. DDC for the monitor is provided from the chipset. The TFP410 supports resolutions up to UXGA (1600x1200.)

For details on the TFP410 transmitter, refer to the datasheet *TFP410, PanelBus DVI Transmitter* (literature number SLDS145).

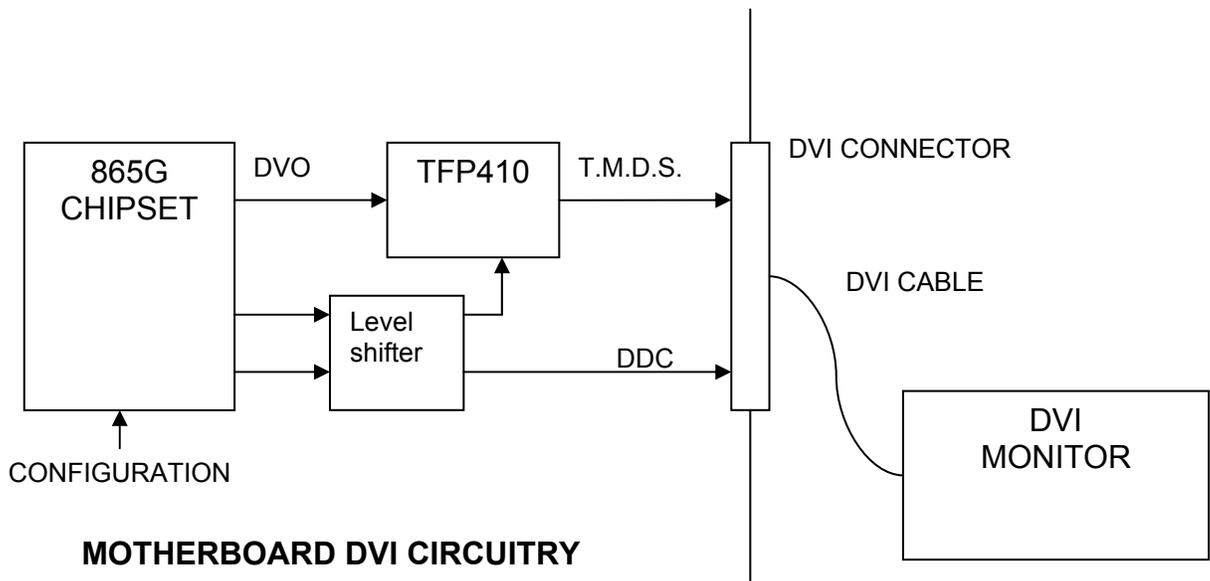


Figure 1. DVI Transmitter Implementation Diagram

Signal Connection

While the 865G chipset is referred to throughout this document, any chipset that uses the Intel Extreme Graphics driver and has a DVO port will drive the TFP410. Refer to the appropriate chipset datasheet and platform design guide.

Image data is available from the 865G chipset on the DVO lines multiplexed with the AGP signal lines. When implementing DVI on the motherboard, the AGP signals are not used. The chipset pin names use the AGP naming convention, but the DVO names are provided in the chipset datasheet. Refer to the documentation for the chipset.

Chipset Configuration

The 865G chipset must be configured for DVO output to set the function of the multiplexed AGP/DVO lines. Since the DVO mode could also drive an ADD (AGP Digital Display) card in the AGP connector, configuration specific for the TFP410 transmitter on the motherboard is needed. Table 1 shows a summary of the chipset configuration. Refer to the "Multiplexed Intel® DVO Down" section of the *Intel® 865G/865PE/865P Chipset Platform Design Guide* for specific requirements and the latest information.

Table 1. Chipset Configuration Summary

Chipset signal	Connection
ADD_DET#	Pull low with 330 ohms
ADD_ID	Pull ADD_ID7 low with 330 ohms (ADD_ID = 0x7F)
GRCOMP	Pull to 1.5V with 43.2 ohms
GSWING	Not connected
GVREF	See the <i>Voltage Reference</i> section

Image Data Connections

The TFP410 can be connected to either of the DVO ports. Refer to the following table for signal connections.

Table 2. Image Data Connections Between 865G Chipset and TFP410

TFP410 Signal	Chipset Signal	Description
DATA[11:0]	DVOx_D[11:0]	Pixel data
HSYNC	DVOx_HSYNC	Horizontal sync
VSYNC	DVOx_VSYNC	Vertical sync
DE	DVOx_BLANK#	Video data enable
IDCK+	DVOx_CLK#	Pixel clock
IDCK-	DVOx_CLK	Pixel clock

Note: The “x” in the signal name refers to either the “B” or “C” port.

The differential clock should be connected as described to provide the proper data to the TFP410 on the desired clock edge.

The trace length of data and control signals from the chipset to the transmitter should be kept as close to equal as possible. Fast edges from data sources are expected to require consideration of these traces as transmission lines. The transmitter does not provide termination of the signal lines internal to the chip. Refer to routing and termination recommendations from the chipset documentation.

Voltage Reference

The TFP410 must be operated in the low swing mode when connected to the DVO port of the chipset. The TFP410 VREF input must be at the logic threshold voltage GVREF provided to the chipset. This will be typically be provided by a divider from the logic voltage using 1-kohm resistors. Refer to the “Multiplexed Intel® DVO Down” section of the Intel® 865G/865PE/865P Chipset Platform Design Guide for specific requirements.

Configuration of the TFP410

The TFP410 is operated with I2C configuration when used with the 865G chipset and software driver. All configuration signals for the TFP410 require 3.3-V signal levels. The configuration pins should be used as shown in the following table. For additional information, refer to the TFP410 datasheet.

Table 3. TFP410 configuration pins

Signal Name	Terminal Number	Description
A[3:1]	6, 7, 8	I2C Address, tie to GND or leave open to allow to default low.
ISEL/RST	13	Derived from system reset
BSEL/SCL	15	I2C clock, refer to the I2C section
DSLE/SDA	14	I2C data, refer to the I2C section
EDGE/HTPLG	9	Hot plug input, refer to the hot plug section
PDz	10	Tie to ground
RESERVED	34	Tie to ground
DKEN	35	Tie to ground
TFADJ	19	Connect with 510 ohms to TVdd

I2C Operation

Two I2C busses are required from the chipset, one for configuration of the TFP410 and one for the DDC lines. A level shifter is required for each. MI2C_DATA and MI2C_CLK should be used for communication to the TFP410. MDVI_CLK and MDVI_DATA are used for the DDC line communications. Refer to the chipset documentation for the latest recommendations on bus use.

Level shifting

Intel has an application note describing level shifting of the I2C bus for DDC. The TI SN74TVC3010 is a 10-bit voltage clamp that can be used for these level shifters. One side of the device can be configured for the 1.5-V signals from the chipset, the other side can be used for the 3.3-V signals for the TFP410 and the 5-V signals for the DDC bus.

Hot Plug Detection

The TFP410 can support the DVI hot plug pin with the HTPLG input. A voltage limiting circuit is required to limit the high-level voltage (5 V) of the DVI connector to the maximum level for the TFP410. Various circuits could be used, the simplest may be a few resistors and diodes. The circuit should also ensure a low voltage at the TFP410 when the DVI cable is disconnected.

Interrupt support has been evolving with the drivers. If the hardware interrupt connection is desired from the TFP410, the MSEN signal should be provided to the Chipset's DVOBC_INTR# signal. This connection was not tested on the ADD card on which this application brief is based.

Unused Inputs

Unused inputs to the TFP410 such as D[23:12] should be tied high or low and not be left floating. For requirements of the chipset, refer to the 865G documentation.

Driver Support

The TFP410 is supported in the drivers for the 865G chipset starting with Intel(R) Extreme Graphics Driver 13.0. When implementing the TFP410 on the motherboard, a SPD device is not needed as on an ADD card. To provide information on the device for the driver, a Flex-AIM (.flx file) is merged into the MBI (Modular BIOS Interface) portion of the SBIOS. Contact your Intel FAE if assistance is need building the BIOS

Power Supply Decoupling

Power supply decoupling design can vary widely depending on the designer and system requirements. Various techniques can give good results. It is important to provide a low inductance path to the TFP410 power and ground pins as well as to the decoupling capacitors. It is desirable to keep high frequency noise present on the system power out of the TFP410, and also to keep any high-frequency currents generated by the TFP410 off the system supply. The following suggestions may provide guidelines for the TFP410.

Use solid ground plane. If more than one ground plane is used, tie ground planes together with as many vias as is practical. This provides a desirable return path for current. Each supply should be on separate split power planes, where each power plane should be as large an area as possible. Connect PanelBus transmitter power and ground pins and all by-pass capacitors to the appropriate power or ground plane with a via. Vias should be as fat and short as practical; the goal is to minimize the inductance.

The number and size of the decoupling capacitors required depends on the design of the circuit board. The three power supplies for the chip, DVDD, PVDD, and TVDD should be treated similarly:

Place one 0.1-uF capacitor as close as possible between each device power pin and ground.

A bulk decoupling capacitor such as a 10-uF or 22-uF tantalum capacitor should be placed on the sub-plane between the supply and 0.1-uF capacitors.

A ferrite bead should be used to separate the sub-plane from the source.

Additional capacitors may be needed depending on the size of the sub-planes and impedance of the ferrite beads and capacitors.

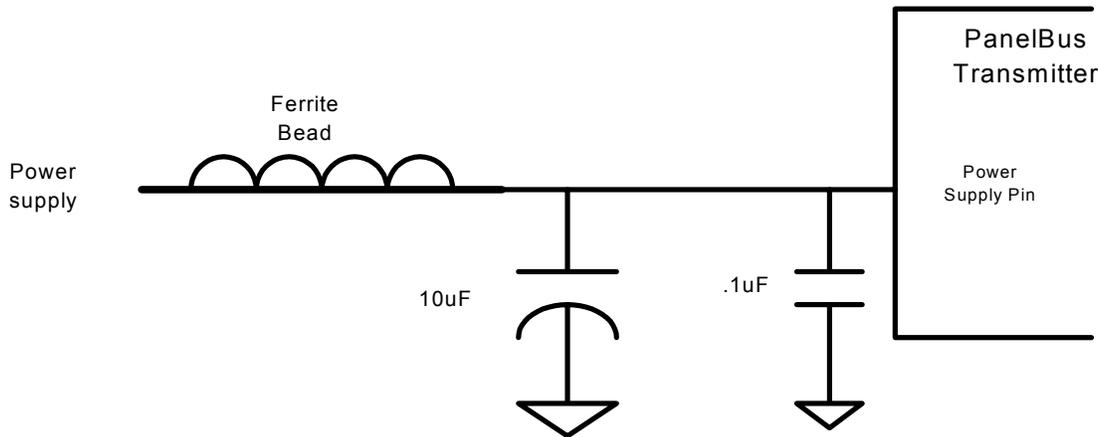


Figure 2. Power Supply Decoupling

DVI Routing High-Speed Differential Signal Traces

(TxC-, TxC+, Tx0-, Tx0+, Tx1-, Tx1+, Tx2-, Tx2+)

Trace impedance should be controlled for optimal performance, 50 ohms is recommended. Each differential pair should be equal in length and symmetrical and should have equal impedance to ground with a trace separation of 2x to 4x Height. A differential trace separation of 4X Height yields about 6% cross-talk (6% effect on impedance).

We recommend that differential trace routing should be side-by-side, though it is not important that the differential traces be tightly coupled together because tight coupling is not achievable on PCB traces. Typical ratios on PCB's are only 20-50%; 99.9% is the value of a well-balanced twisted-pair cable.

Each differential trace should be as short as possible (<2" preferably) with no 90° angles. These high-speed transmission traces should be on an outer layer with a continuous ground plane on the next plane layer.

Operation at UXGA resolution requires careful construction of the transmission lines and selection of high-quality cables and connectors.

DVI Connector Routing

Clear-out holes for connector pins should leave space between pins to allow continuous ground through the pin field. Allow enough spacing in ground plane around signal pins vias, however. Keep enough copper between vias to allow for ground current to flow between the vias. Avoid creating a large ground plane slot around the entire connector; minimizing the via capacitance is the goal.

Additional Components on DVI Lines

TxC-, TxC+, Tx0-, Tx0+, Tx1-, Tx1+, Tx2-, Tx2+ signals all route directly from the device to the DVI connector pins. Additional components are not recommended on these outputs. Most components degrade the high-speed signal edges required for satisfactory operation at higher DVI frequencies. If components are added, care must be taken to avoid stubs and capacitance from mounting pads.

Reflections can occur from the DVI connector with a second reflection from the DVI transmitter. This combination can affect the observed signal edge quality or cause symbol interference on the DVI signal. Terminations may be considered to reduce these effects, but careful impedance design, device placement, and trace routing are preferred methods. If terminations are considered, various considerations should be made.

Parallel terminations reduce the signal swing and can cause violations of the DC specifications on the DVI lines. Parallel termination also provides a low resistance DC path between the transmitter system and DVI receiver system power supplies, which can produce problems when trying to power down either system.

Series terminations may be ineffective in terminating the reflection at the transmitter since the transmitter output will still be a high impedance. However they could potentially slow the signal edge to avoid the reflection from the connector.

AC terminations prevent the DC current issues of the parallel termination; the added capacitance of the components must be balanced against the termination benefit.

If ESD protection is added to the DVI lines, the protectors should be low capacitance. Care should also be taken to insure the DVI termination voltage from the receiver does not feed through the ESD device and power up the transmitting system.

Common-mode chokes designed for DVI may provide some benefit for the system designer.

PowerPad™ Connection

The TFP410 is housed in a high-performance, thermally-enhanced, 64-terminal PAP PowerPAD. package. Use of the PowerPAD package does not require any special considerations except that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. The recommended option, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained in the following sections. Although the actual size of the exposed die pad may vary, the minimum recommended keepout area for the TFP410 is 5.9 mm x 5.9 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land varies in size, depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, (SLMA002), available via the TI Web pages at URL: <http://www.ti.com>.

For the TFP410, it is recommended that the PowerPAD be soldered to a thermal land grounded to the low-impedance ground plane of the board. This improves not only thermal performance but also the electrical grounding of the device. The recommended pad size for the grounded thermal land is 5.9mm square minimum, centered in the device land pattern. The land size must be as large as possible without shorting device signal terminals. The exposed PowerPAD may be soldered to the thermal land using standard reflow soldering techniques.

References

1. *TFP410, PanelBus DVI Transmitter* (SLDS145)
2. *Intel® 865G/865PE/865P Chipset Platform Design Guide*, Intel Corporation
3. *Intel® 865G Chipset Datasheet*, Intel Corporation
4. *Design Recommendations for Display Compatibility on Intel® Integrated Graphics Chipsets*, Intel Corporation
5. *PowerPAD Thermally Enhanced Package Application Report*, (SLMA002)
6. *Electro-static Discharge Protection of High Performance Integrated Circuits*, AP-208, pages 13-14, California Micro Devices Corporation.

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