Quad-Channel TEC Controller White Paper

September 20, 2002

Contents

Introduction

This white paper describes the design of a DSP-based control system for erbium-doped fiber amplifiers in order to stabilize the wavelength of multiple pump lasers. The platform shows a single TMS320F2812 DSP (abbreviated "F2812" throughout this document) controlling the temperature of four lasers. The analog portions of the design were chosen to minimize the temperature measurement error and maximize the efficiency of the drive to the thermoelectric cooler. The platform highlights the advantages of using a single DSP in this application over using discrete TEC controller modules:

- the ability to control the edges of the PWM signals to the TEC drivers, minimizing electrical noise;
- the ability to use the programmability of the DSP to easily handle exception processing;
- the extendibility of the design to additional TEC channels;
- the ability to add function easily to the DSP to control other aspects of the design, such as back facet diode monitoring and dynamic gain flattening filtering.

The paper concludes showing methods to add additional channels to the base design and reduce the board space of the design.

EDFA Amplification

Erbium-doped fiber amplifiers (EDFAs) are optical amplifiers used in fiber-optic systems. A typical dual-pumped EDFA is shown in Figure 1. The central feature of the amplifier is the erbium-doped fiber. Erbium is a rare-earth element that has energy levels in its atomic structure to amplify light with a wavelength of 1550 nm [1].

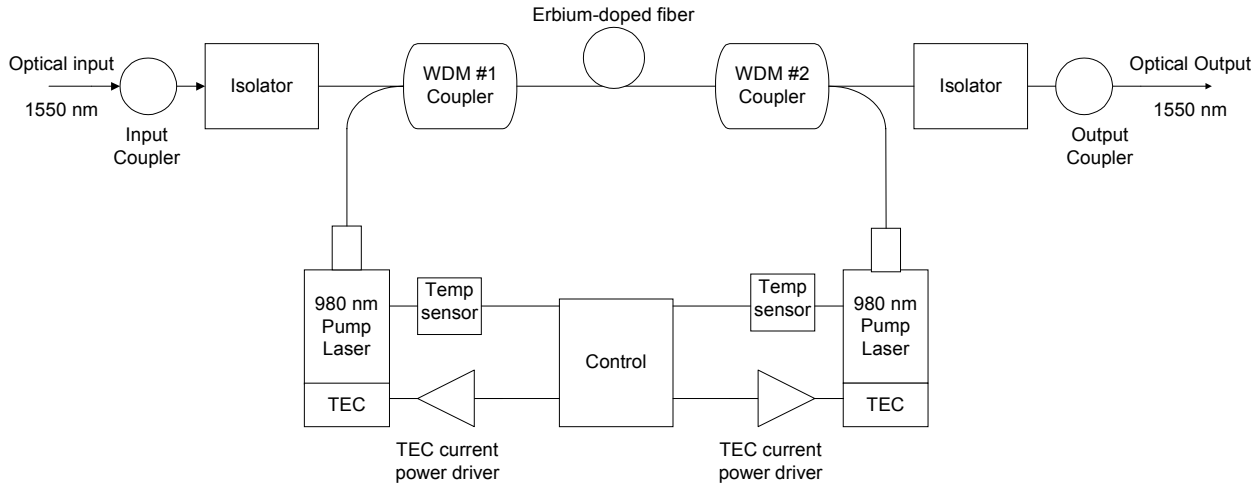

Figure 1: Dual-Pumped EDFA Basic Block Diagram

The energy for the amplification comes from the "pump" lasers. A typical system has two lasers, where the powers are optimized in the first stage for low noise and in the

second stage for high efficiency (high gain) [2]. The pump lasers excite the erbium to an energized (but slow-to-decay) state; when a weak 1550 nm signal enters the fiber at the optical input, the light stimulates the erbium atoms to release their stored energy as additional 1550 nm light. The amplification continues down the fiber, which is usually several meters long.

The optical input passes through the first isolator to the coupler, where 980-nm energy is coupled into the fiber. The 1550-nm signal is amplified and passes to the second coupler, which passes in energy from the second pump laser. The resultant optical signal passes through the second isolator and out the optical output port.

Requirement on Temperature Control of the Pump Laser

A typical pump laser module (Figure 2) includes a laser diode (LD), a photo diode (PD), a thermistor (R_{TH}), and a thermoelectric cooler (TEC).

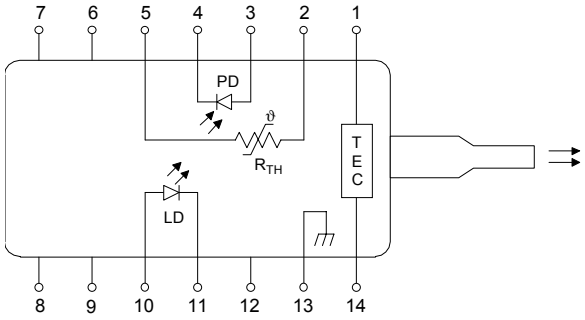

Figure 2: Pump Laser Module

The pump laser's output wavelength is required to be "close" to the 980-nm excitation frequency of the erbium atoms in order for the amplifier to work efficiently. Since the pump laser's output wavelength depends on its temperature, the pump laser needs to operate at a constant temperature to ensure pump conversion efficiency. The wavelength dependence on temperature varies between 0.02nm/°C and 1 nm/°C. For efficient operation of the EDFA system, a stability of ±4 ppm in laser wavelength is needed [3]. This translates into a requirement that the temperature of the pump laser be controlled as loosely as ±0.2°C or as strictly as ±0.004°C, depending on the wavelength dependence of the pump laser.

Temperature Measurement and Control

The temperature of the pump laser is measured with a thermistor. The thermistor has a negative temperature coefficient –its resistance decreases with increasing temperature. While the thermistor has a non-linear response over its operating range (see, for example, Figure 3), its response is linearized over the small operating temperature variation to which the laser is being controlled.

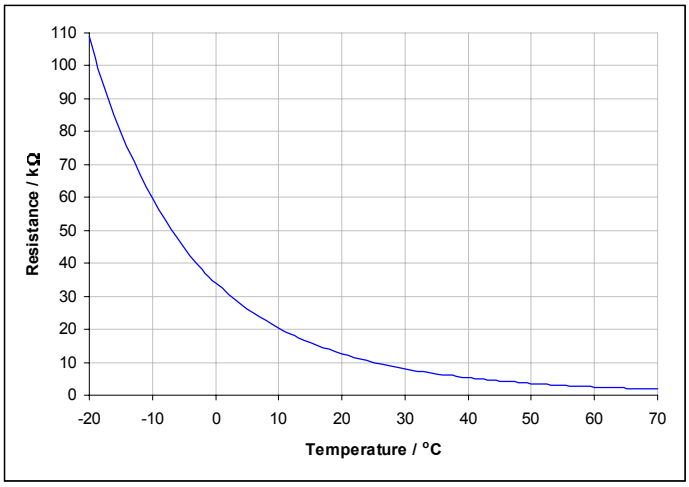

Figure 3: Example Thermistor Resistance as a Function of Temperature

The laser outputs the proper wavelength at a particular temperature that varies slightly from laser to laser. The laser unit's output wavelength is measured, and the thermistor resistance at which the wavelength is optimal is recorded. The job of the control loop is to maintain the thermistor, and hence the pump laser, at that particular temperature. The control loop, then, must maintain the stability of the temperature to the set-point.

A thermoelectric cooler (TEC) is used to maintain the pump laser at the proper temperature. The TEC is a Peltier element that is mounted near the laser diode. Current is driven through the element to either heat or cool the laser diode to maintain its temperature and, consequently, the laser's output wavelength.

A pulse-width modulation (PWM) scheme to generate the current driven through the TEC element was chosen because of its power efficiency. Instead of directly driving the desired current through the element with a linear driver, which would keep the driving transistors in their active region continuously, dissipating excessive wasted power, the TEC driver generates a rectangular waveform with a varying duty cycle that is filtered to produce the desired current through the element. Since the driving transistors are not continuously in the active region, the driving efficiency is greatly improved.

System Requirements

While the temperature control of the pump laser is important for proper EDFA operation, there are other functions the system must perform. For example, many pump lasers have a back facet diode that can be monitored to ensure that the laser is maintaining its output power. Many systems incorporate a control loop to monitor the diode and control the laser diode current. Power at the input and output of the amplifier can also be monitored. There are also additional functions such as dynamic gain-flattening filtering that require processing power in the system. These additional applications are explored later in this paper.

Because of the multitude of system functions, it may be advantageous to centralize the various control functions into a single processor as opposed to buying intelligent parts for each function as well as incorporating a processor. The platform described here shows how a single processor combined with targeted analog parts can produce a cost-effective, multifunction-capable design with a small footprint.

System Design Goals

The control system design goals are to tightly control the temperature of multiple pump lasers efficiently while minimizing any interactions between the pump lasers being controlled (e.g., through power supply coupling). Since dual-pump EDFA lasers use two lasers, controlling four pump lasers with a DSP seemed reasonable. To maximize the efficiency of driving current to the TEC, a PWM scheme is used. To prevent interaction between the PWM controls to each TEC, a method needed to be implemented to control the duty cycle and the edges of the PWM waveforms to prevent minimize simultaneous switching noise between the channels. It was also desirable to minimize the number of power supplies to the analog and control circuitry – all of the circuitry runs from 3.3V except for the core of the DSP that requires 1.8V. Finally, it was a goal to demonstrate a method to meet these goals using a processor that has plenty of spare MIPS available for other required monitoring/control functions of the EDFA system.

Summarizing, the system design goals were:

- <0.01°C temperature stability on each channel
- Control of four pump lasers' temperatures
- Efficient control of TEC (use PWM drivers)
- Phase control of PWM to minimize power supply noise
- 3.3V operation
- Minimize size by using a single DSP with spare MIPS for additional functions

Demonstration Board Design

Core Design Block Diagram

The block diagram of the core system designed to meet these goals is shown in Figure 4. This section of the paper describes the overall function of the core design and details the important features of the parts used in the design.

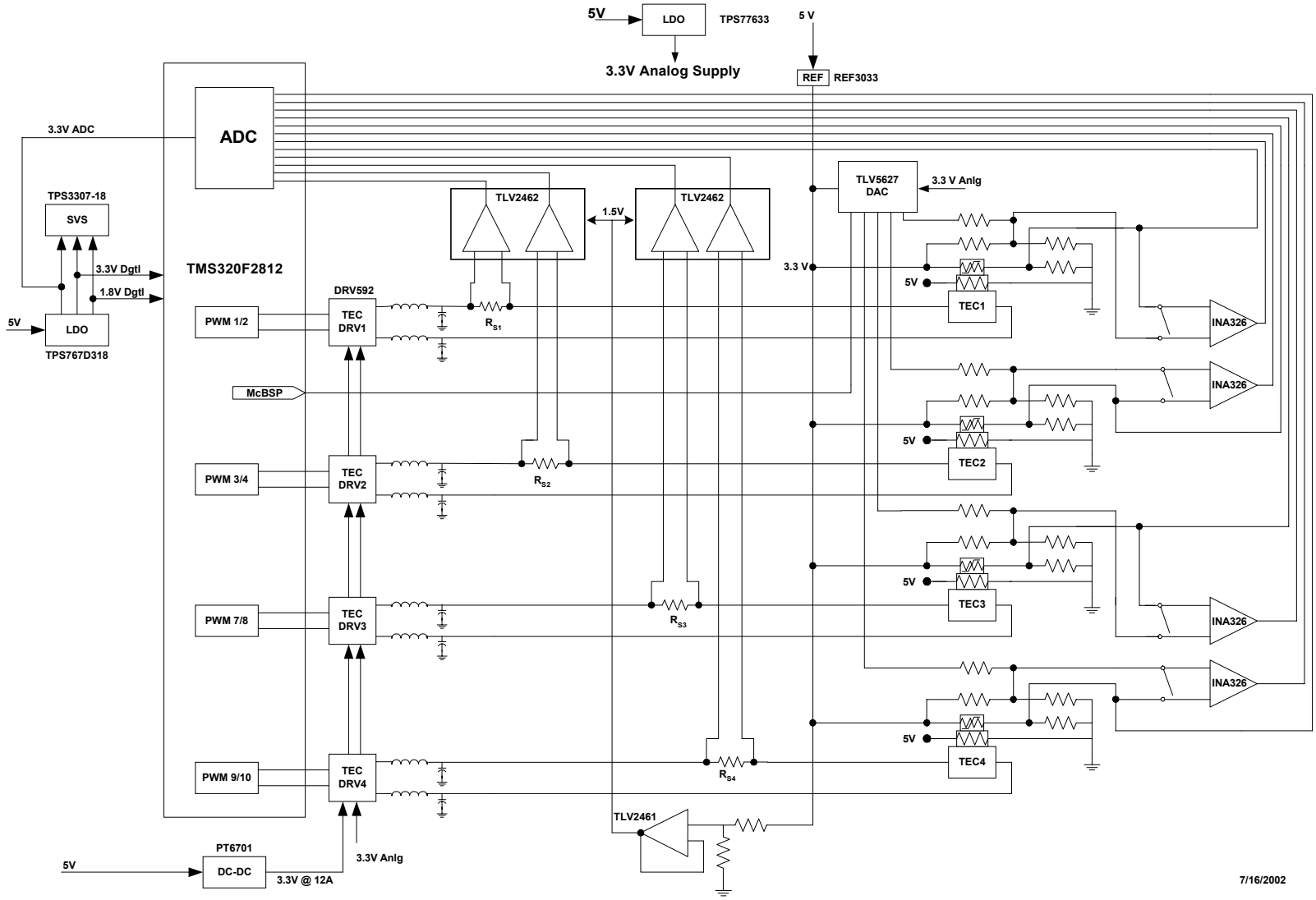

Figure 4: Demonstration Platform Block Diagram

The laser pumps are replaced on the board with units that emulate the thermal characteristics of the pump lasers. Each unit consists of a power resistor to generate heat as the laser would do in operation, a thermistor to measure the package temperature, and a TEC to control the package temperature, all contained within a butterfly package such as would house an actual pump laser. Measurements and modeling, described below, were made to ensure that the emulated pump laser's thermal characteristics would match that of an actual pump laser.

The thermistor is part of a bridge circuit that is used to accurately measure the temperature of each package. The bridge output is fed through INA326 buffer amplifiers to the F2812's internal 12-bit ADC. An analog switch is used to short out the bridge periodically to measure the reference voltage of the bridge to compensate for any component or reference drifts.

The servo control PID algorithm computes the appropriate control effort needed to maintain the desired set-point. The output of the control algorithm controls the duty cycle of the PWM drivers onboard the F2812 DSP. These PWM outputs drive the DRV592's. The outputs of the DRV592's are passed through lowpass filters to produce low-noise control voltages to the TECs.

Also required are safety circuits to prevent damage to the TEC element. For example, both the voltage across and the current through the TEC are monitored. If excessive voltage or current is detected, the processor takes the appropriate actions to prevent damage to the TEC. Sense resistors are placed inline with the currents to the TEC drivers to sense if the TEC units draw too much current. This can happen if a TEC unit is damaged or if the TEC cooling capability is exceeded. The voltage across each sense resistor is amplified with a TLV2462 and passed to an ADC channel of the F2812. The control software monitors the current to ensure that excessive current isn't being drawn across the TEC elements.

Since the controller software knows the voltage being applied to the TEC, sensing of over-voltage is performed within the control algorithm. Details are in the "Control Loop Design" section of this paper.

A more subtle failure condition is a short or open circuit in the thermistor. If allowed to operate unchecked, the control algorithm would force the TEC to one extreme or the other of its operating current, since no change in the temperature would be sensed. This could lead to the eventual destruction of the TEC. The processor is able to perform reality checks on the readings from the thermistor and act appropriately in the event of a thermistor open or short. Details of this software checking are in the "Sensor Error Detection" section, below.

The remainder of this section of the paper describes the reasoning behind the selection of the various parts used on the demonstration platform. More detailed hardware design information is included in the hardware description document supplied with the platform.

TMS320F2812 Processor

The F2812 DSP's design makes it ideal for a TEC temperature control application. It has multiple PWM channels that can be independently controlled, allowing TEC control while minimizing power-supply ripple. The PWM's high rate (292 kHz) improves the efficiency of the TEC control operation. Its onboard 12-bit ADC provides a compact method to measure the thermistors of the pump lasers. And the F2812 provides ample processing power to easily control four pump laser diodes' temperatures with spare power to handle other system requirements.

Since the external memory is not used in this application, it is possible to use the F2810 processor in place of the F2812 processor used on our demonstration platform. The F2810 is smaller (128 pins vs. 176 pins for the F2812's LQFP package).

DRV592 PWM Driver

The DRV592 is an ideal device to drive the TEC. Its low driver impedance maximizes the efficiency to the TEC. It is able to run at the low 3.3V supply voltage used by the DSP and other electronics in the system. It contains safety circuitry to protect itself from over-current and over-temperature conditions and to report those conditions to the processor.

The DRV592 accepts TTL-compatible PWM inputs from an external PWM driver, such as those contained on the F2812. These inputs allow the PWM signals to be controlled by the DSP to minimize simultaneous switch noise on the power supplies.

INA326

This instrumentation amplifier is used to measure the thermistor's resistance in the bridge circuits. The amplifier, designed for single power supply operation, features low offset (125 μV maximum) and offset drift with temperature (0.4 μV/°C), which is important to meet the tight accuracy temperature tracking specification for this design. It also features a rail-to-rail output swing and input range, which allows this device to stay within the design's 3.3V power supply voltage constraint. The high common-mode rejection ratio (>94 dB) makes it an ideal device for a bridge measurement circuit. Finally, the low 1/f noise allows for accurate measurement of the unknown thermistor value in the bridge.

TLV2462

These operational amplifiers are used to measure the TEC drive current across sense resistors (one per channel). The TLV2462 features rail-to-rail input/output dynamic range, high output drive capability, the ability to work from a low supply voltage, and low power supply current requirements. The rail-to-rail dynamic range is important since the voltages to the TECs can swing to the rails. The low supply voltage capability allowed the analog design to stay within its 3.3V constraint.

Features to Assist Demonstration and Evaluation

Not shown in the block diagram are some features that have been added to the demonstration platform to assist in the evaluation of the TEC function. These features are described here.

The F2812 contains an SCI interface that can be easily tied to a PC's UART through a level translator (e.g., the SN75LV4737A). A command interface has been developed that allows the control loop operation to be monitored and controlled from a program on the host PC. Using this program, temperature step responses and temperature statistics can be easily collected and displayed.

Several LED's have been placed on the board to indicate when the temperature is in control, when power is good on the unit, or when error conditions (e.g., thermistor shorted out) have been detected.

Control Loop Design

This section of the paper describes the measured thermal response of a typical pump laser and how these measurements were used to both architect the control loop and guide the design of a mockup unit that emulated the thermal performance of an actual pump laser.

Thermal Characterization of a Pump Laser

A pump laser (Corning 980nm Optilock™) was mounted to an AMC7820 evaluation board [4] and its thermal behavior characterized. This pump laser has a maximum output power of 250- to 300-mW.

It was posited that the temperature would change exponentially in response to a change in TEC current, and this was confirmed experimentally. In the testing, the laser was first allowed to achieve a steady-state temperature while operating at full power. Then the TEC either heated or cooled the laser. Data was taken for about 50 seconds each trial. The temperature was only moved by a small amount since the time constants needed are for the steady-state control of the TEC. The measured data was fit to an exponential, and the time constants are shown in Table 1 and Table 2.

Table 1: Pump Laser Heating Time Constants

Temperature change (°C)	**20 to 25**	**25 to 30**	**30 to 35**	**35 to 40**	**20 to 30**	**30 to 40**	**25 to 35**
Time constant (sec)	4.240	4.258	4.398	4.362	4.430	4.228	4.288

Table 2: Pump Laser Cooling Time Constants

Temperature change (°C)	**40 to 35**	**35 to 30**	**30 to 25**	**25 to 20**	**40 to 30**	**30 to 20**	**35 to 25**
Time constant (sec)	4.572	4.483	4.315	4.086	4.313	4.232	4.381

The average time constant is about 4.3 seconds for small temperature changes.

The laser mock-up units used on the platform were built in butterfly packages and were tuned to have approximately the same time constants as the real laser units. This allows demonstration of the temperature control capabilities of the platform without the need to have an actual laser in operation.

Servo Sampling Rate

Because the system to be controlled exhibited a first-order response with a relatively long time constant, a straightforward PID controller with moderate sampling speed is sufficient to control the temperature of the laser.

Servo sample rates that are near multiples of the AC power-line frequency, but not exactly synchronized with the power-line, could result in power-line frequencies and their harmonics aliasing into near-DC temperature sensor inaccuracies. To prevent this, the sample rate should be chosen to avoid line-frequency harmonics. Sample rates at half-multiples of the line frequency will work well.

$$f_{servo} = (n + 0.5) * f_{line}.$$

For operation on both 50- and 60-Hz line frequencies, the sample rate should be chosen as a half-multiple of 150 Hz.

$$f_{servo} = (n + 0.5) * 150\ Hz$$

A servo sampling rate of 825 Hz was chosen for the demonstration platform. An 825 Hz sampling rate will repeat every four cycles of 60 Hz and every two cycles of 50 Hz.

At 825 Hz, the DSP is still only about 20% utilized, so the DSP could easily support faster sample rates. The limiting factor is the time constant of the filter on the INA326 error amplifier.

Control Loop Operation

This section describes the operation of the servo control loop for the TEC controller.

Each servo control period is started by a periodic interrupt from a timer in the DSP. During each sample, these operations take place:

1. The temperature is measured and controlled for each TEC channel, described in detail later.
2. The DSP processes any pending commands from the host.
3. The status display is updated and any needed fault protection is engaged.
4. Diagnostic information is sent to a diagnostic buffer for retrieval by the host.
5. Periodically (once every 128 samples), the drift cancellation circuit is activated to measure and cancel drift in the temperature sensor subsystem.
6. With most of the remaining time, the DSP polls for activity on the UART serial port.
7. The DSP returns to its idle state and waits for the next timer interrupt.

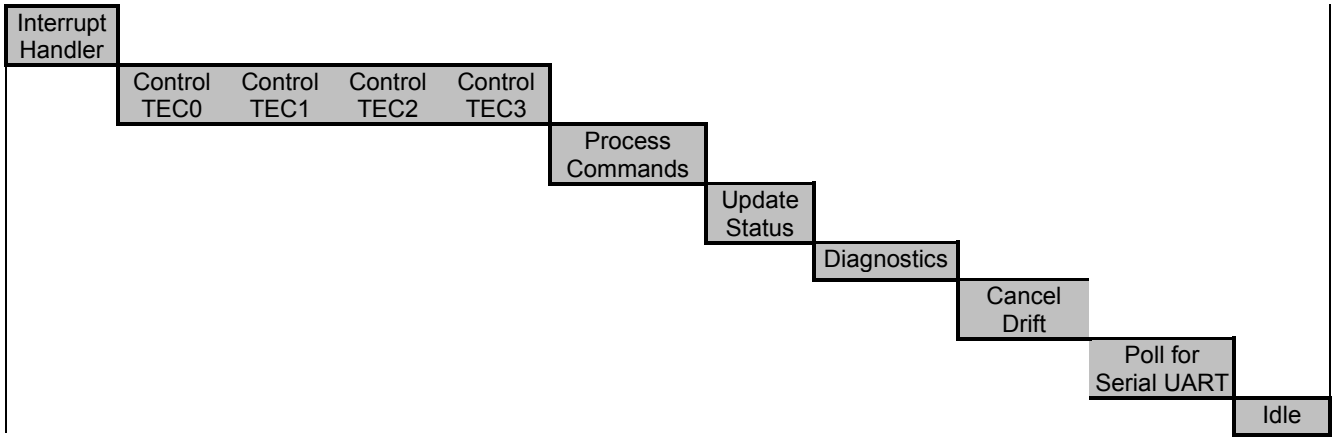

Figure 5: Task Flow Diagram

During each period, the DSP reads the temperature sensors using the A/D converters, calculates a control voltage, and sends the control voltage to the TECs via the D/A converters.

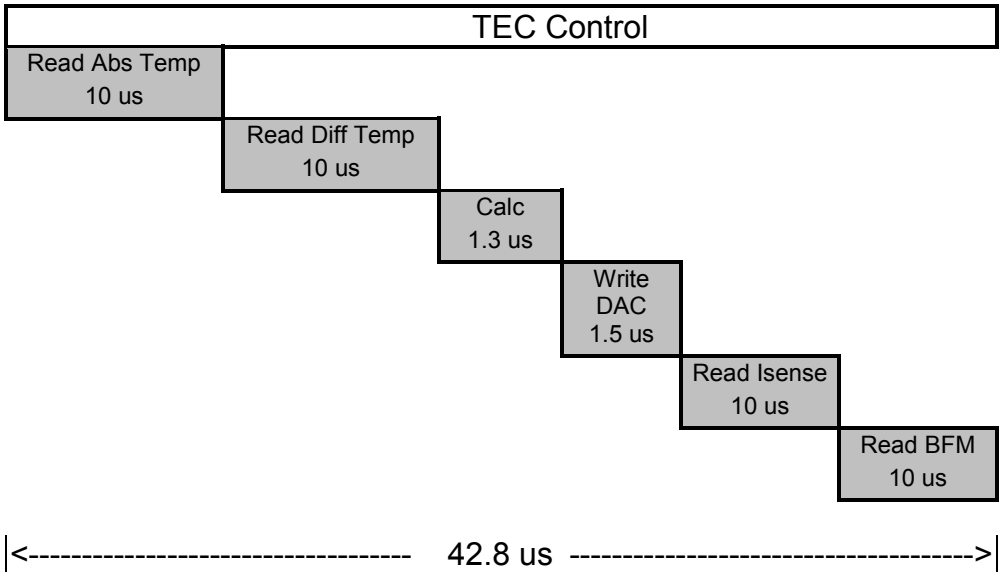

Figure 6: Detailed TEC Control Timing

Temperature Sensor Reading and Signal Processing

Reading the Sensor

The C2812 DSP contains 12-bit A/D converters and an A/D hardware sequencer that allows rapid collection of up to 16 samples. In the TEC control application, the sequencer is configured to read the same input channel ten times in rapid succession.

Processing the Sensor Signal

The ten raw values are then combined into a single value with more resolution and less noise. First, the highest and lowest values of the ten samples are discarded to help filter out transients. Next, the remaining eight values are averaged. The raw readings have 12 bits of resolution, and the smoothed value has 15 bits of resolution. Finally, a simple first-order equation converts the smoothed value into degrees C.

Calculating the Temperature Error

The control voltage calculation uses a "temperature error" as its input. The temperature error is the difference between the temperature measured by the sensors and the desired temperature setpoint. The method of calculating the temperature error depends on the control mode chosen:

1) In Absolute Mode, the A/D converter reads the absolute temperature of the sensor. The temperature error is calculated in the DSP by digitally subtracting the setpoint temperature from the measured temperature.

2) In Difference Mode (the default), the voltage from the temperature sensor is subtracted from a reference voltage by an analog difference amplifier before being read by the A/D converter. The result is a cleaner signal that uses much more of the input range of the A/D converter, but corresponds to a smaller range of sensor temperatures. The temperature error in Difference Mode can be calculated two ways:
   a) Digital: A setpoint offset value can be digitally subtracted from the analog difference signal to create the temperature error.
   b) Analog (default): An external setpoint DAC can be controlled to adjust the setpoint voltage into the analog difference amplifier.

Sensor Error Detection

The absolute temperature is always read during each control period, even when the controller algorithm is not operating in Absolute Mode, as a means for detecting thermistor failure. When the thermistor voltage is less than $1/16^{th}$ of full-scale, this is interpreted by the DSP as an open-circuit. Thermistor voltages greater than $15/16^{th}$ of full-scale are interpreted as short-circuits. In either case, the DSP reports a failure, disables the mock laser drive, and gradually ramps the TEC current down to zero to protect the device.

Control Voltage Calculation

The control voltage is calculated using a simple Proportional+Integral (PI) controller. The integrator term gradually pulls the steady-state temperature error to zero, while the proportional term quickly move the temperature toward the setpoint.

In general, increasing the current through a TEC device increases its cooling. However, because of ohmic heating within the TEC, increasing the TEC current beyond a certain value, called Imax, actually decreases the amount of cooling. The output value of the control voltage calculation is limited to 2.7 volts to ensure that Imax is not exceeded.

To limit integrator windup during startup and after large setpoint changes, the integrator term is limited to 95% of Vmax.

The software is written to support a derivative term for PID control. However, since the derivative term is used mostly to cancel rapid disturbances (which don't occur much in this application), and tends to amplify sensor noise, the derivative gain is presently set to zero.

Control Voltage Output

PWM DAC Architecture

The C2812 DSP contains two event managers (EVA and EVB) that each includes two GP timers and three full-compare units (see Figure 7). Up to eight PWM waveforms (outputs) can be generated simultaneously by each event manager: three independent pairs (six outputs) from the three full-compare units, and two independent PWMs from the GP-timer compares.

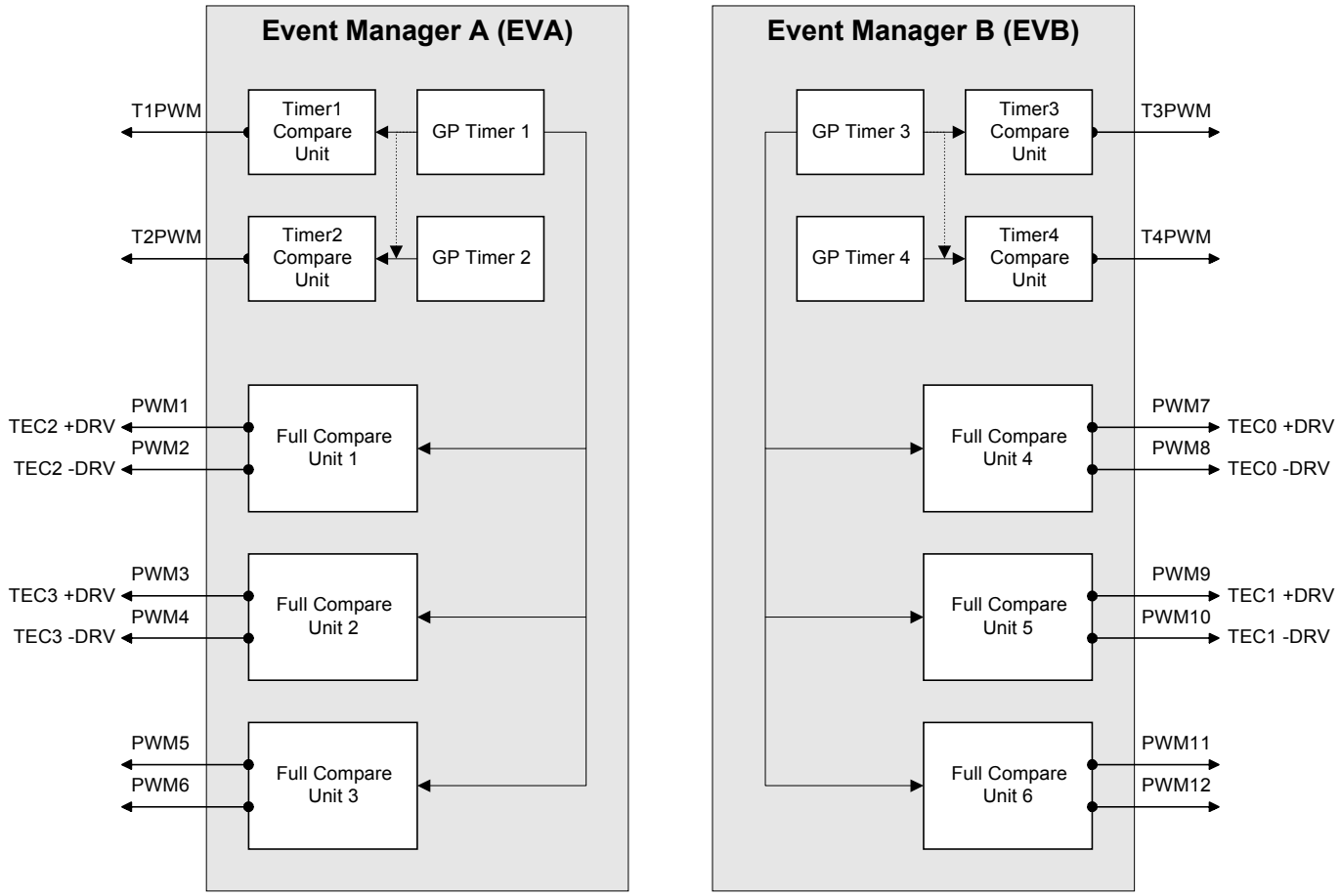

Figure 7: Event Managers

PWM Waveform Generation

The differential PWM inputs to the drivers are driven in a sign-magnitude manner. At any given voltage level, only one of the two input lines will be modulated, while the other line will be held at zero. To achieve positive output currents, the PWM+ line will be modulated and the PWM- line will be held low. For negative output currents, the PWM- line is modulated and the PWM+ line is low. This modulation scheme give a smooth transition between positive and negative

currents and yields lower switching noise than some schemes that modulate both lines simultaneously.

PWM Phase Alignment

The DSP's main clock runs at 150 MHz. The GP Timer1 period register is set to roll over every 512 samples, yielding a period of 150MHz / 512 = 292.96875 kHz. The GP Timer1 clock drives the Timer1 Compare Unit and the Full Compare Units 1, 2, and 3, so all PWM outputs derived from them are guaranteed to be phase-aligned to each other. GP Timer 3 serves a similar function in EVB, so the PWM outputs from EVB are also guaranteed to be phase-aligned to each other.

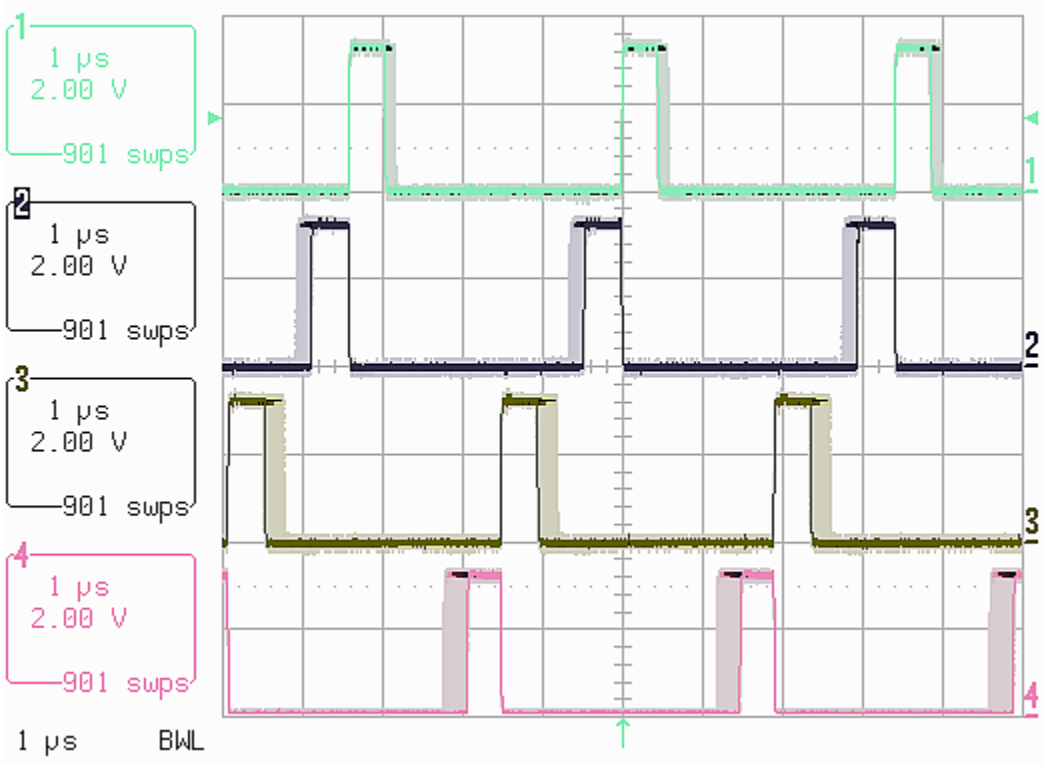

Figure 8: PWM Phase Alignment

Figure 8 shows the PWM outputs for all four TEC control channels. Note that the rising edge of channel 1 is always aligned with the falling edge of channel 2, regardless of the duty cycle. Likewise, channel 3 always rises when channel 4 falls. The phase of channels 3 and 4 is about 90° from channels 1 and 2.

DAC Resolution Extension

The PWM DACs have 10 bits of resolution (nine magnitude bits plus one sign bit). During testing in a slowly changing ambient condition, glitches of up to 10 milli-Kelvins were seen when the LSB of the DAC changed.

Increasing the PWM period from 512 to 1024 or 2048 would have increased the DAC resolution by one or two bits respectively, but it also would have slowed down the PWM frequency by 2x or 4x, rendering the driver output filters ineffective.

Rather than changing the PWM period, a software-only technique was used to modulate the LSB of the PWM DAC setting. For each servo control period the DAC only has one of 1024 possible settings. However, the average output over a longer time period (still shorter than the thermal time constant of the TEC device), can be one of 32768 possible values, giving 15 effective bits of resolution.

Performance Measurements

This section provides a summary of the performance evaluation of the Quad-Channel TEC Controller platform.

The four metrics used to evaluate the system are:

1. Step response
2. Temperature drift
3. Tracking temp changes due to "laser" intensity changes (resistor current changes)
4. Tracking temp changes due to ambient changes.

Step Response to Commanded Setpoint Temperature

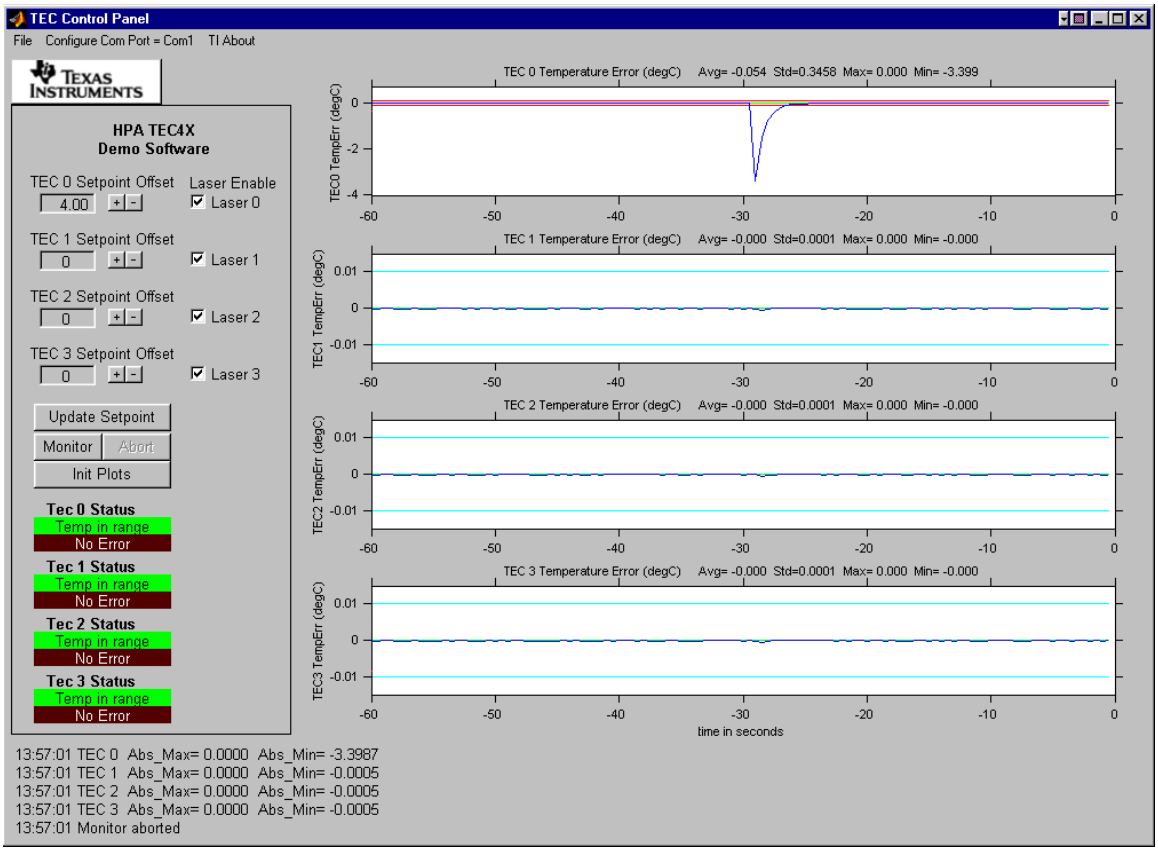

Figure 9: Response to 4°C Setpoint Temperature Step

A command was issued to move the TEC0 setpoint temperature by 4 C. As seen in the zoomed-in plot below, the controller pulled the temperature error within 0.100 C in 3 seconds, and to within 0.010C in 5.5 seconds. Note that no overshoot appears. Also note that the other three channels do not see any cross-coupling from TEC0.

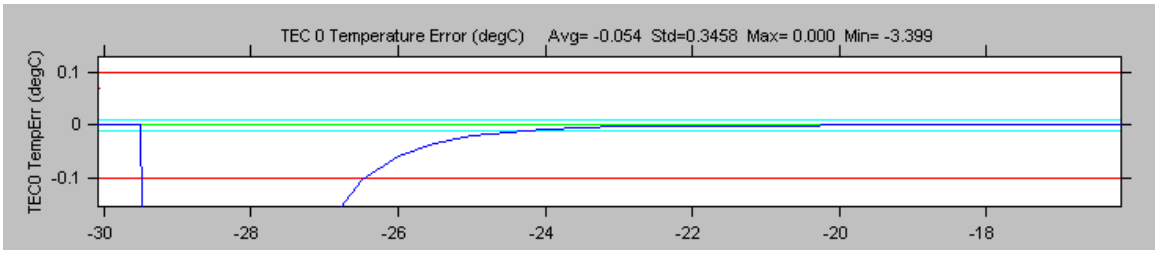

Figure 10: Detailed Response to 4°C Setpoint Temperature Step

In this next figure, the setpoint temperature was switched from +4.0 to –4.0C. The controller pulled the temperature error under 0.100C in 5 seconds. A cross-coupling error of about 1 mK is barely visible on the other three channels.

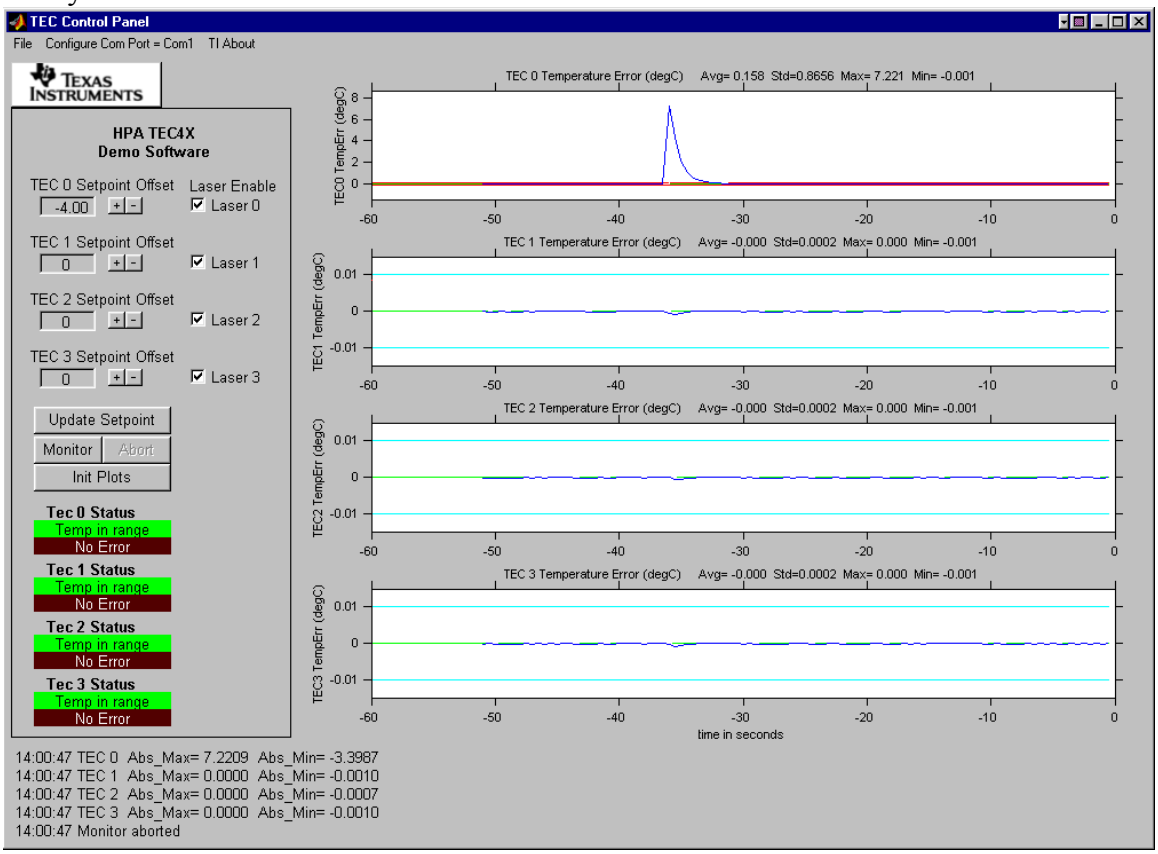

Figure 11: Response to -8°C Setpoint Temperature Step

Step Response to Laser Heat Load Change

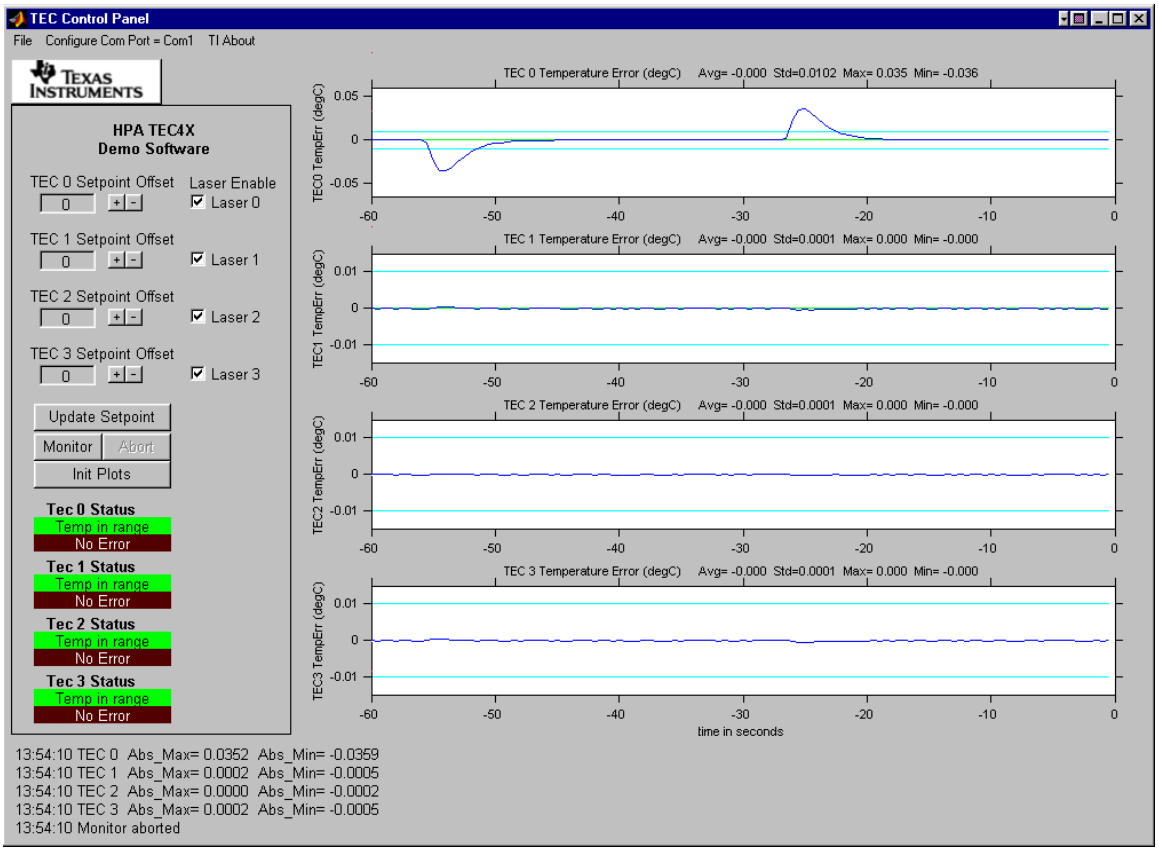

Figure 12: Response to Changing Heat Load

The 430 mW laser heat source for TEC0 was turned off, and then turned back on 30 seconds later. The controller held the temperature excursion to 0.035C, and was back within 0.010C in 5 seconds. Note that no cross-coupling is seen with the other channels.
Turning the laser on or off does not instantly show up as temperature error since it takes a few seconds for the heat to flow from the laser to the thermistor. Contrast this with the instantaneous response to a change in setpoint temperature.

Tracking Ambient Temperature Changes

In this TEC controller system, the heat from the laser and the TEC must be dumped into the heat sinks. Without a control loop operating, a change in heat sink temperature would translate directly into a change in laser temperature. The purpose of the control loop is to attenuate those deviations.

Changes in ambient temperature cause the heat sink temperature to change with a first-order response with a time constant of several minutes. P+I controllers respond to step changes with zero steady-state error, and to ramp inputs with a constant error that is proportional to the slope of the ramp input. Compared to the short time scale of the laser/TEC assembly, the first-order response of the heat sink temperature looks like a ramp input to the laser. As the heat sink approaches the ambient temperature, the rate of change decreases and the laser temperature error approaches zero.

In Figure 13, a board configured to hold the TEC temperature at 35C was moved from room temperature (74F, 23C) into a heated chamber (150F, 65C). In the 9-minute period that followed, the TEC temperature never deviated more than 0.002C from the setpoint. As the heat sinks approached the chamber temperature, the TEC temperature deviation gradually shrunk toward zero.

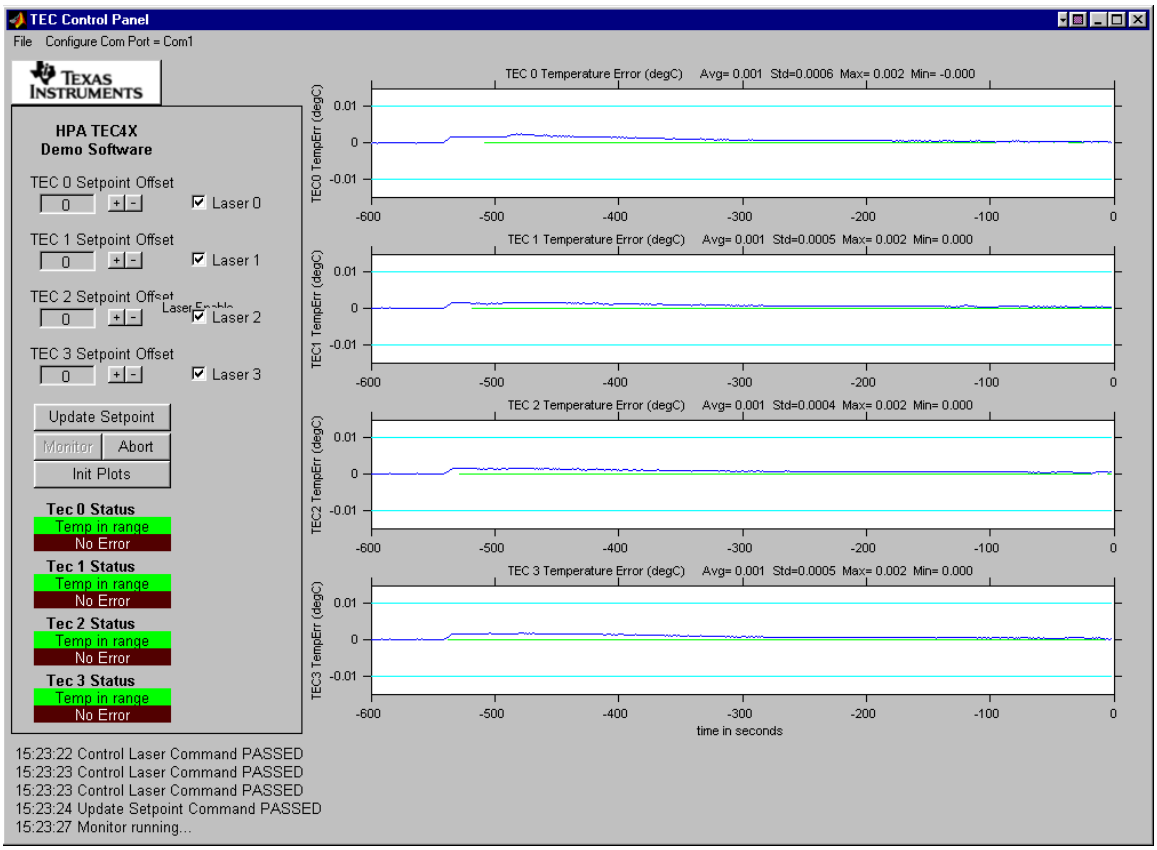

Figure 13: Response to Changing Ambient Temperature from Cold to Hot

After the board temperature had acclimated in the hot chamber, the board was removed and placed next a high-volume fan. This airflow cooled the heat-sink temperature much more quickly than they had heated up. This rapid temperature swing caused a larger but faster TEC temperature deviation of 0.015 to 0.017C.

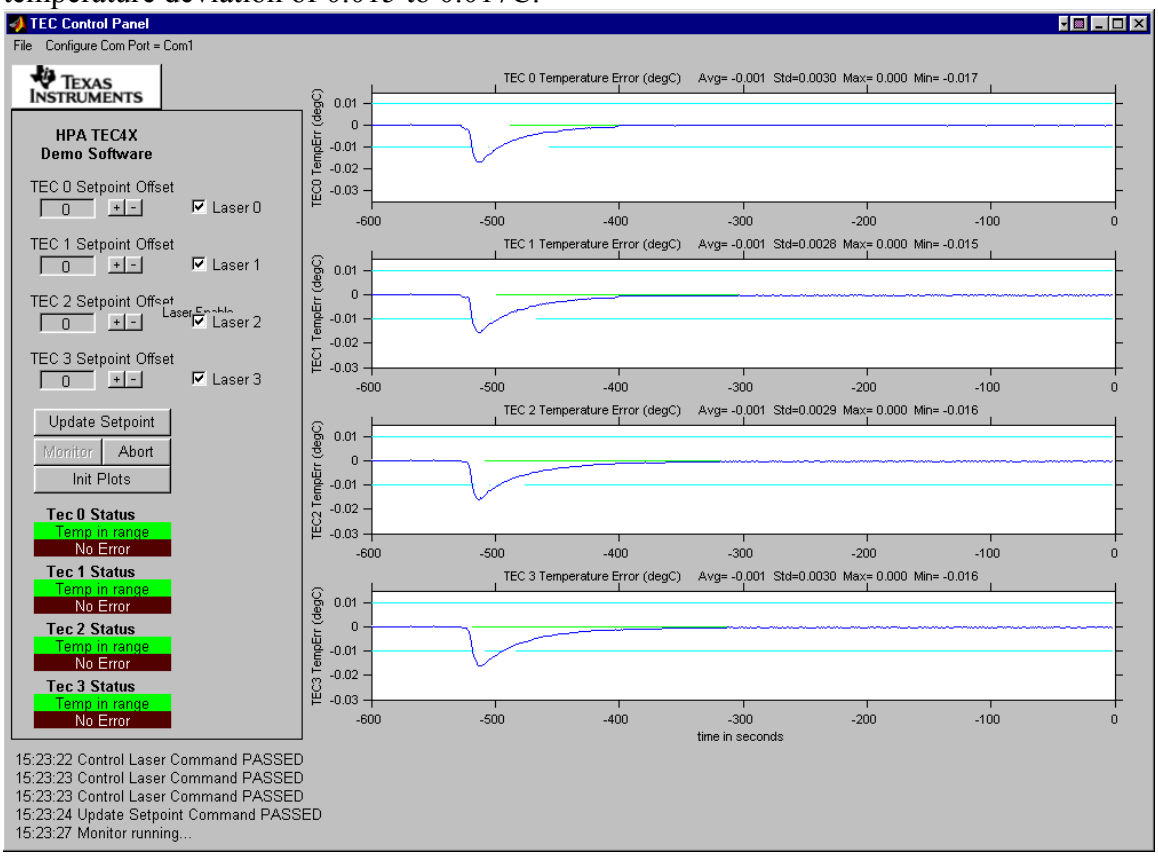

Figure 14: Response to Changing Ambient Temperature from Hot to Cold

Drift Due to Electronics Temperature Changes

As the board temperature changes, the temperature measured by the sensor will also change. Sources for this drift include

- Sensor bridge reference voltage
- ADC reference voltage
- Sense amplifier offset
- Sensor bridge resistor changes

The TEC controller attempts to cancel out drift from the first three sources by periodically (every 155 ms) shorting the inputs of the sense amplifier and measuring the change in offset voltage since startup.

To demonstrate the effectiveness of this circuit, the thermistor was unplugged and replaced with a single 10k resistor of the same type used in the sensor bridge. The board was then moved between a cold chamber, room temperature, and a hot chamber while measuring the drift. Each data point is the average of 120 reading taken 0.5 seconds apart.

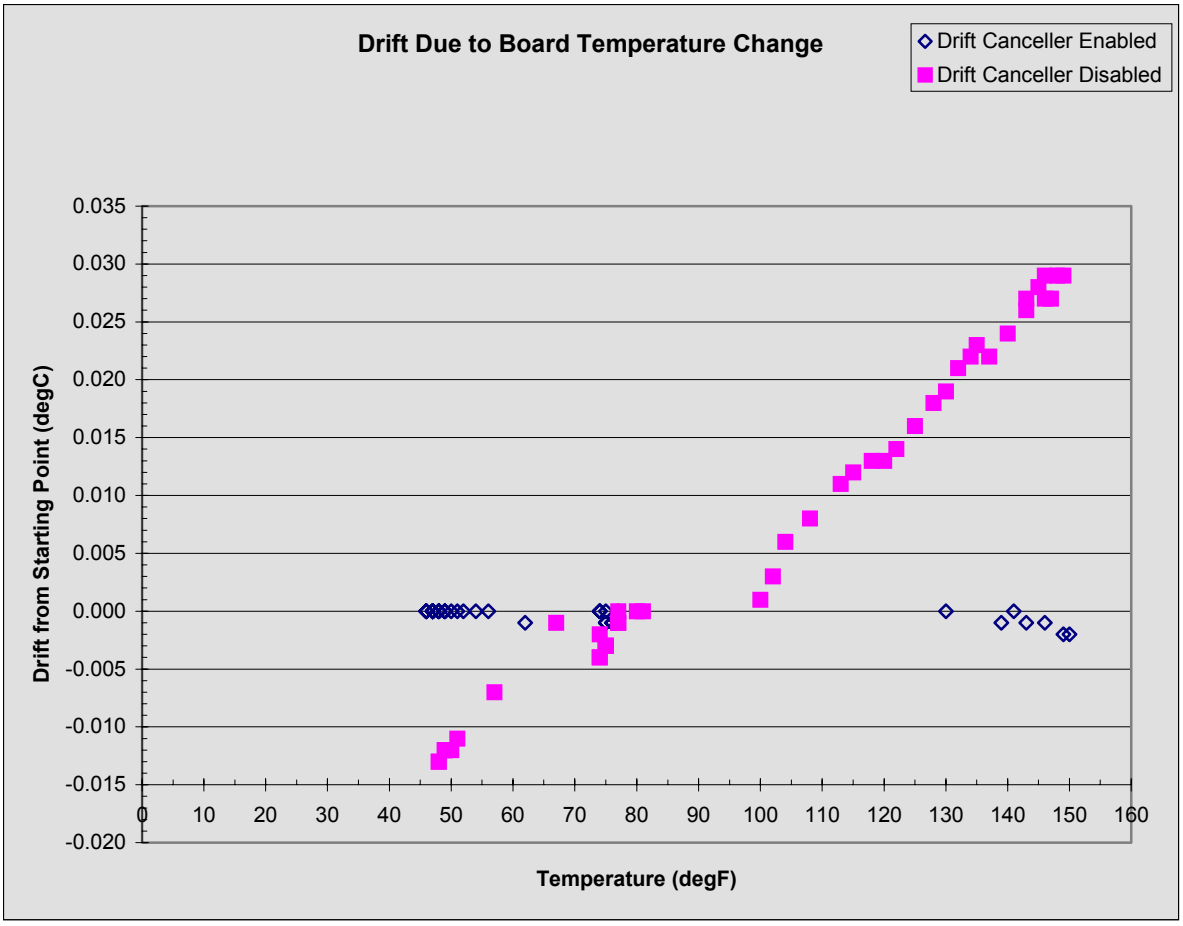

Figure 15: Drift Due to Board Temperature Change

Without the drift canceller, the indicated temperature varied from –13 mK at 48F to +29 mK at 150F. This corresponds to 52 mK drift over a 70C range.

With the drift canceller turned on, the drift is a little over 1 mK. From this, it is clear that the drift canceller is a useful feature for high-precision applications.

Processor Utilization

The control of the EDFA laser's temperature is a straightforward control problem, and the loading on the F2812 DSP is low. As seen in Figure 16, over 80% of the processing time is spent waiting for character transfers in the serial UART. Even at maximum communication speeds, most of the time the processor is idle. This leaves plenty of spare processing power to attend to other tasks required by the system.

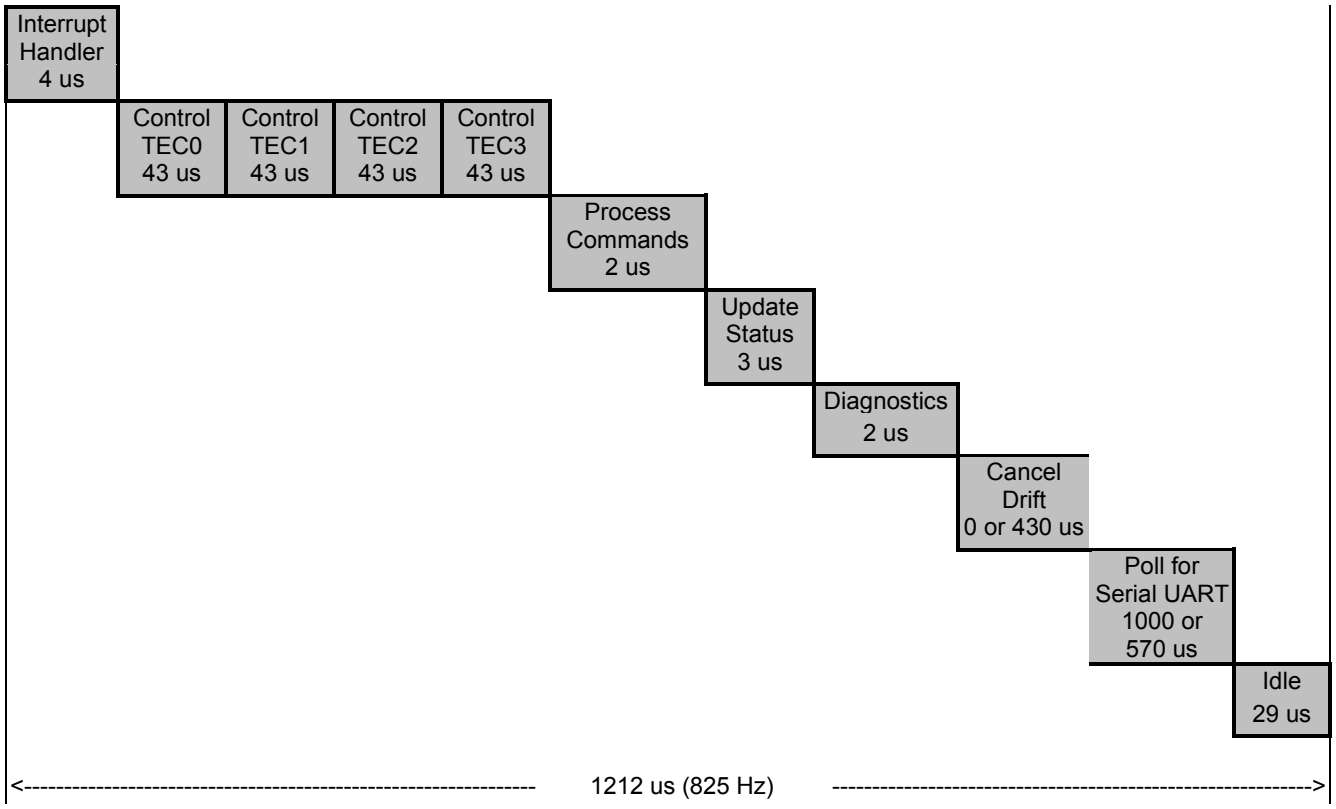

Figure 16: Overall Timing Diagram

Extending the Design

The basic design shown with this engineering platform can be extended in many ways. This section describes modifications and extensions that are possible.

Optimizing the Design for Area

The demonstration platform was designed to show the implementation of a four-channel TEC controller in a way that would allow the user to probe the operation of the design easily. Additional circuits were also added to allow the user visibility to the controller operation. Finally, the board was designed to place all components only on the top side of the board. Because of this, the design is not optimal for board space usage. This section of the paper describes techniques that can be used to reduce the board space usage of the design.

One option to reduce the board space around the DSP is to use the BGA package for the DSP. Not only will the DSP use slightly less board area, but the decoupling capacitors can be moved to the back of the board. An alternative is to use the F2810 if external memory isn't required (it's not on this platform, for example), which has a smaller package than the F2812's LQFP package.

Many of the discrete components can be placed on the back of the board to reduce board space.

The inductors used for the DRV592 output filters were sized to handle a 3A drive into the TECs. Some TECs require less current (1A-2A), and the inductors can be reduced in size for these less stringent requirements.

A method to remove half of the TEC filter network components, saving a significant amount of area, is described in the "Quad-Channel TEC Controller Hardware Description."

The power circuitry on the board was designed to allow an external power "brick" to be connected to the board and for design convenience. The circuitry is not representative of what would be required inside an actual EDFA amplifier. Optimization of the circuit for the actual system requirements would probably result in a reduction of the power supply circuitry area.

Much of the circuitry on the board was added as diagnostic or feature selection circuitry to demonstrate the control loop operation and to assist in the debug of the DSP. In an actual system, the JTAG header, the RS232 connector, the jumpers, and many of the LED's and their associated drivers could be removed.

Because both the current and voltage being driven to the TEC are being monitored, it is possible to remove the current monitoring circuitry on the platform with minimal reduction in functionality. The software controls the voltage being sent to the TEC, and prevents this voltage from exceeding a certain value. In addition, the DRV592 driver devices have circuitry that shut off the current being driven to the TEC when it exceeds 4 amperes, as it might in a fault condition where the TEC is shorted. In this case, an error signal is sent to the DSP to indicate

that an error has occurred. Because of these other checks for excessive current being driven into the TEC device, the current monitoring circuitry is a good candidate to remove to reduce the total circuit size.

TMS320F2810

The engineering platform was designed with an F2812 DSP because of silicon availability early in the DSP's development. Since the external data bus of the DSP is not used in this design, it is possible to substitute the smaller F2810 DSP into the design with no loss in performance or function.

It is also possible to use the MicroStar BGA package for the processor instead of the PGF package used. This would reduce the size of the design, as described above.

Back Facet Diode Monitoring

Because of the light load on the DSP, it can easily accommodate additional functions. Common functions that can be added include back facet diode power monitoring, output power monitoring, and dynamic gain flattening filtering.

The circuit for either the back-facet diode power monitoring or the output power monitoring is basically the same: a trans-impedance amplifier converts the current through a photo-diode detector into a voltage measured by an ADC [5].

Dynamic gain flattening equalization is necessary in wavelength division multiplexing (WDM) systems where power- and wavelength-dependent gain characteristics of EDFA's can lead to SNR degradation in the system. The basic idea is to measure the frequency response of the system using an optical spectrum analyzer, and then adjust the gains across the transmission wavelengths to provide an optimal and uniform signal strength at these wavelengths. The problem is complicated in a dynamically re-configurable WDM network since lasers and connections are added or dropped as required by the system. One solution is to use a DSP to continually measure and compensate for the frequency response variations of the network. The equalization algorithm requires Fourier transform operations and is therefore ideally suited for a DSP implementation. [6,7]

Extension to Additional Channels

The demonstration platform showed how four TECs could be controlled with a single F2812 DSP. Because of the processing power left in the DSP, it is possible to consider extending the design to more TEC channels being controlled. This section of the paper describes how the design could be extended to control eight TECs simultaneously.

Figure 17 shows the architecture of the F28x event managers that are used to control the PWM signals to the TEC units. In the present design, the TECs numbered zero through three are used.

TECs numbered four through seven are those that could be added to extend the capability of the platform to eight TECs being controlled by a single DSP.

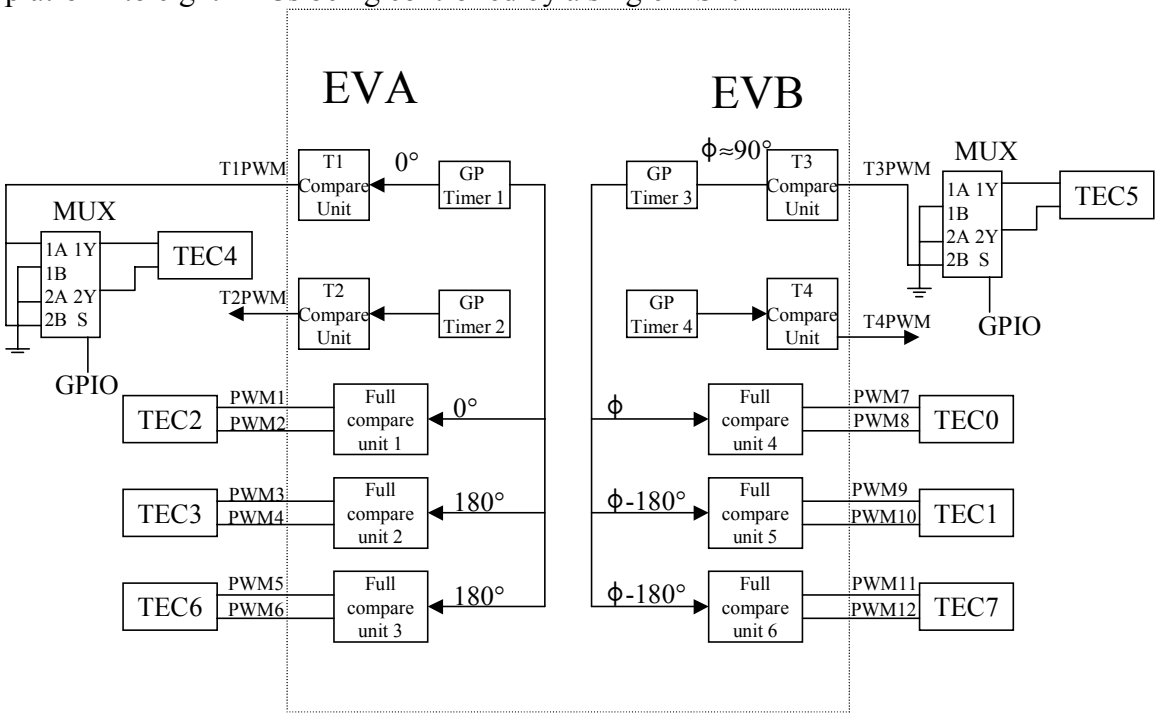

Figure 17: PWM DAC Configuration for Eight TEC Channels

The F2812 DSP contains two event managers (EVA and EVB) that each includes two GP timers and three full-compare units. Up to eight PWM waveforms (outputs) can be generated simultaneously by each event manager: three independent pairs (six outputs) from the three full-compare units, and two independent PWMs from the GP-timer compares. Two timers are used (GP Timer 1 and GP Time 3), configured to produce timing signals approximately 90-degrees apart from each other. When four TEC channels are used, as on the demonstration platform, the four quadrature-encoder pulse drivers then generate signals that are at 0-, 90-, 180-, and 270 degrees. This spreads out the PWM edge transitions and minimizes noise on the power supply rails.

The additional four channels are added in the following fashion. First, two TEC channels ("TEC4" and "TEC5") are attached to the timer-1 and timer-3 outputs. These signals are set to operate at 0- and 90-degrees. These signals control the PWM duty cycle to these two added TECs. The sign of the corrections are controlled by two GPIO pins, one per TEC channel. The other two added TEC channels ("TEC6" and "TEC7") are added to the two remaining quadrature-encoder pulse drivers ("Full compare unit 3" and "Full compare unit 6"). These two channels operate at 180- and 270-degrees. The end result is four added channels operating 90-degrees apart from each, spreading their PWM edge transitions apart to minimize power supply noise.

It is also necessary to use eight additional ADC channels to measure the temperature and temperature error of the four additional TEC channels. In the demonstration platform design , four ADC channels are available for reading the back-facet monitor voltage and four ADC channels are used for over-current detection. As described above, the over-current measurement using the sense resistor through the ADC channels can be accomplished with the over-current detection feature of the DRV592 driver. By dropping the current sense and BFM control functions from the DSP, eight ADC channels could then be used to read the temperature sensors in the four added TEC channels.

As Figure 18 shows, controlling eight TECs does not burden the DSP much more than four. Most of the time spent controlling each TEC is used to read and process the sensor signals. Without the current sense and back-facet monitor, the control time for each TEC channel drops from 43 us to 23 us, thus providing most of the processing time needed to control the four additional TECs.

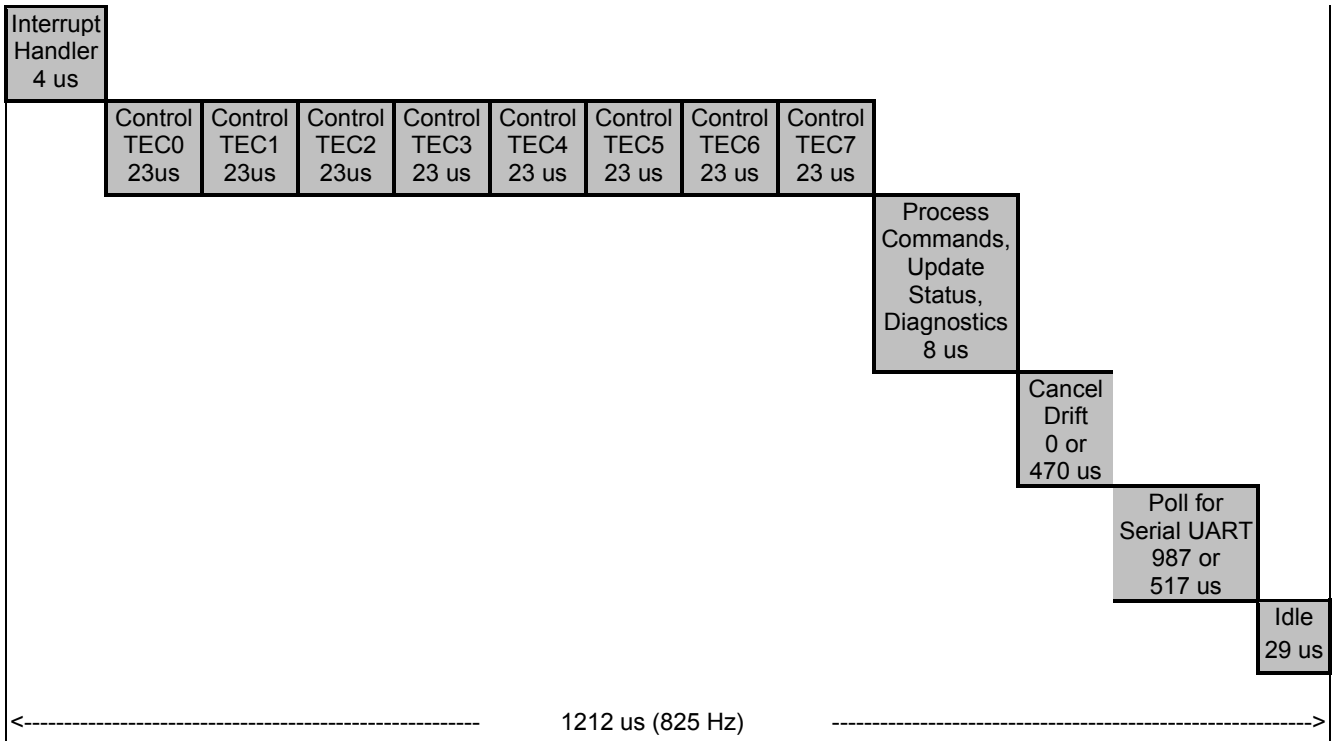

Figure 18: Timing Diagram When Controlling Eight TEC Channels

Conclusions

An engineering platform that demonstrates a single TMS320F2812 DSP controlling four TEC control loops was shown. The analog portions of the design were chosen to minimize the temperature measurement error and maximize the efficiency of the drive to the thermoelectric cooler. The advantages of using a single DSP over discrete TEC controller modules are the ability to control the edges of the PWM signals to the TEC drivers, minimizing noise, the ability to use the programmability of the DSP to easily handle exception processing, the extendibility of the design to additional TEC channels, and the ability to add function easily to the DSP to control other aspects of the design, such as back facet diode monitoring and dynamic gain flattening filtering. Finally, methods to add additional channels and reduce the footprint of the base design were shown.

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