XIO1100 NAND-Tree Test

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ABSTRACT

Checking the interconnections between integrated circuits (IC) once they have been assembled on a PCB is important in some applications. The normal method for performing this check is through using boundary scan as defined by the IEEE Std 1149.1a specification (also known as JTAG). Since boundary scan is not implemented in the XIO1100 PHY, an alternative method must be employed. The XIO1100 PHY has a NAND-tree test feature that can be used. This document discusses the NAND-tree test feature, explains what it does, and describes how to use it.

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1 Introduction

The common method for checking the interconnections between the ICs is to use JTAG boundary scan. Since the XIO1100 PHY does not support JTAG boundary scan, a NAND-tree feature has to be employed.

A NAND tree is exactly how it sounds: A number of nested NAND gates in which each I/O pin is an input to one NAND gate. Figure 1 illustrates a NAND tree. The output of the nested NAND gates is provided on the JTAG_TDO pin. A NAND-tree feature does not provide 100% coverage but does allow for checking the connectivity of most I/Os on the XIO1100 PHY.

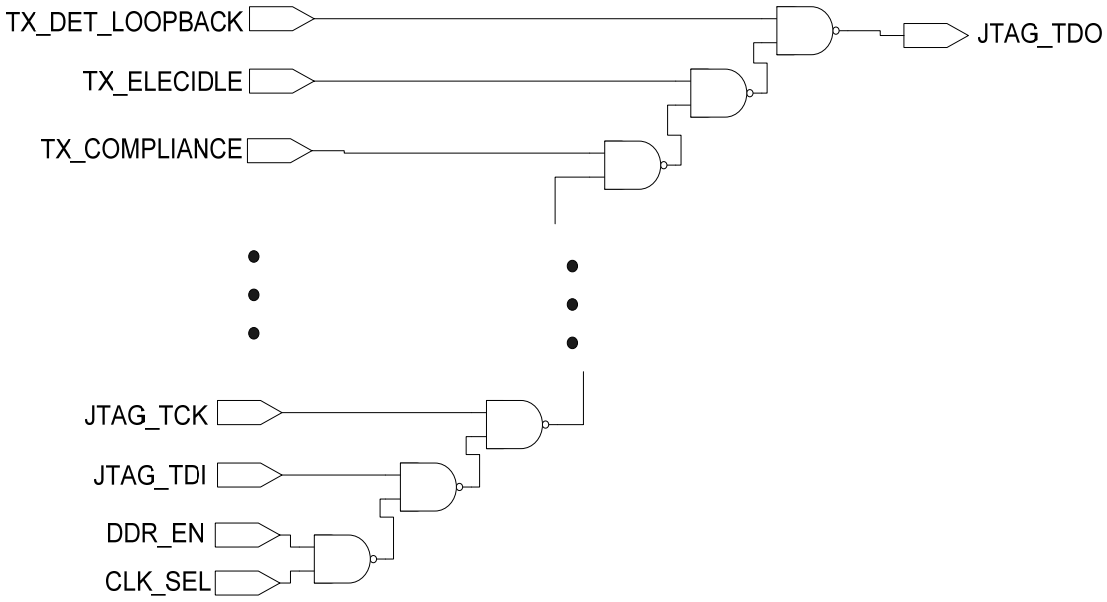

Figure 1. XIO1100 NAND Tree

2 JTAG Pins

In the XIO1100 datasheet, the five reserved pins are B9, A10, B10, A9, and C9. These pins should be left unconnected during normal operations except for C9 which should be tied to GND.

To use the NAND-tree mode in the XIO1100 PHY, these pins need to be connected to a JTAG controller. The function of each reserved pin is described in Table 1. The system designer should note that some of the reserved pins have internal pullup resistors. Also note that the JTAG pins in Table 1 are NOT 3.3-V tolerant. These pins are powered from the VDD_IO supply (1.5 V or 1.8 V). See the XIO1100 datasheet for the electrical characteristics of VDD_IO pins.

Table 1. JTAG Pins

Pin #	Description
B9	JTAG_TCK. This pin has a weak internal pullup resistor.
A10	JTAG_TDI. This pin has a weak internal pullup resistor.
B10	JTAG_TDO
A9	JTAG_TMS. This pin has a weak internal pullup resistor.
C9	JTAG_TRST

3 NAND Tree Pin Order

Table 2 shows the pin order of the NAND tree. The pins must be toggled in the order listed. The result of the NAND logic can be observed on the JTAG_TDO pin.

Table 2. NAND Tree Pin Order

Order	Pin Name
1	TX_DET_LOOPBACK
2	TX_ELECIDLE
3	TX_COMPLIANCE
4	TX_CLK
5	TX_DATA0
6	TX_DATA1
7	TX_DATA2
8	TX_DATA3
9	TX_DATA4
10	TX_DATA5
11	TX_DATA6
12	TX_DATA7
13	TX_DATA8
14	TX_DATA9
15	TX_DATA10
16	TX_DATA11
17	TX_DATA12
18	TX_DATA13
19	TX_DATA14
20	TX_DATA15
21	TX_DATAK0
22	TX_DATAK1
23	RX_DATA0
24	RX_DATA1
25	RX_DATA2
26	RX_DATA3
27	RX_DATA4
28	RX_DATA5
29	RX_DATA6

30	RX_DATA7
31	RX_DATA8
32	RX_DATA9
33	RX_DATA10
34	RX_DATA11
35	RX_DATA12
36	RX_DATA13
37	RX_DATA14
38	RX_DATA15
39	RX_DATAK0
40	RX_DATAK1
41	RX_STATUS0
42	RX_STATUS1
43	RX_STATUS2
44	RX_ELECIDLE
45	RX_POLARITY
46	RX_VALID
47	P1_SLEEP
48	POWERDOWN0
49	POWERDOWN1
50	PHYSTATUS
51	JTAG_TCK
52	JTAG_TDI
53	DDR_EN
54	CLK_SEL

4 Performing the NAND-Tree Test

4.1 Putting XIO1100 PHY into NAND-Tree Mode

To put the XIO1100 PHY into NAND-tree mode, software must set bit 2 in the TESTMODE register. The TESTMODE register is 32-bits in length and is located at JTAG OPCODE 0x2. The default value of this register should be 0x00000000. It is important that the software set only bit 2. Once bit 2 is set to a ‘1’, the XIO1100 PHY is in NAND-tree mode.

4.2 Stepping Through the NAND Tree

Once the XIO1100 has been put into NAND-tree mode, the I/O pins listed in Table 2 should all be driven low. Once all I/O pins are low, the JTAG_TDO pin should be high.

At this point, the logic controlling the pins listed in Table 2 can toggle the first pin from low to high and the observed JTAG_TDO from high to low. This indicates the first pin is connected properly.

The logic controlling the pins should then leave the first pin high and then toggle the second pin from low to high. The JTAG_TDO pin should go from low to high. This indicates that the second pin is connected properly.

Pins 1 and 2 should be left high and then the logic should toggle pin 3 from low to high. The JTAG_TDO pin should go from a high to low. This indicates that the third pin is connected properly.

The logic should continue this sequence for every pin listed in Table 2. Every pin in Table 2 that causes JTAG_TDO to toggle high-to-low or low-to-high indicates a good connection. If JTAG_TDO fails to toggle when a pin in Table 2 toggles from low to high, the pin has a bad connection.

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