

# **Protecting RS-485 Interfaces Against Lethal Electrical Transients**

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## **ABSTRACT**

Industrial networks must operate reliably in harsh environments. Electrical over-stress transients caused by electrostatic discharge, switching of inductive loads, or lightning strikes, will corrupt data transmission and damage bus transceivers unless effective measures are taken to diminish transient impact.

This article gives an overview of the three most commonly applied transient immunity tests, and provides recommendations on how to protect network nodes against real world transients.

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## 1 Transient Immunity Tests

The following three transient immunity tests are part of the IEC61000-4 family of electromagnetic compatibility tests, specified by the International Electrotechnical Commission (IEC).

### 1.1 Electrostatic Discharge (ESD) Immunity

The Electrostatic Discharge (ESD) Immunity test, IEC61000-4-2, simulates the electrostatic discharge of an operator directly onto an adjacent electronic component. Electrostatic charge usually develops in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the equipment-under-test (EUT), which can happen via direct contact with the EUT (contact discharge), or via an air-gap (air-discharge).

Characteristic for this test are the short rise time and the short pulse duration of less than 100ns, indicating a low-energy, static pulse. This test requires a minimum of 10 single discharge of positive and negative polarity with a recommended time interval between discharges of 1 second.

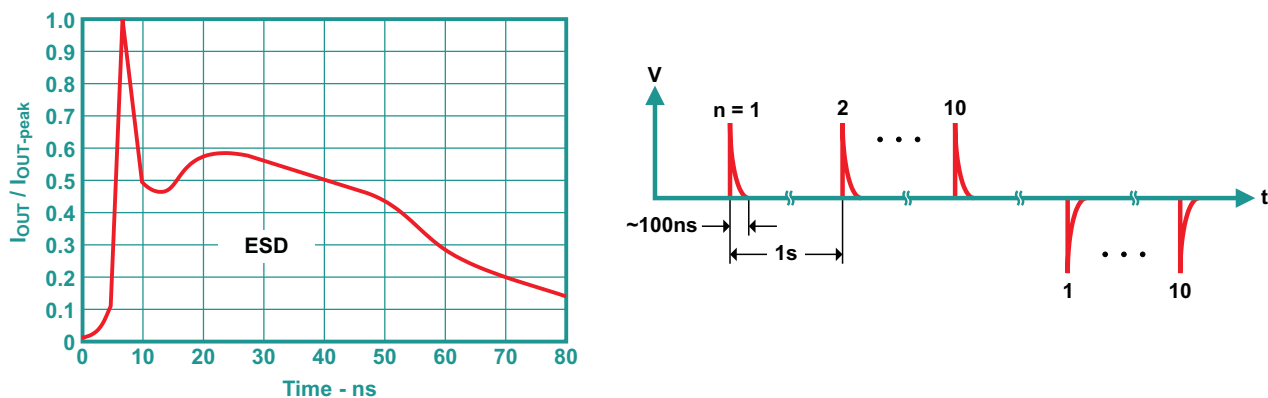


Figure 1. Current Wave Form of ESD Pulse and Timing Sequence of Pulses

The test procedures of many electronic equipment manufacturers ascribe ESD tests the lowest priority of all transient immunity tests as their potential occurrence is limited to the handling, installation and maintenance work of input modules, during which operators are advised to wear ESD protective clothes as well as to intentionally discharge themselves prior to any direct contact with the module.

### 1.2 Electrical Fast Transients (EFT) Immunity

The test for Electrical Fast Transients (EFT) or Burst Immunity, IEC61000-4-4, represents the most important test as it simulates the everyday switching transients caused by the interruption of inductive loads, relay contact bounce, etc. This test is performed on power-, signal-, and Earth wires. A burst is defined as the sequence of pulses of limited duration. In this case, a burst generator produces a sequence of test pulses with a decay time, (down to 50% of the peak value), of less than 100ns. The typical duration of a burst is 15ms at a repetition rate of 5 kHz. The burst period, the time from one burst start to the next, is 300ms. Significant for the test pulse are its short rise time, the high repetition rate, and its low energy content. This test requires the application of six burst frames of 10 seconds duration with 10 seconds pause intervals between frames.

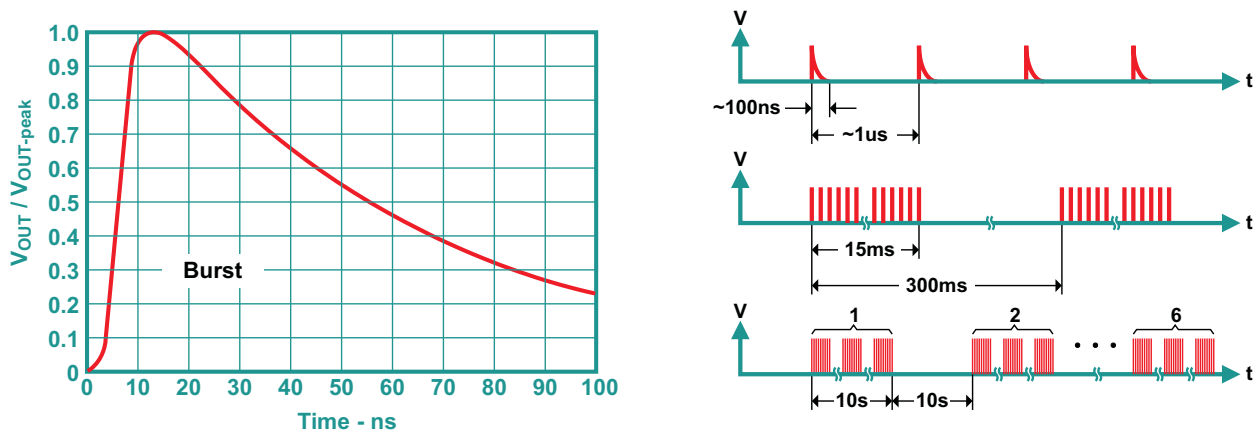


Figure 2. Voltage Wave Form of an EFT (Burst) Pulse and Timing Sequence of an Entire Test Cycle

While the fast rise time and the low energy content of an EFT are similar to the ones of an ESD pulse, the number of pulses per test cycle is not. Assuming a 1µs interval between pulse-front to pulse-front, an EFT burst of 15ms duration contains at least 15000 pulses. Multiplied by the number of bursts within a 10s window, which is 10s/300ms = 33.3 bursts, yields 500,000 pulses per 10s window. Thus the application of six 10s windows with a 10s pause interval results in a cool 3 million pulses within 50 seconds. This sheer endless pounding of transients upon the EUT appears to become an insurmountable task for the protection circuit to survive.

However, since the EFT testing does not involve the direct contact of conductors but rather the indirect application via a capacitive clamp, the choice of a proper, industrial RS-485 cable with internal shielding can produce a remedy to the DUT by attenuating the coupling of EFT energy into the conductors.

### 1.3 Surge Immunity

While the **Surge Immunity Test, IEC61000-4-5**, is the most severe transient immunity test in points of current and duration, its application is often limited to long signal and power lines (L > 30m). This test simulates switching transients caused by lightning strikes, (direct strike or induced voltages and currents due to an indirect strike), or the switching of power systems including load changes and short circuits.

The surge generator's output waveforms are specified for open- and short-circuit conditions. The ratio of the open-circuit peak-voltage to the peak short-circuit current is the generator output impedance. Characteristic for this test are the high current, due to low generator impedance, and the long pulse duration, (approximately 1000-times longer than for ESD and Burst tests), indicating a high-energy pulse.

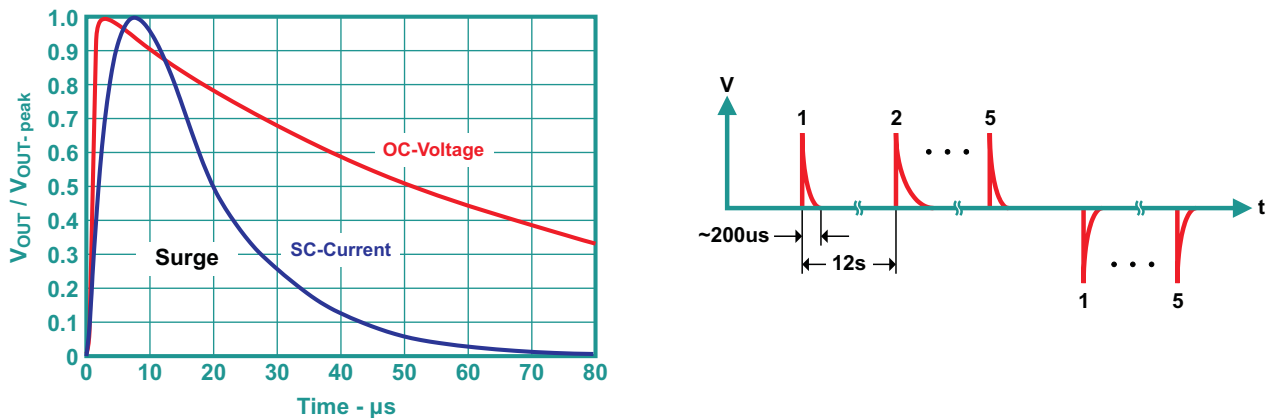


Figure 3. Voltage and Current Wave Form of a Surge Pulse and Timing Sequence of a Test Cycle

This test requires 5 positive and 5 negative surge pulses with a time interval between successive pulses of 1 minute or less. A common procedure is to shorten the pause intervals down to 12 seconds, thus reducing total test time below 2 minutes. While this approach intensifies the surge impact, due to the protection circuits reduced recovery time between pulses, it contributes to a significant reduction in test cost.

## 2 Test Levels and Priority

To protect electronic equipment adequately against electrical transients regional standard bodies have established a list of transient immunity test requirements which can vary in the level of test voltages applied. [Table 1](#) lists a typical set of requirements and their applied test levels for industrial applications.

**Table 1. EMC Test Requirements**

Priority	Immunity Test	Standard	Port	Voltage	Level
1	Burst	IEC61000 - 4 - 4, (5/50ns via capacitive clamp)	Power lines	±4kV	4
			Signal lines	±2kV	4
2	Surge	IEC61000 - 4 - 5, (1.2 / 50µs–8 / 20 µs), 42Ω–0.5µF	Signal lines	±0.5kV	1
		IEC61000 - 4 - 5, (1.2 / 50µs–8 / 20 µs), 2Ω–18µF	Power lines	±1kV	2
3	ESD	IEC61000 - 4 - 2, in air gap	Power and signal lines	±15kV	4
		IEC61000 - 4 - 2, in contact	Power and signal lines	±8kV	4

1. Because the Burst test simulates the everyday switching transients, it has the highest priority of the three transient immunity tests. While low in energy content, the vast numbers of transients continuously bombard the protection circuitry without much time for recovery.
2. The surge test, although of far less occurrence, ranks next due to its high energy content and lethal impact on electronic components. It is important to notice that lightning, can produce current surges in the range of tens of thousands of amps (10kA to 100kA). While primary protection devices located at a building's boundary, try to diminish the initial surge as much as possible, the remaining currents between 1kA to 4kA can still traverse along power lines into the building. Their large magnetic fields can easily couple into adjacent data communication lines if proper shielding is not applied.
3. The test of least importance is the one for ESD immunity. It is proven that the main cause of ESD failures in the field is due to human involvement during the rare events of network installation and maintenance. Furthermore, the enforcement of wearing ESD protective clothing during these activities reduces the risk of electrostatic discharge to a minimum.

### 3 Pass-Criteria

There are three pass-criteria defining of how well a device or equipment must perform during and after a transient test.

- Criterion A allows no performance degradation during the application of noise transients, thus requiring normal operation during and after the test. With regards to the RS-485 or CAN bus, this means that the bit-error-rate of the data transmission should stay consistently low.
- Criterion B accepts some degradation in performance, such as unintentionally logic-state changes, which inevitably will lead to a BER increase. However, after the test, the system must be self-recoverable and return to normal operation.
- Criterion C accepts the loss of function, such as a latch-up event, but without device damage. After test, a manual restart or toggling of the power supply is necessary to return the system to normal operation.

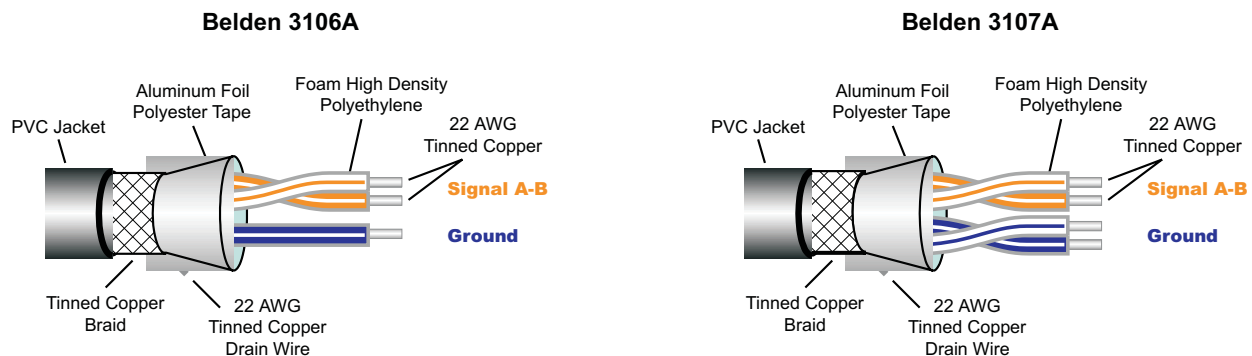
While the data sheets of many transceiver devices claim high ESD protection levels of up to 30kV, they often fail to state the pass-criterion applied. Therefore, during ESD testing expect the BER to increase as many devices are designed with criterion B in mind.

Also relying solely on a transceiver's integrated ESD structure when designing a data link for real world application, may fail. A robust data link requires external protection circuitry to absorb the much higher impact of burst and surge transients.

### 4 Protection Circuitry

Reliable protection against electromagnetic interference begins with the right choice of transmission cable. Choosing industrial RS-485 cable over cheap unshielded twisted pair (CAT5) or flat-band cable has two major advantages:

1. The cable's nominal characteristic impedance of  $Z_0 = 120 \Omega$  matches the switching characteristics of RS-485 transceivers, thus minimizing signal distortion caused by reflections due to impedance mismatch,
2. The braided shield provides substantial attenuation to noise currents induced by burst and surge transients, thus reducing the impact on subsequent transient protection devices.



**Figure 4. Industrial 2-Pair and 1.5-Pair RS-485 Cables With Shield and Drain Wire**

Although industrial RS-485 cable is available with up to 4 signal-pairs, [Figure 4](#) shows only a 1.5-pair and a 2-pair sample for half-duplex data links. In both cases, one signal pair connects to the A and B terminal of an RS-485 board connector, and the ground conductor(s) plus the drain wire connect to the ground terminal of the connector. Using an entire signal pair for the ground connection, as in the case of the Belden 3107A cable, assures a lower ground inductance path for transient currents returning from the board than the single ground conductor of the Belden 3106A cable.

[Figure 5](#) shows the circuit schematic of a basic RS-485 node. A screw terminal, serving as the RS-485 connector, connects the transmission cable to the transceiver (XCVR). Three transient voltage suppressor diodes (TVS) are used to eliminate common-mode transients between A and ground and B and ground, and differential transients between A and B.

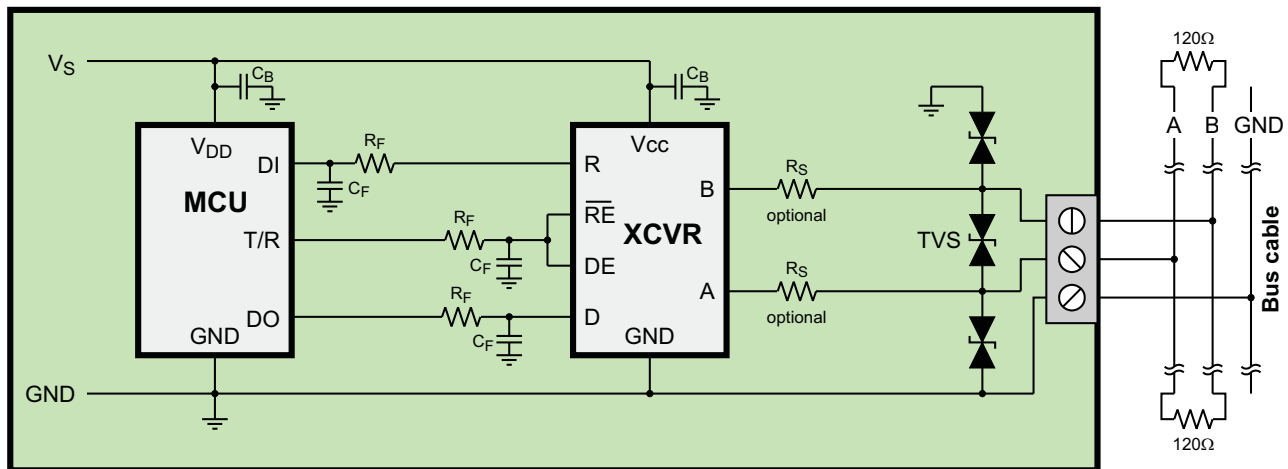


Figure 5. Protection Circuitry for Transient Immunity

Modern transient voltage suppressors are the preferred protection components for high-speed data transmission due to their low capacitance, which allows them to be designed-in into every node of a multi-node network without requiring a reduction in data rate. With response times of a few picoseconds and power ratings of up to several kilowatts TVS diodes present the most effective protection against ESD, burst, and surge transients.

Figure 6 shows the V-I characteristics of a TVS. Up to the stand-off voltage,  $V_{WM}$ , the transient suppressor is high-impedance and only a few micro-amps of leakage current pass through the device. Therefore, when selecting a TVS make sure its stand-off voltage is above or equal to the maximum bus voltage potential during normal operation,  $V_{WM} \geq V_A, V_B$ .

At the break-down voltage,  $V_{BR}$ , the TVS begins clamping, that is the device becomes low-impedance and starts conducting high current. Due to its dynamic impedance, current flowing through the TVS creates a voltage drop, known as the clamping voltage,  $V_C$ . This voltage rises with increasing current. Unfortunately, the clamping voltage often exceeds the maximum voltage ratings of a transceiver's bus terminals.

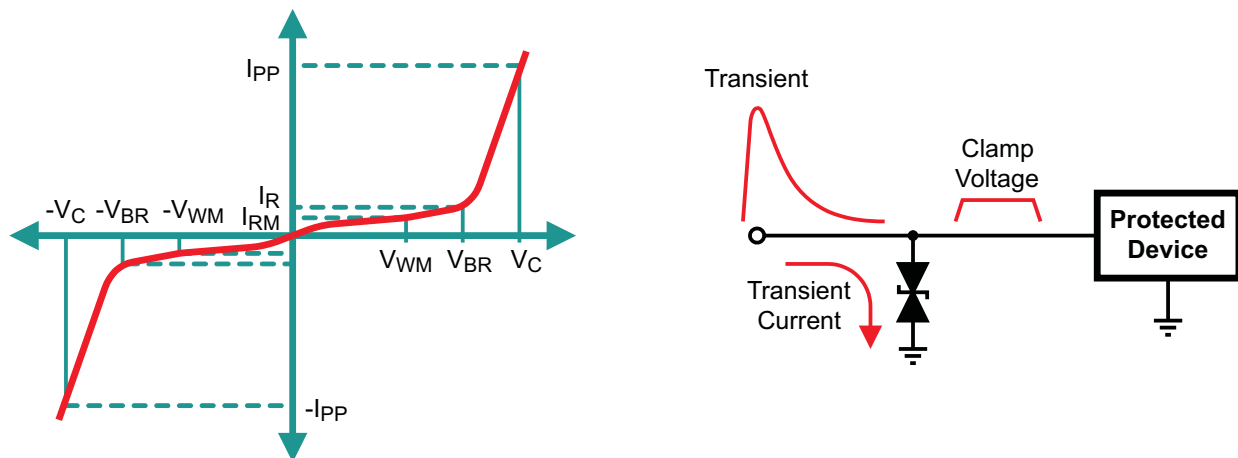


Figure 6. TVS Characteristics and Clamp Voltage Impact

For example, to comply with the RS-485 specified common-mode voltage range of  $-7V$  to  $12V$ , TVS stand-off voltages should be  $V_{WM} \geq 12V$ . Depending on the power rating of the TVS chosen, the maximum clamp voltages can range from  $25V$  up to  $35V$ , which is significantly higher than the maximum bus voltage of  $14V$  of a standard transceiver. In this case, the internal protection circuit of the transceiver must absorb the remaining clamp energy to protect the device from damage.

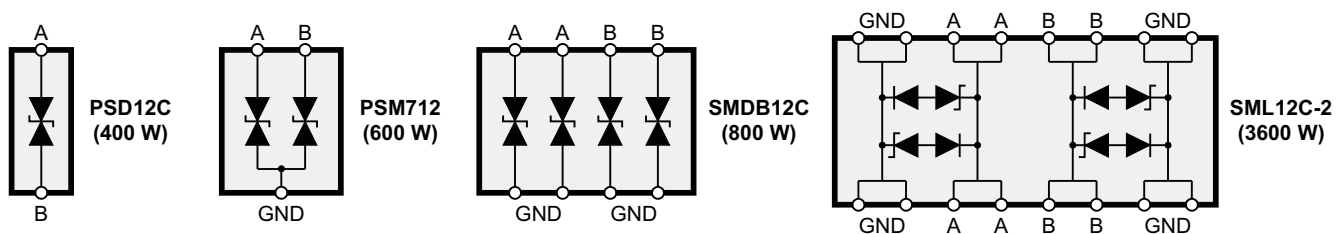
For ESD and burst transients, the clamp energy is low due to the short pulse duration, and does not pose a problem to the internal ESD cells. Clamp energy from surge transients; however, can present a serious challenge due to the much longer pulse duration. For transceivers specified with low ESD immunity, it may be necessary to reduce the remaining current flowing into the transceiver through series resistors. Common resistor values range from 10Ω to 20Ω. Note these resistors must be surge-rated to provide high pulse robustness.

In addition to the suppressor action on the transceiver bus side, further protection against signal degradation is required on the transceiver single-ended side. This is accomplished with R-C low-pass filters which filter transient remnants in the receive path, and stop high frequency noise from entering the transmit path.

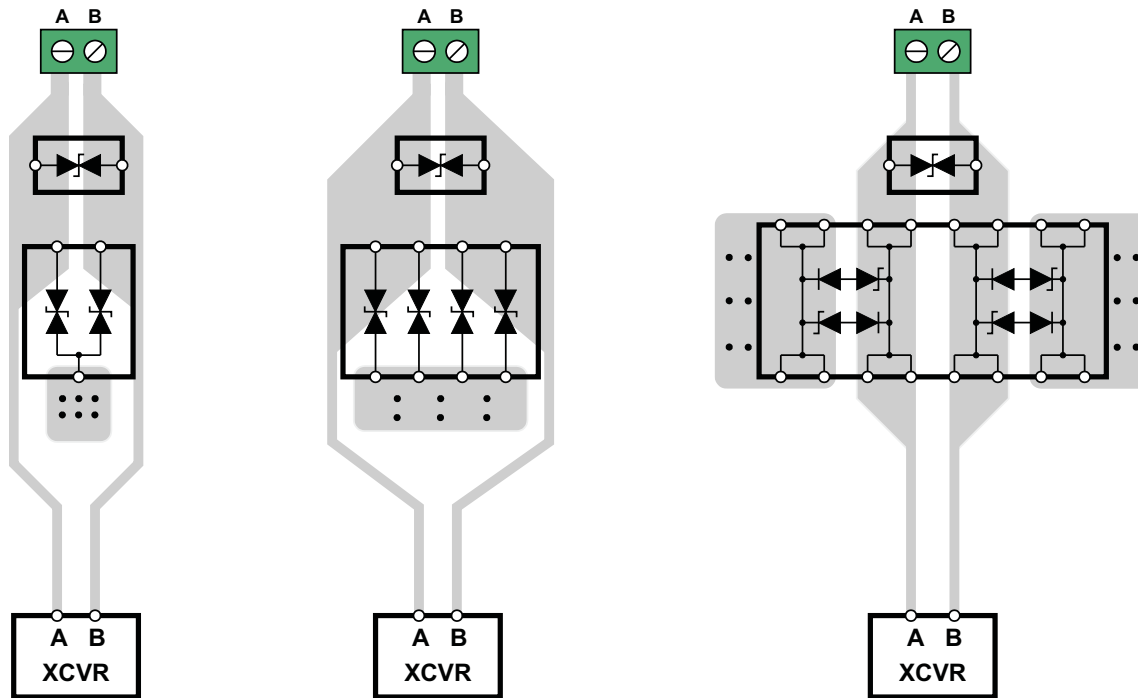
## 5 Guidelines for Circuit and PCB Design

**Do not treat transient protection as an add-on feature, instead plan for it at the beginning of the design.**

- To accomplish an EMI robust board design, use a four-layer PCB with layer stacking in the following order (top-to-bottom): Bus signal layer, ground plane, power plane and control signal layer.
  - Routing the differential signal traces on the top layer avoids the need for vias (and the introduction of their inductances) and allows for clean interconnects between the connector and the transceiver.
  - Placing a solid ground plane next to the bus signal layer provides an excellent low-inductance path for return currents and establishes controlled impedance for transmission line interconnects.
  - Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in<sup>2</sup>.
  - Routing the control signals on the bottom layer provides greater routing flexibility as these signal links have margin to tolerate discontinuities such as vias.
- When choosing a transient suppressor diode assure that the stand-off voltage is above the expected common-mode voltage range, which can be smaller or larger than the -7V to 12V specified by EIA-485.
- In addition to select a TVS with sufficient power rating, look for a device topology that allows smooth routing of the signal traces between the connector and the transceiver. Figure 7 presents some TVS diodes with 12V stand-off voltage, but different power ratings and topologies, and Figure 8 provides routing suggestions for minimum inductance paths, based on the TVS component layout.



**Figure 7. TVS Diodes in Various Topologies and Power Ratings**



**Figure 8. Routing Options for Different Topologies**

- Do not let the transients pass across the circuit board. Eliminate them right at the board entrance by placing the transient voltage suppressors as close to the connector as possible.
- Ground TVS with multiple ground vias to make inductance between TVS and ground plane lower than the signal trace inductance between TVS and transceiver. Note that transients contain high-frequency components which follow the path of least inductance.
- Introducing some distance between the TVS and the transceiver is recommended as it increases the signal trace inductance. This approach not only makes the signal trace the less preferred path for transients, it also slows down the edges of any transient remnants.
- For transceivers with low ESD rating insert surge-rated 10Ω to 20Ω MELF resistors in series to the transceiver bus terminals to reduce the remaining TVS clamp energy.
- Implement EMI filtering on the single-ended side of the transceiver through simple R-C low-pass filters.
- Apply 100nF by-pass capacitors as close as possible to every IC. Ground each capacitor with at least two vias to the ground plane to reduce the total via inductance. Note, because of  $V = L \times di/dt$ , even small inductances can cause significant high voltages due to fast transient rise times.

## 6 Conclusion

Electrical over-stress transients, such as ESD, burst, and surge pulses vary in rise time, duration and energy content. Protecting RS-485 network nodes against these transients requires more than just a high ESD rating of the transceiver. Industrial RS-485 cabling in combination with external transient voltage suppressors placed closely to the bus connector provide the most efficient protection against all three types of transients.

## 7 References

- Further information on RS-485 transceivers is available at [www.TI.com/interface](http://www.TI.com/interface) .
- For information on low-capacitance transient voltage suppressors visit [www.protekdevices.com](http://www.protekdevices.com), [www.semtech.com](http://www.semtech.com), and [www.vishay.com](http://www.vishay.com) .
- For information on industrial RS-485 cable visit [www.Beldencable.com](http://www.Beldencable.com) .



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