Application Report
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Considerations for PCB Layout and Impedance Matching Design in Optical Modules

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ABSTRACT

The optical module offers an effective high-speed solution for a growing telecom market. Data rates range from 155 Mbps to 6 Gbps and even up to 10 Gbps. Transmitter optical sub-assemblies (TOSAs) and laser drivers may have different resistances in a given application, so the reflection could be worse if the designer does not use an impedance transfer circuit to absorb it. Additional uncertain noise and reflection could also come from poor printed circuit board (PCB) layout as well. This report discusses how to use the impedance transfer circuit when we connect a mismatched trace and non-terminated TOSA, as well as what we should take into consideration when we lay out the PCB for optical design. This document primarily refers to the ONET8501V VCSEL driver and the ONET1101L DFB driver as the devices under consideration.

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1 Introduction

The optical module offers an attractive high-speed solution for a growing telecom market. Data rates range from 155 Mbps to 6 Gbps and are now approaching 10 Gbps. In such ultra high-speed frequency areas, close attention must be paid to the PCB layout and impedance matching because these issues can seriously affect the output performance and destroy the results.

Generally, impedance matching is modeled by software simulation or manual computations. However, optical modules are an application with several constraining factors: frequency over Gbps; variations in the laser driver model; the actual transmission lines; and, most importantly, the laser TOSA. These factors often make it difficult to simulate impedance matching precisely. As a result, even with good models to predict the operating conditions with relative accuracy, designers often cannot easily obtain results that match well with actual measurements.

In the optical design approach discussed in this document, impedance mismatch results in reflection. We will use a 10-G direct modulater laser (DML) module board as our example. Figure 1 shows the four reflection points that occur when using this type of DML board.

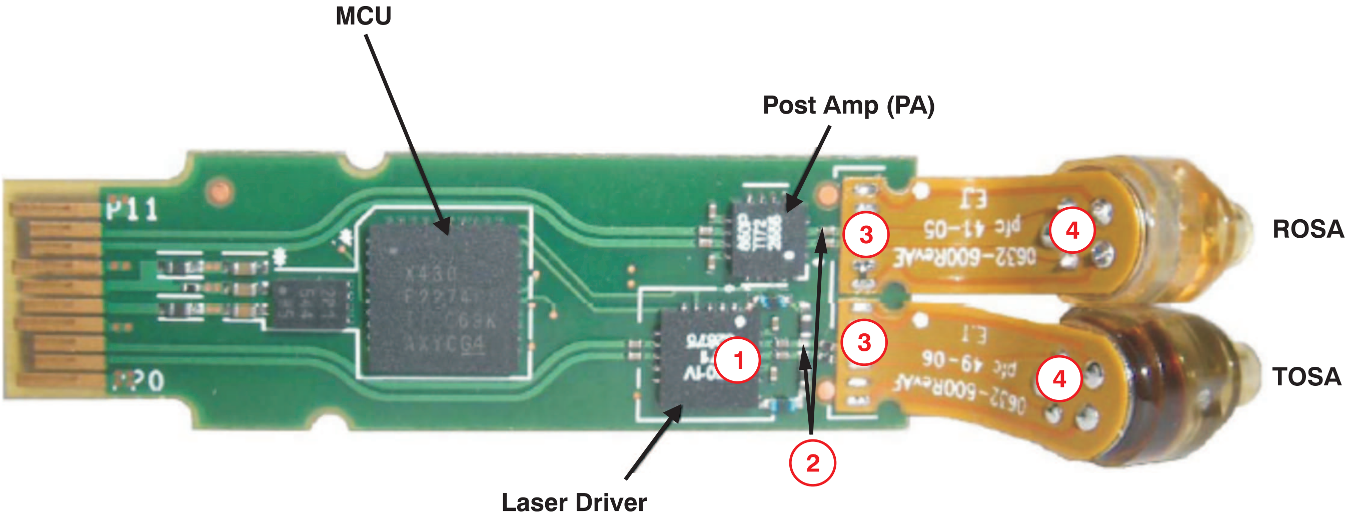


Figure 1. Reflection Points on an Optical Module

The technique discussed here includes an analysis of the signal path that can generate reflections from the driver to the laser (TOSA) in four areas:

1. The IC pin to the trace
2. The PCB trace on board
3. The PCB trace to the flex cable
4. The flex cable to TOSA (ROSA) elements

At point 2, the reflection is primarily generated by the PCB layout. For the other points, the reflections are a result of impedance mismatching. At an impedance mismatch, a portion of the transmitted signal is reflected back towards the signal source, and it can propagate back and forth in the trace until it is attenuated. The reflected signals can interfere with the primary transmitted signal, increasing the data jitter and reducing the SNR. The reflected energy can be terminated by a driver based on the SDD22 specification. If the reflected energy is too high, we need an additional circuit to optimize the impedance matching so that the reflected energy can be absorbed.

2 Impedance Transfer Circuit Considerations

It is well known that the amount of reflected signal from the load depends on the degree of mismatch between the source impedance and the load impedance. The reflection coefficient expression is defined as shown in Equation 1:

$$\Gamma_L = \frac{V_{REFL}}{V_{IN}} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{1}$$

In this equation, Z_0 is the transmission line impedance; this factor is usually a constant with an industry normalized value such as 50 Ω or 100 Ω. In a matched system, when the load impedance Z_L matches the transmission line impedance, $\Gamma_L = 0$ and we have zero reflection. This objective is the target of the circuit design.

In the receiver portion of the optical design, the input and output of the limiting amplifier and the output of the transimpedance amplifier are all 100-Ω differential impedance; thus, the transmission lines are 100-Ω differential, and matching is relatively easy.

However, the transmitter part is not so simple to design. A distributed feedback (DFB) or Fabry-Perot (FP) laser is a low-resistance component, typically ranging from 7 Ω to 10 Ω. The flexible PCB cable is commonly a 25-Ω, single-ended trace. There is a reflection at the interconnection between the flex cable and the TOSA at point 4; refer to Figure 1. For reducing such reflection, some types of TOSAs integrate resistors to increase the TOSA impedance, as illustrated in Figure 2.

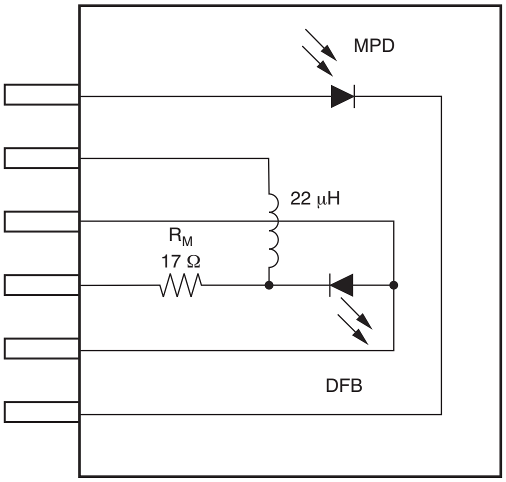
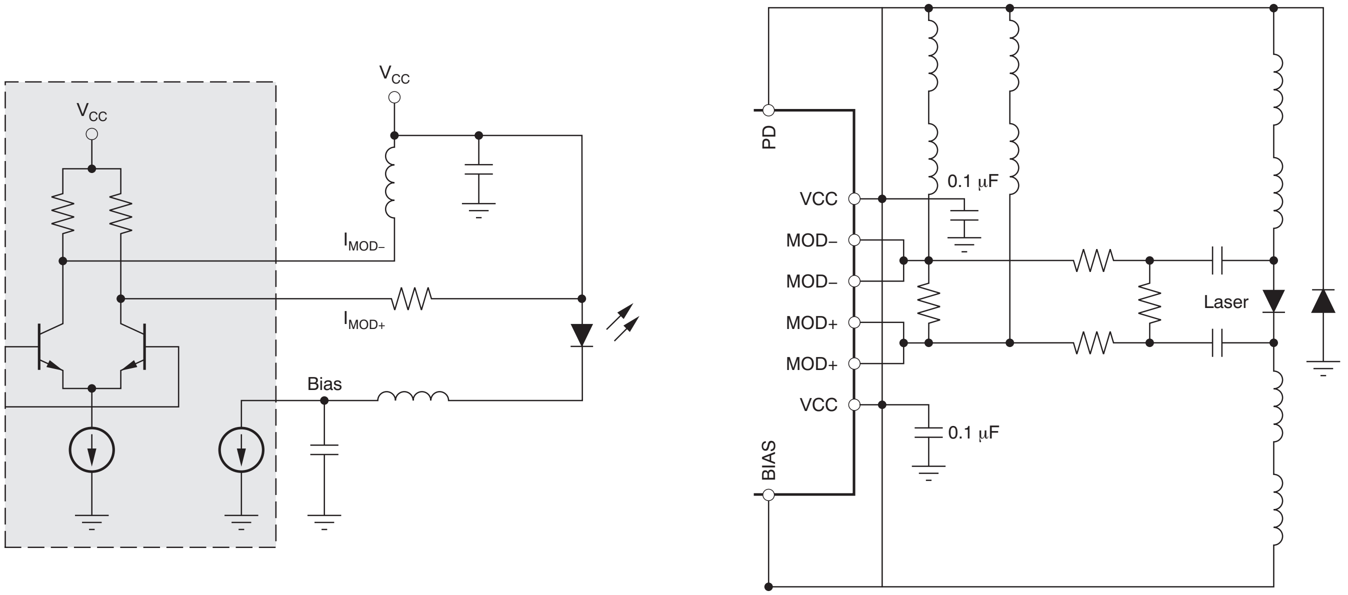


Figure 2. Internal Structure of Terminated TOSA

Such TOSAs are intended for single-ended applications. The total internal resistance is close to 25 Ω and the transmission line can be more easily matched to the TOSA with a minimum amount of reflection. However, many optical designers prefer to use differential mode rather than single-ended mode to avoid issues with common-mode noise and electromagnetic interference (EMI).

Figure 3 compares an optical module driver in both single-ended (**a**) and differential (**b**) modes.



A) Single-Ended Mode B) Differential Mode

Figure 3. Optical Module Drive Modes

In order to match the 50-Ω differential transmission lines in differential mode, a fully-matched TOSA with two 20-Ω internal resistors, together with the laser resistance, results in a load resistance close to 50 Ω. One potential problem is that the resistors consume current and heat the laser, which reduces the overall efficiency of the laser. The driver must supply more modulation and bias current to maintain the extinction ratio (ER) and average optical power (PAV) setting because of the higher temperature of the laser. The greater power consumption makes such fully-matched TOSAs very difficult to use, especially for SFP+ modules that require a total power dissipation of less than 1 W. Because of this power consumption effect, many customers have switched to unmatched TOSAs without internal resistors. The TOSA reflection is inevitable and relies on the driver or impedance transfer circuit to absorb the reflected energy. In recent years, most optical customers have transitioned their designs to use unmatched TOSAs.

3 Examples for Impedance Transfer Analysis

This section reviews several examples for the impedance transfer analysis.

3.1 Impedance-Matched Systems

An impedance-matched system, such as that illustrated in Figure 4, does not need an impedance transfer circuit.

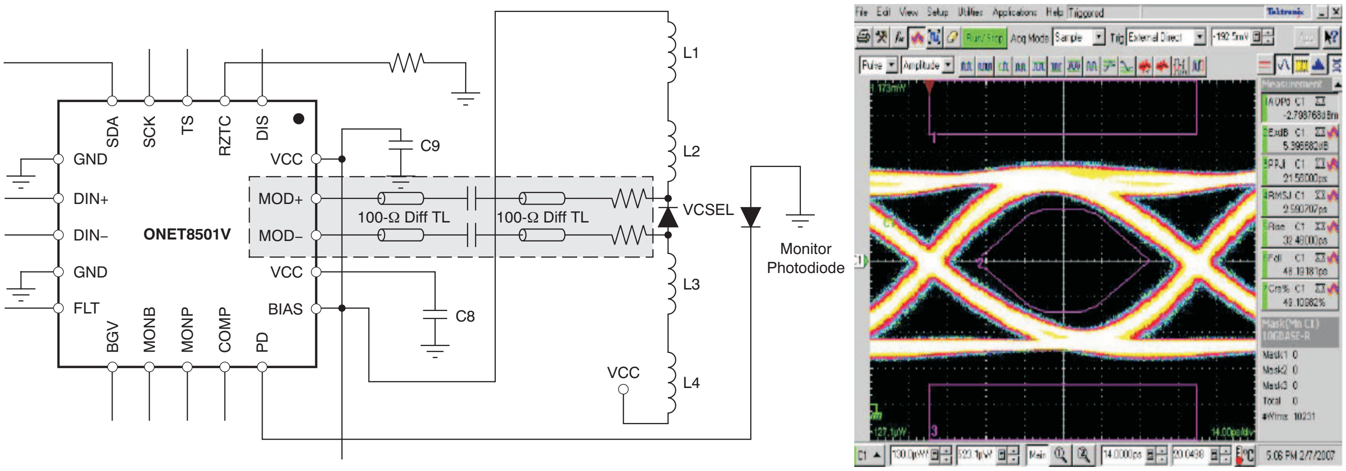


Figure 4. Matched System

In the ONET8501V application presented here, the output impedance is 100-Ω differential; the transmission line is also 100 Ω, and the load is 100-Ω VCSEL TOSA. The resistance matches very well and produces minimum reflection.

3.2 Impedance Transfer for Mismatched Source and Load

Figure 5 illustrates the impedance transfer configuration for a mismatched source and load.

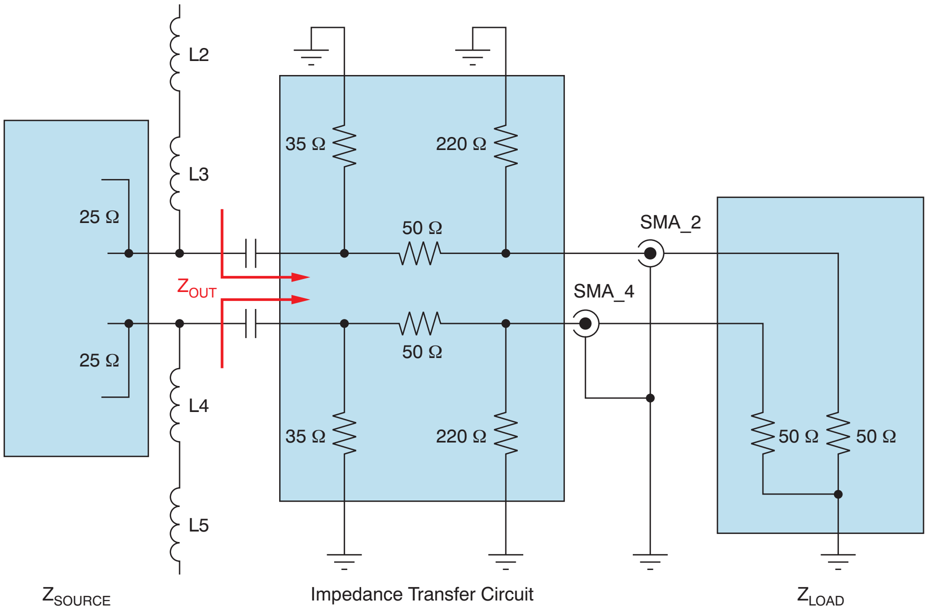
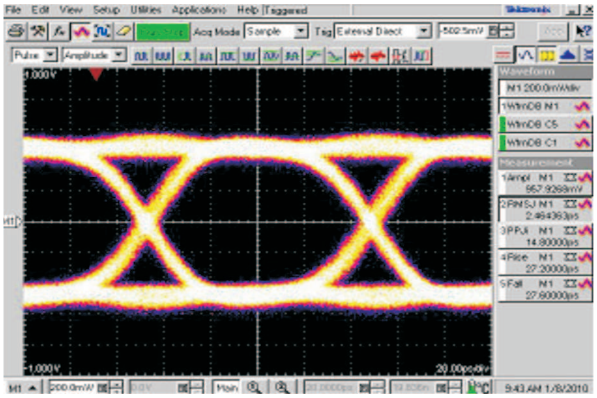


Figure 5. Impedance Transfer for Mismatched Source and Load

The laser driver is 50-Ω differential output and the test load impedance is 100-Ω differential in order to transfer the impedance between the source and load, using the π resistor network to build up the impedance transfer circuit. Grounding with 35-Ω and 220-Ω resistors and a 50-Ω series resistor, the greatest amount of reflection could be attenuated by this circuit. The transfer equation illustrated in Figure 5 is given in Equation 2:

$$Z_{OUT} = (220 \,//\, \frac{1}{2} Z_{LOAD} + 50) \,//\, 35 \tag{2}$$

Z_{LOAD} is 100-Ω differential; therefore, we calculate Z_{OUT} by using half of Z_{LOAD}. The final Z_{OUT} value is 27 Ω, which is very near to the front transmission line resistance. This Z_{OUT} can even generate the eye diagram shown in Figure 6.



1 Ampl M1 957.9268mV
2 RMS J M1 2.464363ps
3 PPJ M1 14.80000ps
4 Rise M1 27.20000ps
5 Fall M1 27.60000ps

Figure 6. Eye Diagram After the Impedance Transfer Circuit

3.3 Impedance Transfer for TOSA and Laser Driver Matching

Figure 7 shows the ONET1101L driving an unmatched TOSA in differential mode.

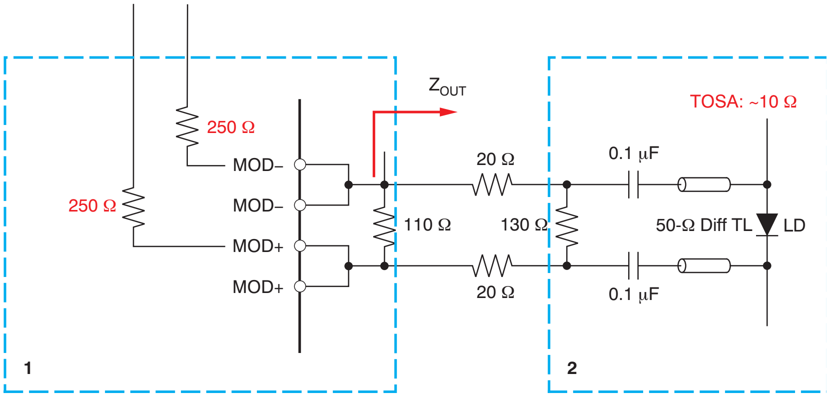


Figure 7. Impedance Transfer Circuit for TOSA and Driver

The ONET1101L laser diode driver is optimized to drive a 50-Ω differential output transmission impedance. For a low-power design, it has a 500-Ω differential back termination. Because the LR DFB TOSA has only 10-Ω impedance (approximately), the reflection is much worse if there is no transfer circuit added. The purpose of the transfer circuit is to drive the load impedance close to 50 Ω from the driver side. From Figure 7, we can derive Equation 3:

$$Z_{OUT} = R_1 // (R_3 + R_4 + R_2 // R_{TOSA}) \tag{3}$$

With the resistor values shown, Z_{OUT} is approximately 35 Ω.

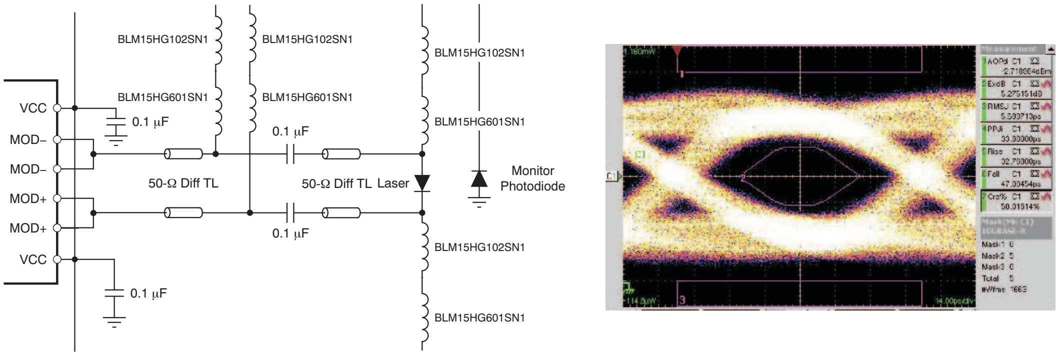
We can then analyze the transfer circuit in the following manner:

1. R_1 combines with the internal driver differential resistance to create a new back termination: Z_S', highlighted in the blue outlined area (1) in Figure 7. The new Z_S' will be 90 Ω. For best results, R_1 should connect as closely as possible with the IC pins.
2. R_2 combines with the TOSA impedance to form a new Z_L', shown in the blue outlined area (2) in Figure 7. The new Z_L' will be very near 9 Ω. With the two serial 20-Ω resistors, the impedance is approximately 50 Ω, which matches the transmission line impedance.

4 Test Results

In the actual test, the values of resistors R_1 and R_2 can be adjusted to achieve the best eye diagram with the lowest power. Smaller resistor values can sometimes improve the output performance, but correspondingly increase the power consumption.

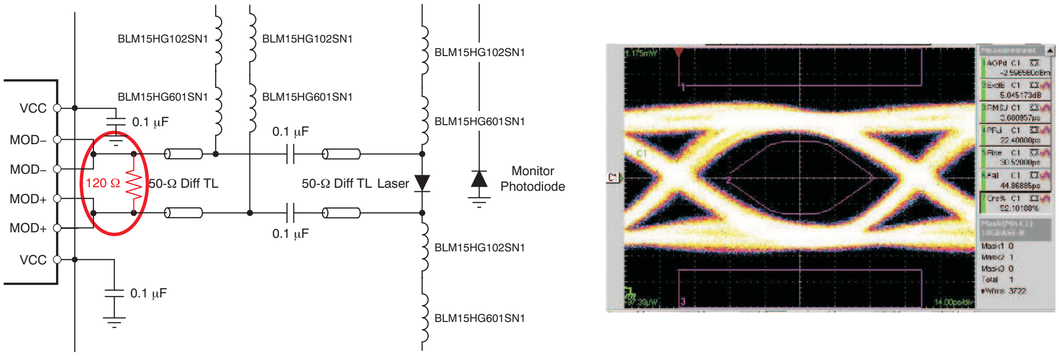
Figure 8 and Figure 9 show various test results with the ONET1101L and NX8341TB TOSA (2 × 10-Ω internal resistors).



1 AOPd C1 -2.718904dBm
2 ExdB C1 5.275151dB
3 RMSJ C1 5.593713ps
4 PPJi C1 33.00000ps
5 Rise C1 32.76000ps
6 Fall C1 47.00454ps
7 Crs% C1 50.01614%
Mask1 0
Mask2 5
Mask3 0
Total 5
#Wfms 1663

Drive directly

Bad eye diagram; MM = 0%, I_{CC} = 109 mA PRBS-31, signal 10.3125 Gbps

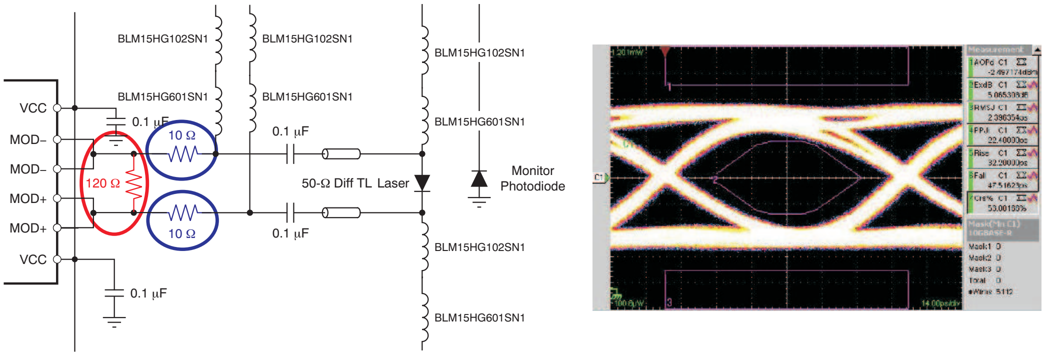


1 AOPd C1 -2.596560dBm
2 ExdB C1 5.045173dB
3 RMSJ C1 3.660957ps
4 PPJi C1 22.40000ps
5 Rise C1 30.52000ps
6 Fall C1 44.86885ps
7 Crs% C1 52.10188%
Mask1 0
Mask2 1
Mask3 0
Total 1
#Wfms 3722

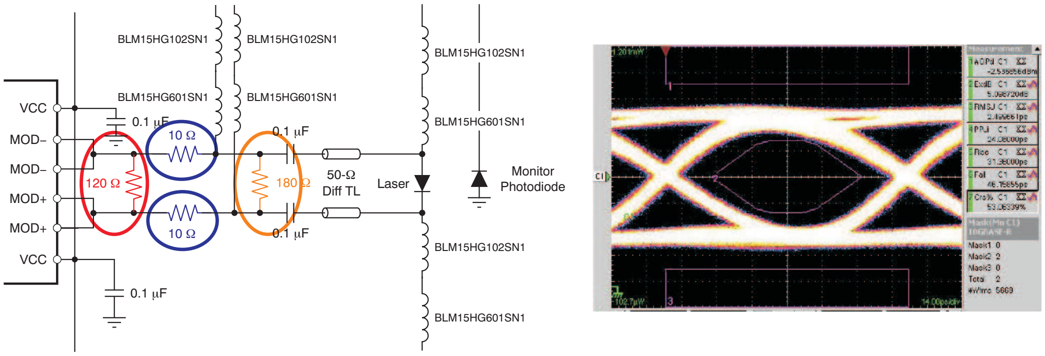
R1 = 120 Ω

Eye diagram improved; MM = 25%, I_{CC} = 121 mA PRBS-31, signal 10.3125 Gbps

Figure 8. ONET1101L Test Results: Poor Performance



Two series 10-Ω resistors Eye diagram improved, MM = 25%, I_{CC} = 131 mA, PRBS-31, signal 10.3125 Gbps



R2 = 180 Ω Eye diagram improved, MM = 25%, I_{CC} = 140 mA, PRBS-31, signal 10.3125 Gbps

Figure 9. ONET1101L Test Results: Improved Performance

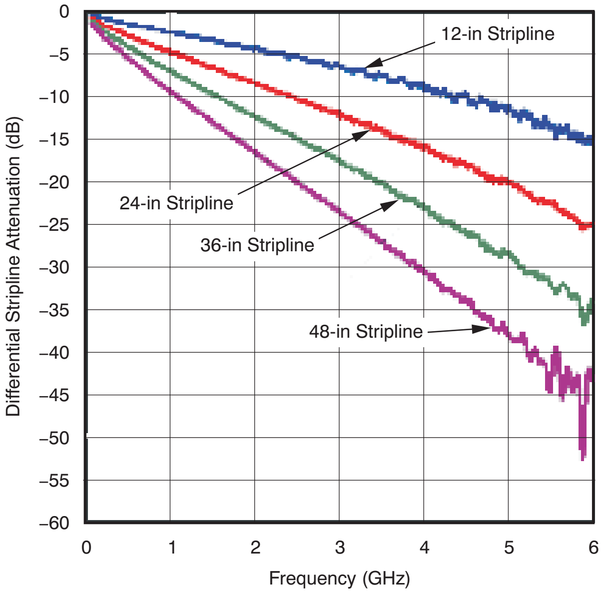
From these tests, we can see that the impedance transfer circuit works quite well to improve the module reflection performance, although the circuit also increases the power consumption at the same time. For different TOSAs and power consumption requirements, we can adjust the resistors values to achieve the best performance.

5 PCB Layout Considerations for Optical Modules

In an optical module design, PCB layout must be done very carefully because of the high-speed system. Several additional factors may affect the high-speed signal integrity.

5.1 Trace Dimensions

In high-speed PCB traces, transmission line losses depend on the frequency and the absorption of electrical energy by the dielectric. Figure 10 shows the signal loss when operatiing with different trace lengths and at different signal frequencies.



$$| \text{Loss } f, L | = e^{-(\alpha_S \bullet \sqrt{f} + \alpha_D \bullet f) \bullet L}$$

Where:

f: Frequency

α_S: Skin effect loss factor

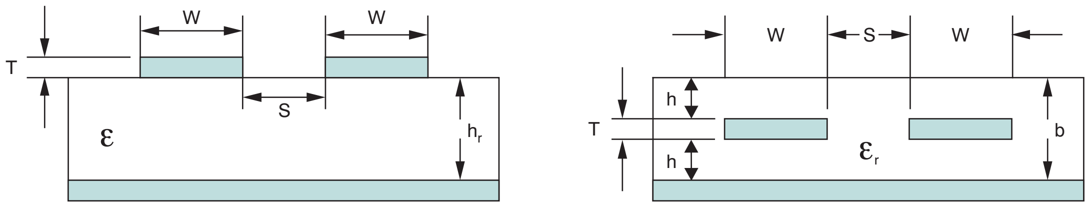
α_D: Dielectric loss factor

L: Channel length

Figure 10. Loss vs Length and Frequency

5.2 Types of Trace (Microstrip vs Stripline)

Figure 11 shows the comparison between the physical geometries of the microstrip and the stripline differential trace layouts.



Microstrip

Stripline

Figure 11. Physical Geometries of Differential Traces

Equations can also be used to calculate the transmission line impedance for a differential signal pair; note that software tools are more accurate, however. We can we calculate the two types of transmission line impedance based on the formulas shown in Table 1.

Table 1. Impedance Equations for Microstrip and Stripline Trace Techniques

Microstrip	Stripline
$Z_{DIFF}\ (\Omega) = 2 \bullet Z_0 \bullet \left(1 - 0.48 \bullet e^{-0.96\frac{s}{h}}\right)$ (4)	$Z_{DIFF}\ (\Omega) = 2 \bullet Z_0 \bullet \left(1 - 0.748 \bullet e^{-2.9\frac{s}{h}}\right)$ (5)
$Z_0\ (\Omega) = \frac{88.75}{\sqrt{\varepsilon_r + 1.47}} \bullet \ln\left(\frac{5.97 \bullet h}{0.8 \bullet W + t}\right)$ (6)	$Z_0\ (\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \bullet \ln\left(\frac{1.9 \bullet b}{0.8 \bullet W + t}\right)$ (7)
$W\ (\text{mils}) = 7.463 \bullet h \bullet e^{-\frac{Z_0 \bullet \sqrt{\varepsilon_r + 1.47}}{88.75}} - 1.25 \bullet t$ (8)	$W\ (\text{mils}) = 2.375 \bullet h \bullet e^{-\frac{Z_0 \bullet \sqrt{\varepsilon_r}}{60}} - 1.25 \bullet t$ (9)

5.3 PCB Routing

There are also several critical aspects of PCB routing that can affect the impedance matching.

- Avoid stubs and discontinuities (similar to those illustrated in Figure 12) in the PCB traces.

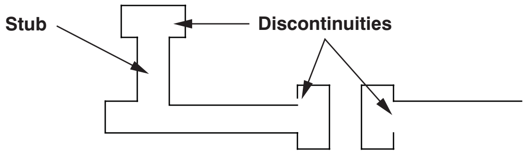
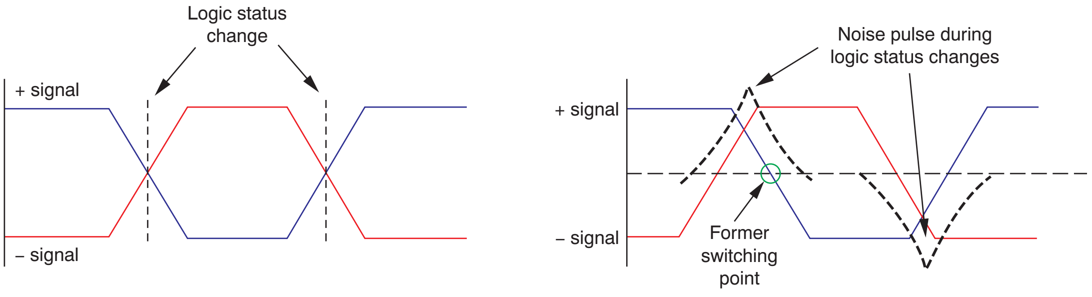


Figure 12. PCB Trace Stubs and Discontinuities

- The differential signal pairs should be the same length. Figure 13 compares differential signal pairs of the same length **(a)** and different lengths **(b)**. If the differential signal pairs are not the same length, the logic switches to zero at different times. Consequently, as shown in Figure 13**(b)**, a noise pulse will occur on the receiver.



(a) Differential Pairs: Same Length **(b) Differential Pairs: Different Length**

Figure 13. Differential Signal Pair Lengths on PCBs

- Use radial bends, shown in Figure 14, if possible. A radial bend is the best option for PCB layout in a module.

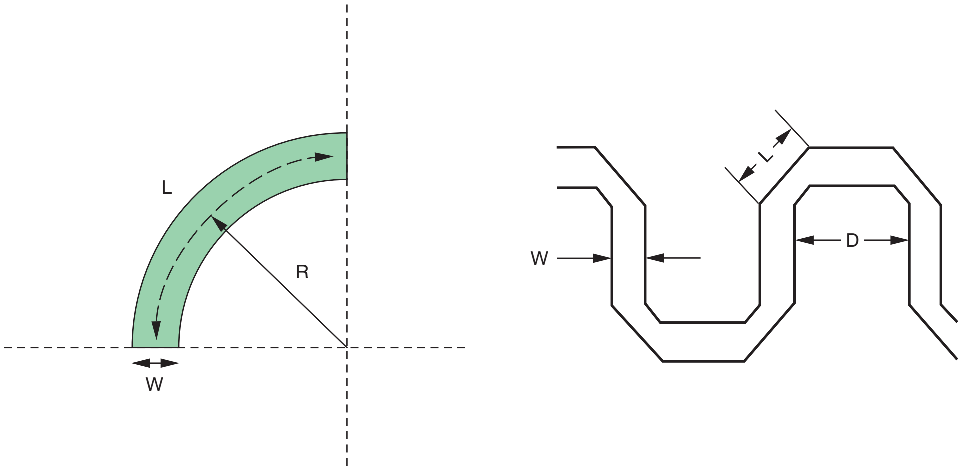


Figure 14. PCB Trace Layout with Radial Bends

R > 5 W is required to keep the trace impedance unchanged. 45-degree chamfered corners have smaller discontinuity than right-angle bends.

6 Summary

For optical module transmitter applications, some reflection is inevitable because of the small laser impedance. A transfer circuit can be added between the laser driver and the TOSA to optimize the matching and improve the overall module performance.

Particular attention must also be paid to the PCB layout for optical designs. Improvements to the trace design and layout can significantly increase the system sensitivity and eye diagram output quality.

7 References

Unless otherwise noted, these documents are available for download from the TI website (www.ti.com).

- ONET8501PB product data sheet, Texas Instruments literature number SLLS910.
- ONET8501V product data sheet, Texas Instruments literature number SLLS837B.
- ONET1101L product data sheet, Texas Instruments literature number SLLS883.
- OKI 10-G DFB OL3356l_z25 product data sheet.
- NEC NX8346TB, NX8341, ADN2526, ADN2525 series product data sheet.
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- *PCB Layout Guidelines for Designing with Avago SFP+ Transceivers*. Application report from www.avago.com.
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