TI Optical Module 10G SFP+ Total Solution

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ABSTRACT

TI 10G optical module SFP+ total solution is a complete demonstrated-working optical transceiver solution targeted for the small form factor pluggable (SFP+).

This solution reduces customer design time, thus saving customer cost without compromising performance. This is achieved by combining TI's laser driver ONET1101, limiting amplifier ONET8501 and powerful MCU MSP430 into an SFP+ multisource agreement standard package, with convincible design files and test results.

This application note provides the schematics, PC-board layout, Gerber files, bill of materials (BOM), firmware, and a graphical user interface (GUI); not only for the module but also for the evaluation board. Test setup, test data, and typical performance for assembled boards are also included in this solution.

Contents

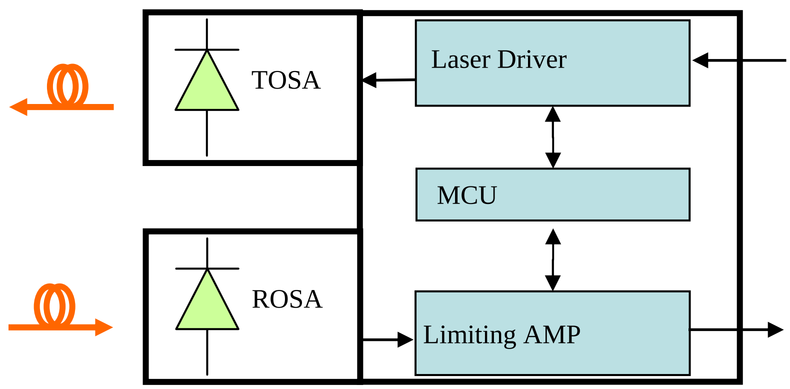
1 Introduction

The enhanced small form-factor pluggable (SFP+) is a compact, hot-pluggable transceiver used for 10G telecommunication and data communications applications. It is a popular industry format jointly developed and well supported by many system component vendors. The form factor and electrical interface are specified by a multisource agreement (MSA).

With complete portfolio for optical transceiver application of laser drivers, limiting amplifiers; combining with TI powerful MCU, TI is able to provide customers a total solution for SFP+ design. ONET1101, 11.3G laser driver, ONET8501, limiting amplifier, MSP430, MCU are chosen for this 10G SFP+.

This application note covers 10km 10G DML base SFP+ design details and test solution: includes module side schematic, PCB layout, firmware, BOM, debugging tips; also evaluation board schematic, PCB layout, GUI, BOM, and test results.

2 SFP+ Block Diagram



SFP+ consists of a transmitter (laser driver ONET1101 + DML NEC NX8341), a receiver (ROSA + limiting amplifier ONET8501) and a control block (MCU MSP430FR5738).

3 Transmitter

The transmitter converts electrical signals to optical signals.

Laser driver ONET1101 amplifies the input signal as modulation and provides DC current to DML as bias.

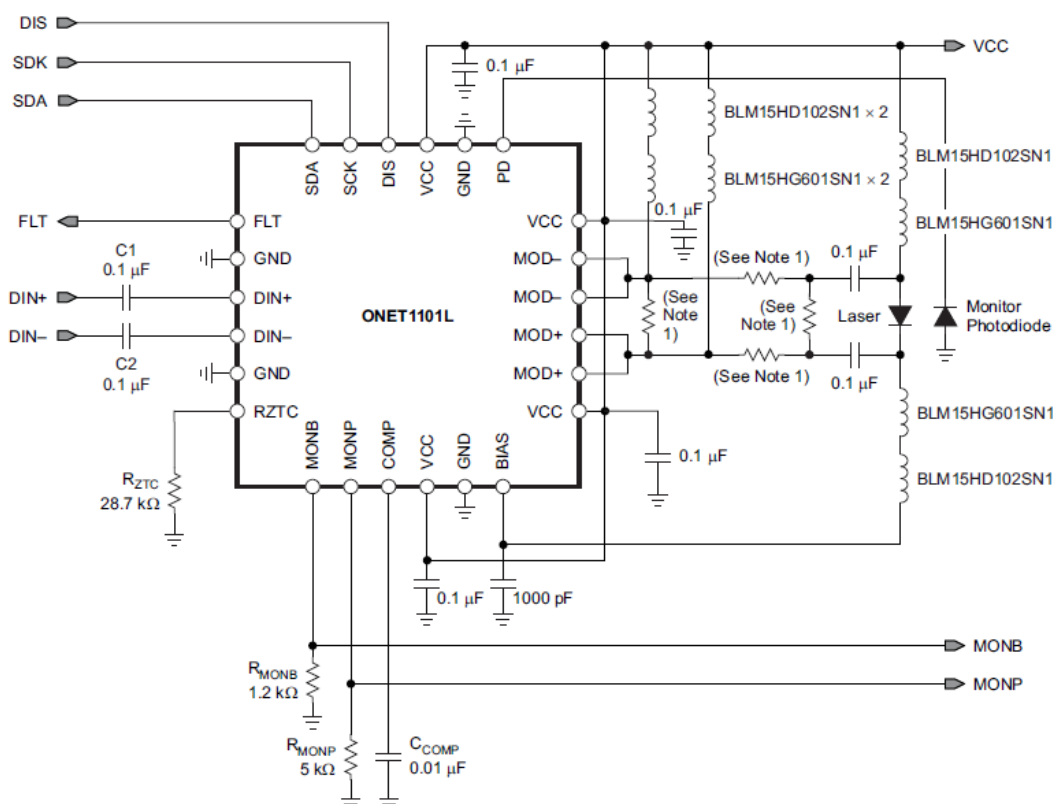
The ONET1101L is a high-speed, 3.3-V laser driver designed to directly modulate a laser at data rates from 2 to 11.3 Gbps.

3.1 Transmitter Schematic:

ONET1101L provides a 2-wire serial interface that helps digital control of the modulation, plus bias currents and cross-point, thus eliminating the need for external components. ONET1101L also includes an integrated automatic power control (APC) loop, plus circuitry to support laser safety and transceiver management systems.

With the digital control interface feature, ONET1101L enables designer focus on high-speed path and impedance matching for best eye performance.

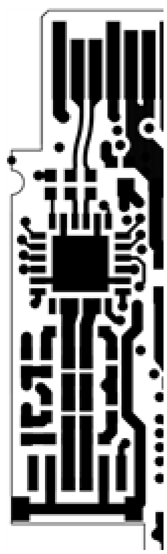
The following schematic shows the optimum impedance structure for typical DML.



3.2 PCB Layout

- A distributed feedback (DFB) laser is a low-resistance component, typically ranging from 7 Ω to 10 Ω.
- The flexible PCB cable is commonly a 25-Ω, single-ended trace.
- There is a reflection at the interconnection between the flex cable and the TOSA.
- A careful layout and impedance match circuit is critical for better performance.

This solution gives demonstrated-working layout, as shown below:



3.3 Calculations

The ONET1101L laser diode driver is optimized to drive 50-Ω differential output transmission impedance.

For a low-power design, it has a 500-Ω differential back termination. Because the LR DFB TOSA has only 10-Ω impedance (approximately), the reflection is much worse if there is no transfer circuit added. The purpose of the transfer circuit is to drive the load impedance close to 50 Ω from the driver side.

Output impedance: differential resistance seen by the MOD± outputs is:

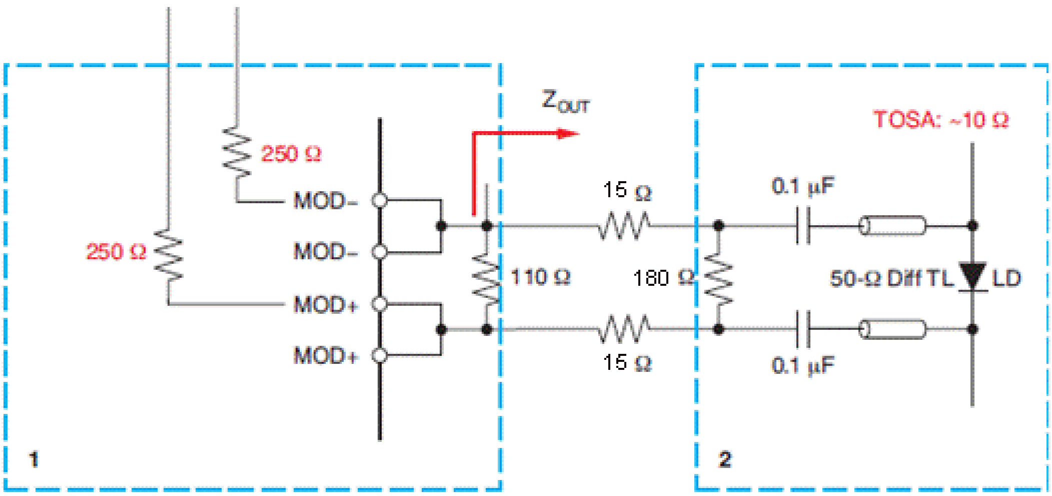
Z_{OUT} = R1//(R2 + R3 + R4 // R_{TOSA})

A typical R_{TOSA} is approximately 10 Ω, optimized R1~R4 are:

R1 = 110 Ω, R2 = R3 = 20 Ω, R4 = 180 Ω,

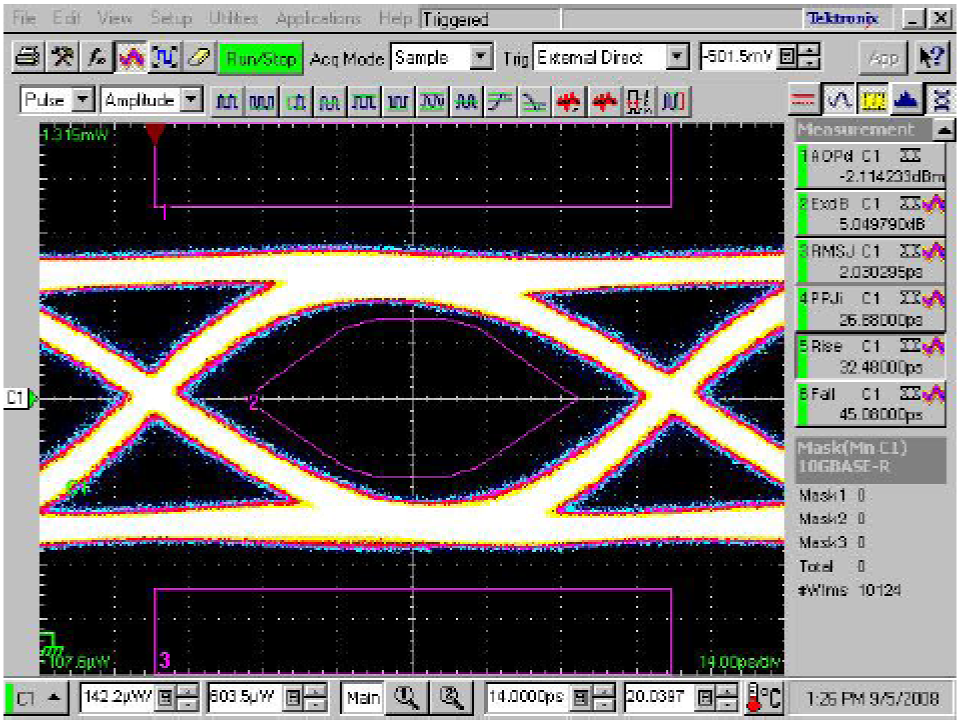
then Z_{OUT} is:

110//(40 + 180//10) = 35 Ω



3.4 Test Result

- TOSA: NEC NX8431
- VCC = 3.12 V;
- ICC = 150 mA;
- Room temperature;
- 10.3G PRBS31
- Mask margin 30%



4 Receiver

The receiver converts optical signals to electrical signals.

Limiting amplifier ONET8501PB amplifies the converted electrical signal as output of the receiver.

The ONET8501PB is a high-speed, 3.3-V limiting amplifier for multiple fiber-optic and copper cable applications with data rates from 2 to 11.3 Gbps.

4.1 Receiver Schematic

ONET8501PB provides a 2-wire serial interface ,which allows digital control of the bandwidth, output amplitude, output pre-emphasis, input threshold voltage (slice level), and the loss of signal assert level.

Predetermined settings for bandwidth and LOS assertion levels can also be selected with external rate selection pins.

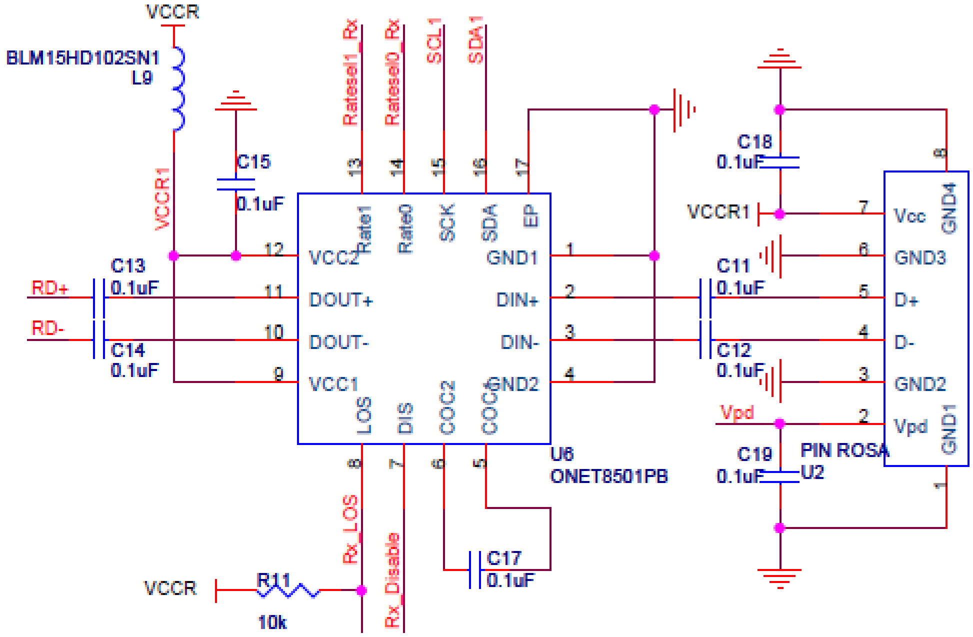
ONET8501PB also provides a gain of about 34 dB, which ensures a fully differential output swing for input signals as low as 20 $mV_{p\text{-}p}$.

The output amplitude can be adjusted to 350 mV_{pp}, 650 mV_{pp}, or 850 mV_{pp}.

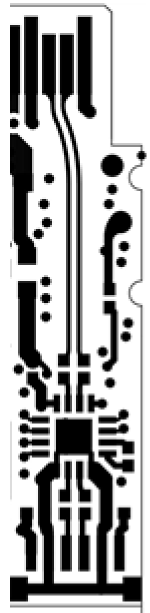
To compensate for frequency-dependent loss of microstrips or strip-lines connected to the output of the device, programmable pre-emphasis is included in the output stage.

A settable loss of signal detection and output disable are also provided.

With the digital control and high gain feature of the ONET8501PB, designers can achieve high-sensitivity performance.



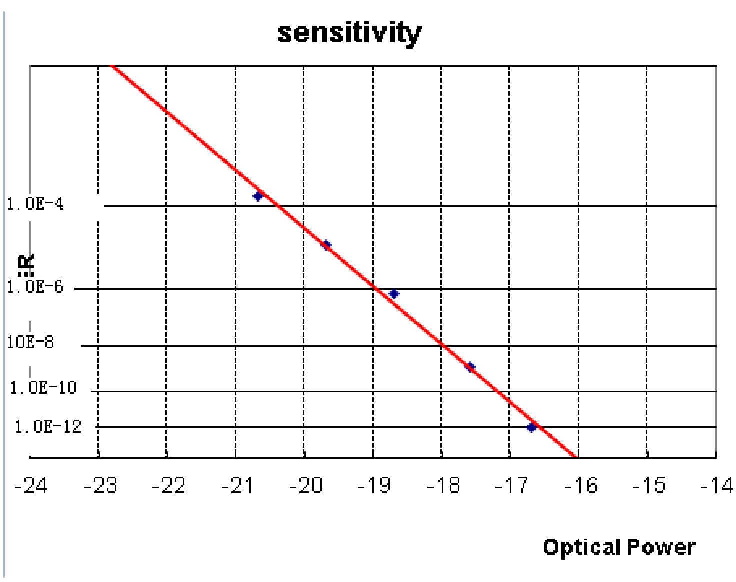
4.2 PCB Layout



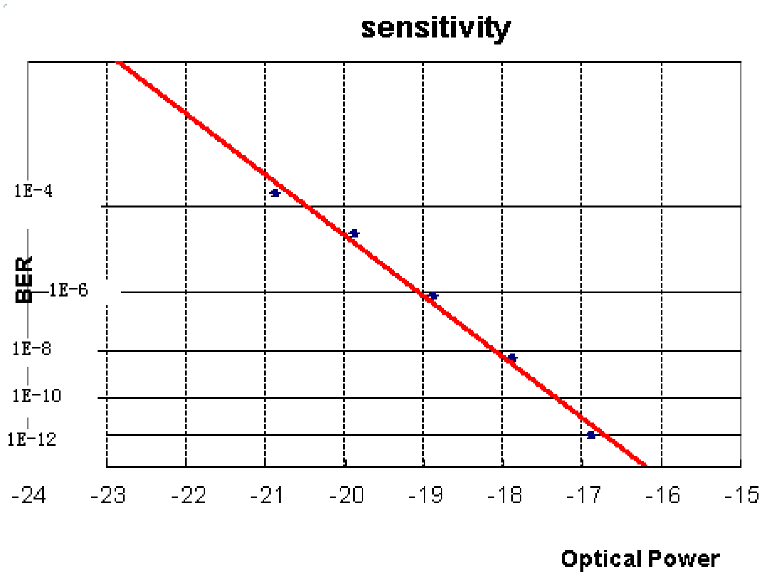
4.3 BER Curves

Test results of two modules:

	Optical Power	Ext.R		
No.1	-0.33dbm	5.0dB	-16.7	0
			-17.6	1.30E-09
			-18.7	6.50E-07
			-19.7	1.40E-05
			-20.7	1.60E-04
			Sensitivity	-16.6465



No.2	-0.27 5.15dB	-16.9	0
第 318 张		-17.9	5.80E-09
		-18.9	7.30E-07
		-19.9	2.80E-05
		-20.9	1.80E-04
		Sensitivity	-16.8258

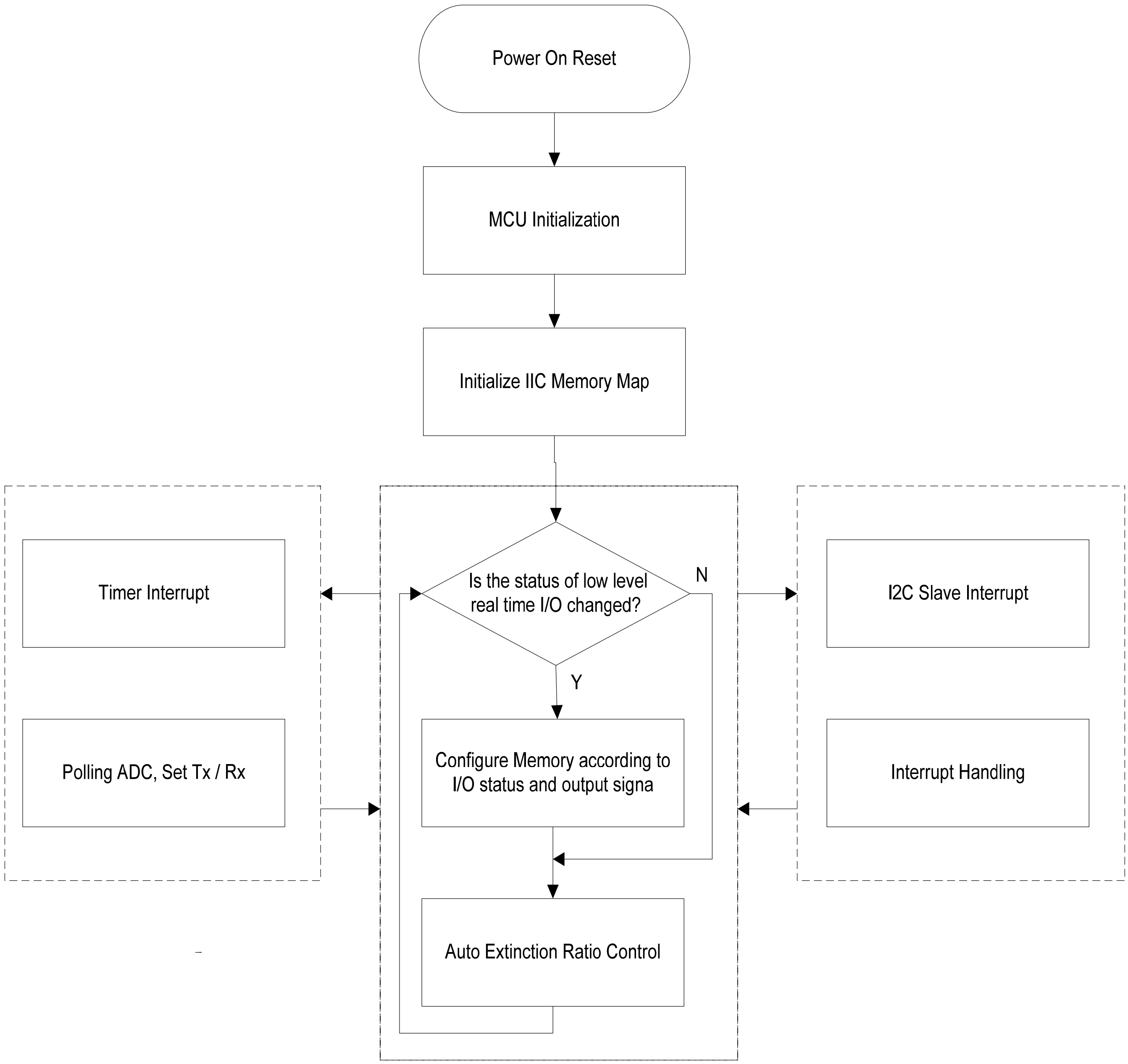


5 Firmware

The firmware running in the MSP430FR5738 finishes the following main tasks:

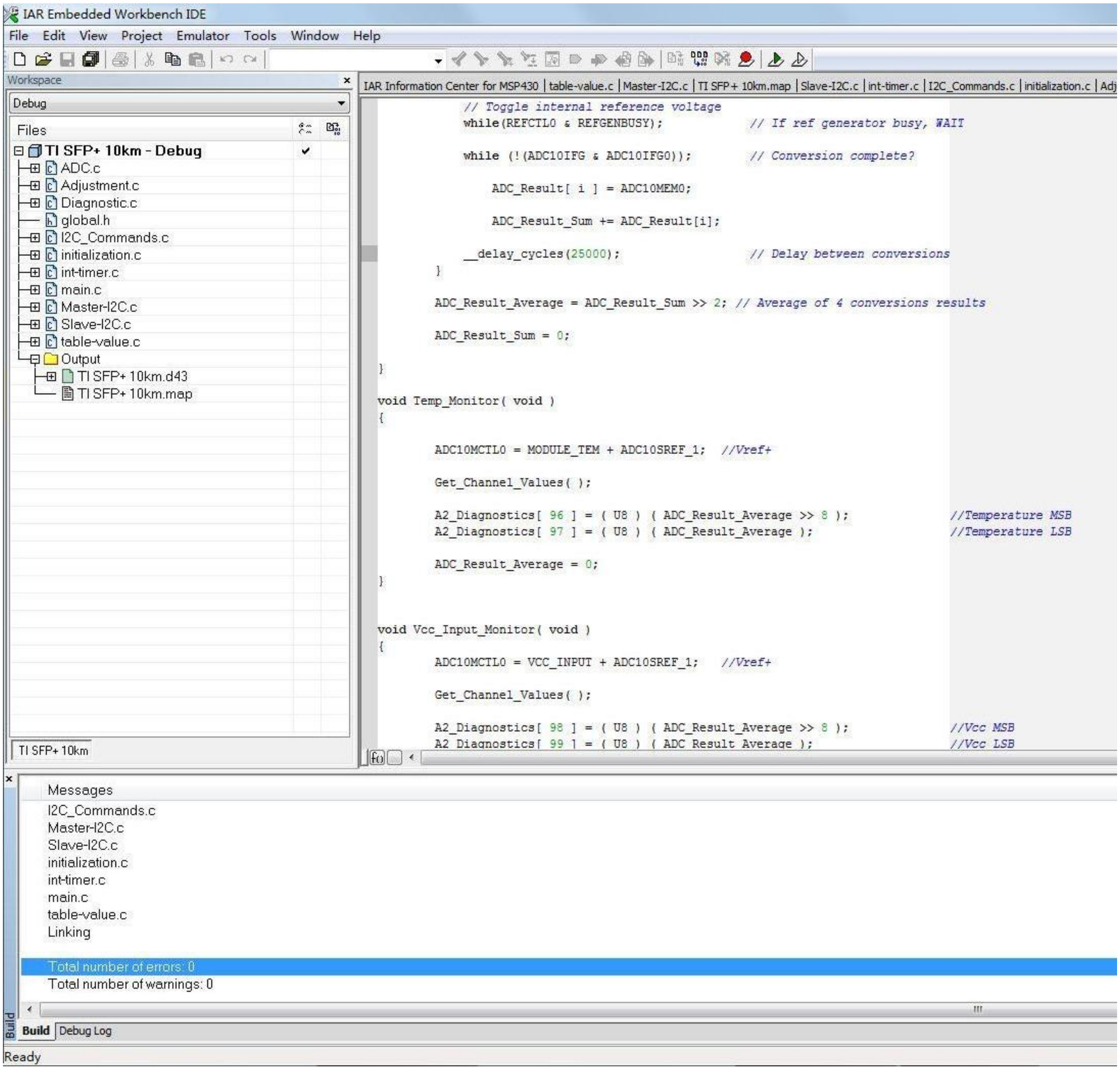
- Monitor ADCs: temperature, input voltage, TX bias, TX power, RX power
- Monitor the analog values to determine whether they exceed the settings; set the alarm and warning flags.
- Calculate the compensatory values and auto-run extinction ratio equalization.
- Act as IIC master to read out and control the laser driver and limit amplifier.
- Act as IIC slave, communicate with the upper control center via IIC bus, send out the monitoring values, the alarm and warning values, pins status, vendor information and other real time information of the SFP+ module, and receive command and execute.

5.1 Firmware Main Flowchart



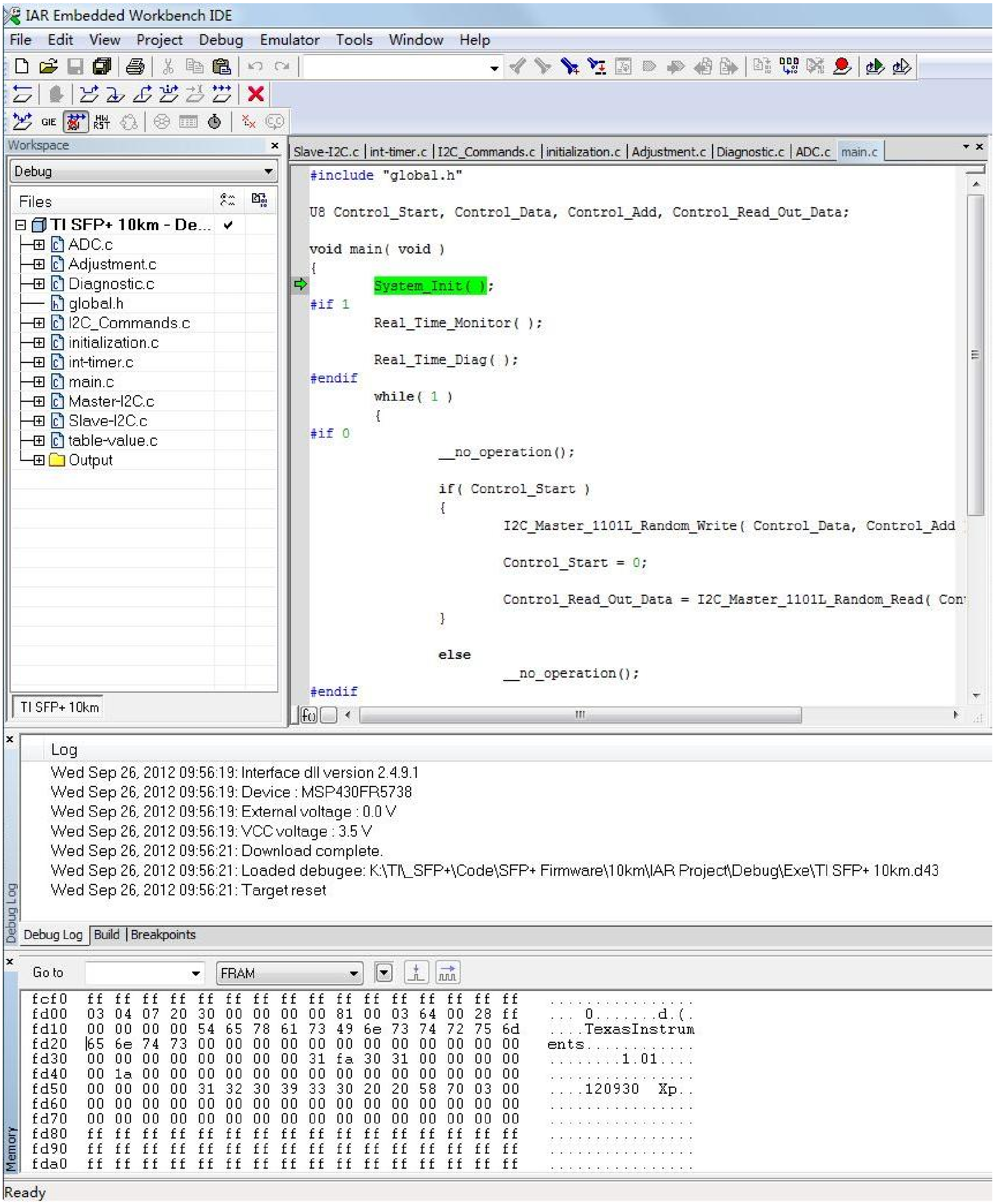
5.2 Compilation environment

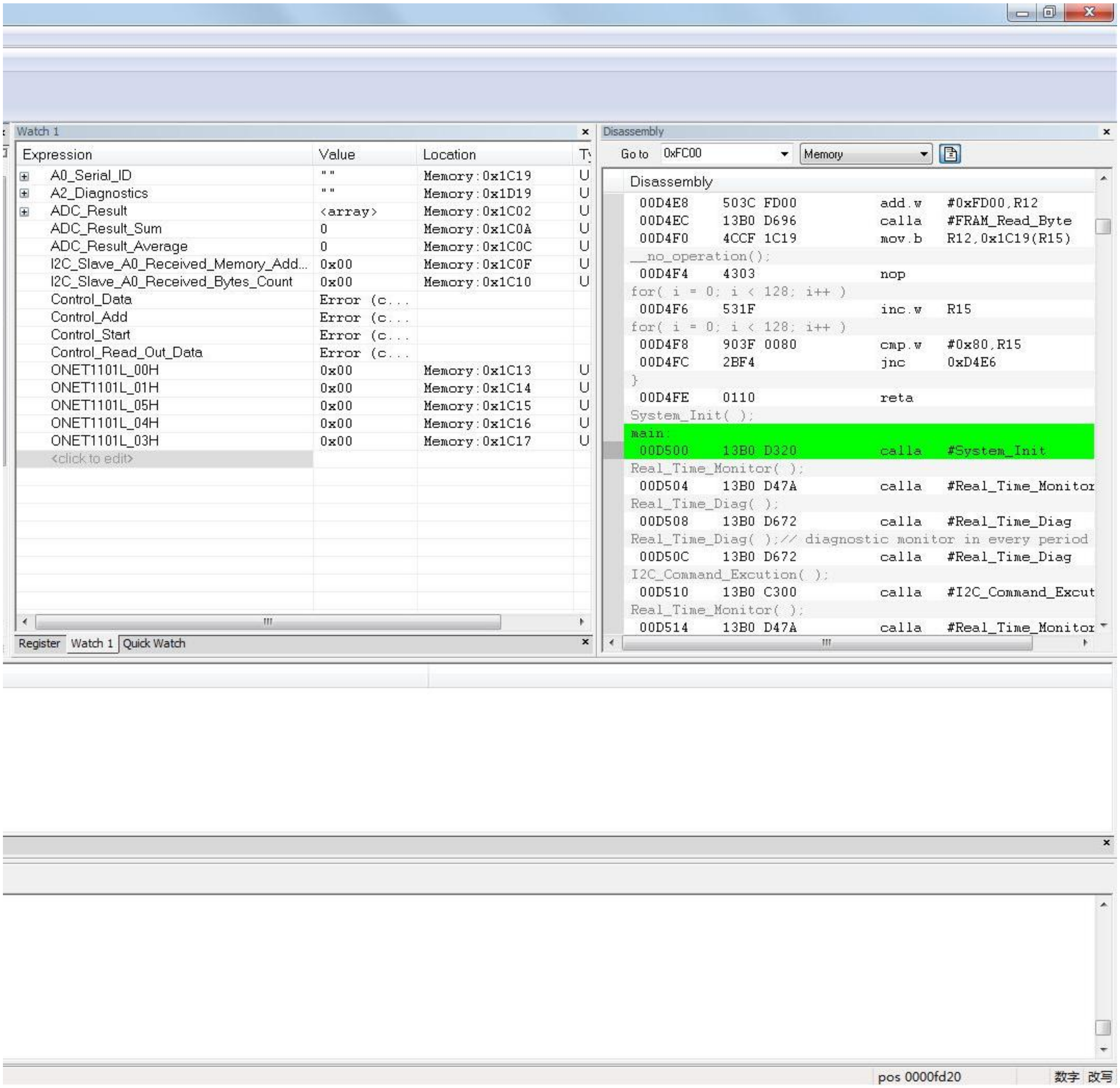
The firmware is compiled and debugged under the IAR IDE environment.

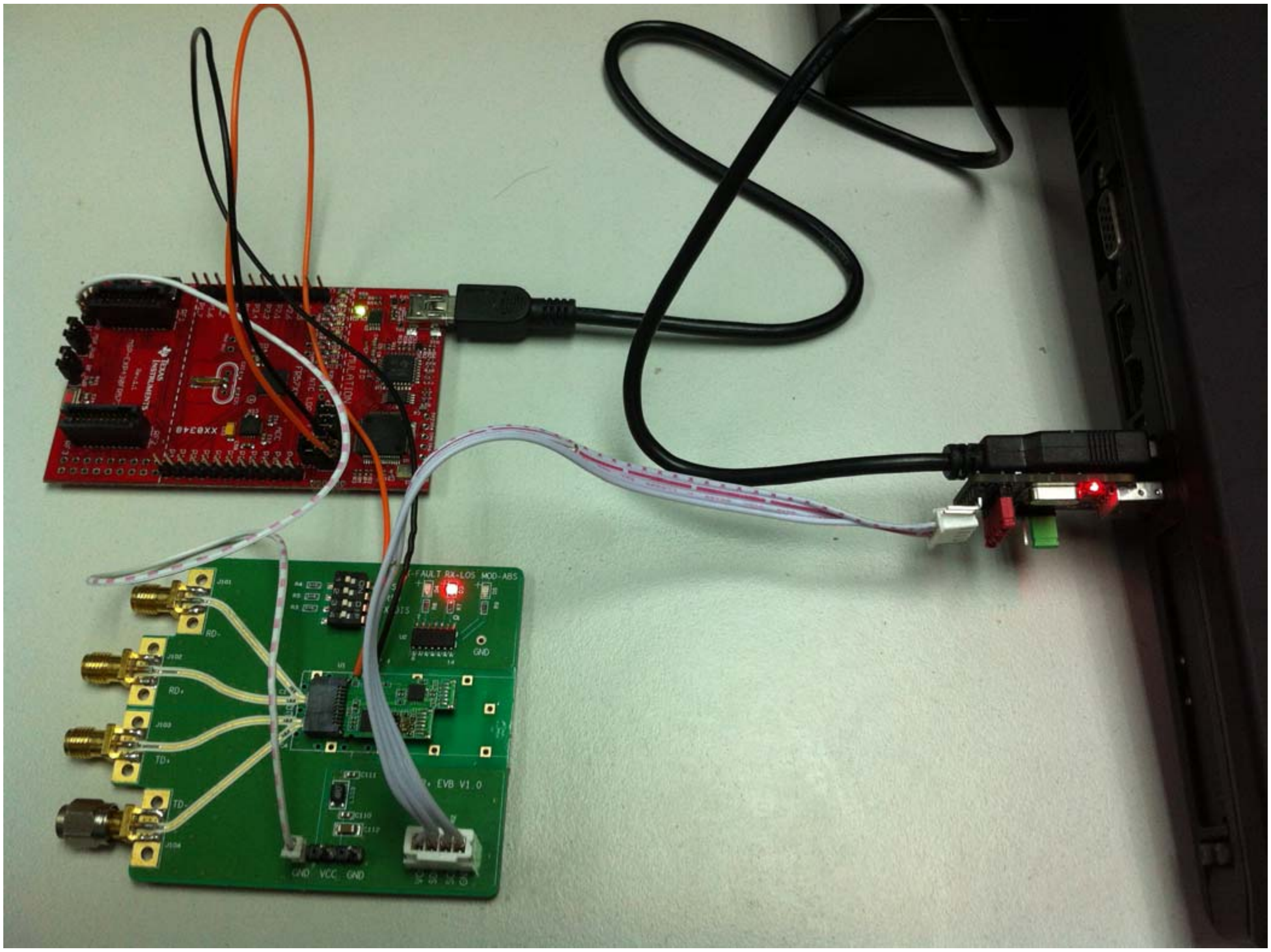


5.3 Simulate and Debug

Run the simulation and debug the firmware using the TI MSP430FR57xx simulator connected with the target board.



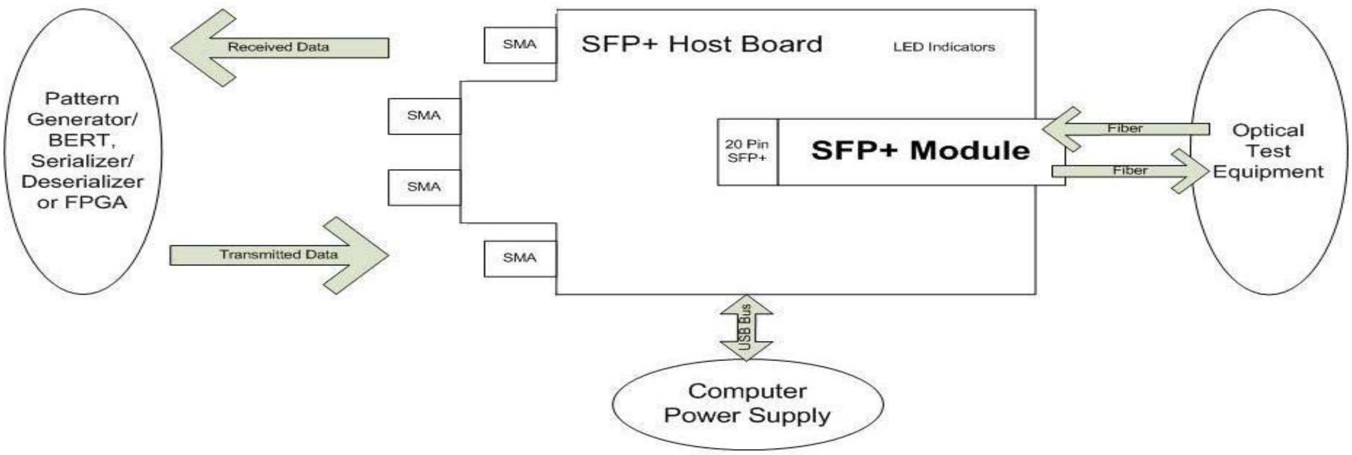

Watch 1
Expression
Value
Location
A0_Serial_ID
""
Memory:0x1C19
A2_Diagnostics
""
Memory:0x1D19
ADC_Result
<array>
Memory:0x1C02
ADC_Result_Sum
0
Memory:0x1C0A
ADC_Result_Average
0
Memory:0x1C0C
I2C_Slave_A0_Received_Memory_Add...
0x00
Memory:0x1C0F
I2C_Slave_A0_Received_Bytes_Count
0x00
Memory:0x1C10
Control_Data
Error (c...
Control_Add
Error (c...
Control_Start
Error (c...
Control_Read_Out_Data
Error (c...
ONET1101L_00H
0x00
Memory:0x1C13
ONET1101L_01H
0x00
Memory:0x1C14
ONET1101L_05H
0x00
Memory:0x1C15
ONET1101L_04H
0x00
Memory:0x1C16
ONET1101L_03H
0x00
Memory:0x1C17
<click to edit>
Register
Watch 1
Quick Watch
Disassembly
Go to
0xFC00
Memory
Disassembly
00D4E8 503C FD00 add.w #0xFD00,R12
00D4EC 13B0 D696 calla #FRAM_Read_Byte
00D4F0 4CCF 1C19 mov.b R12,0x1C19(R15)
__no_operation();
00D4F4 4303 nop
for(i = 0; i < 128; i++)
00D4F6 531F inc.w R15
for(i = 0; i < 128; i++)
00D4F8 903F 0080 cmp.w #0x80,R15
00D4FC 2BF4 jnc 0xD4E6
}
00D4FE 0110 reta
System_Init( );
main:
00D500 13B0 D320 calla #System_Init
Real_Time_Monitor( );
00D504 13B0 D47A calla #Real_Time_Monitor
Real_Time_Diag( );
00D508 13B0 D672 calla #Real_Time_Diag
Real_Time_Diag( );// diagnostic monitor in every period
00D50C 13B0 D672 calla #Real_Time_Diag
I2C_Command_Excution( );
00D510 13B0 C300 calla #I2C_Command_Excut
Real_Time_Monitor( );
00D514 13B0 D47A calla #Real_Time_Monitor
pos 0000fd20
数字 改写

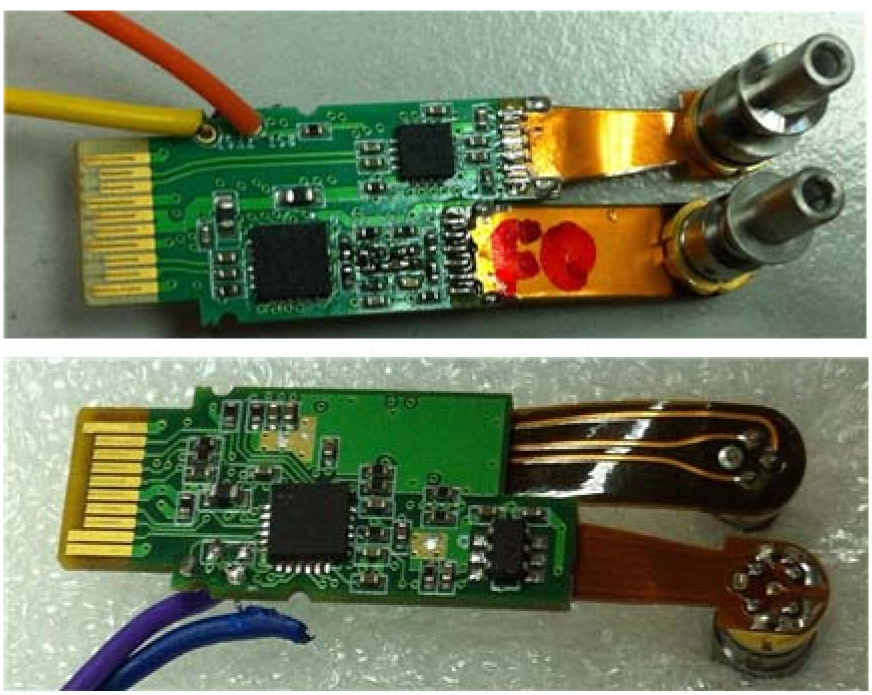


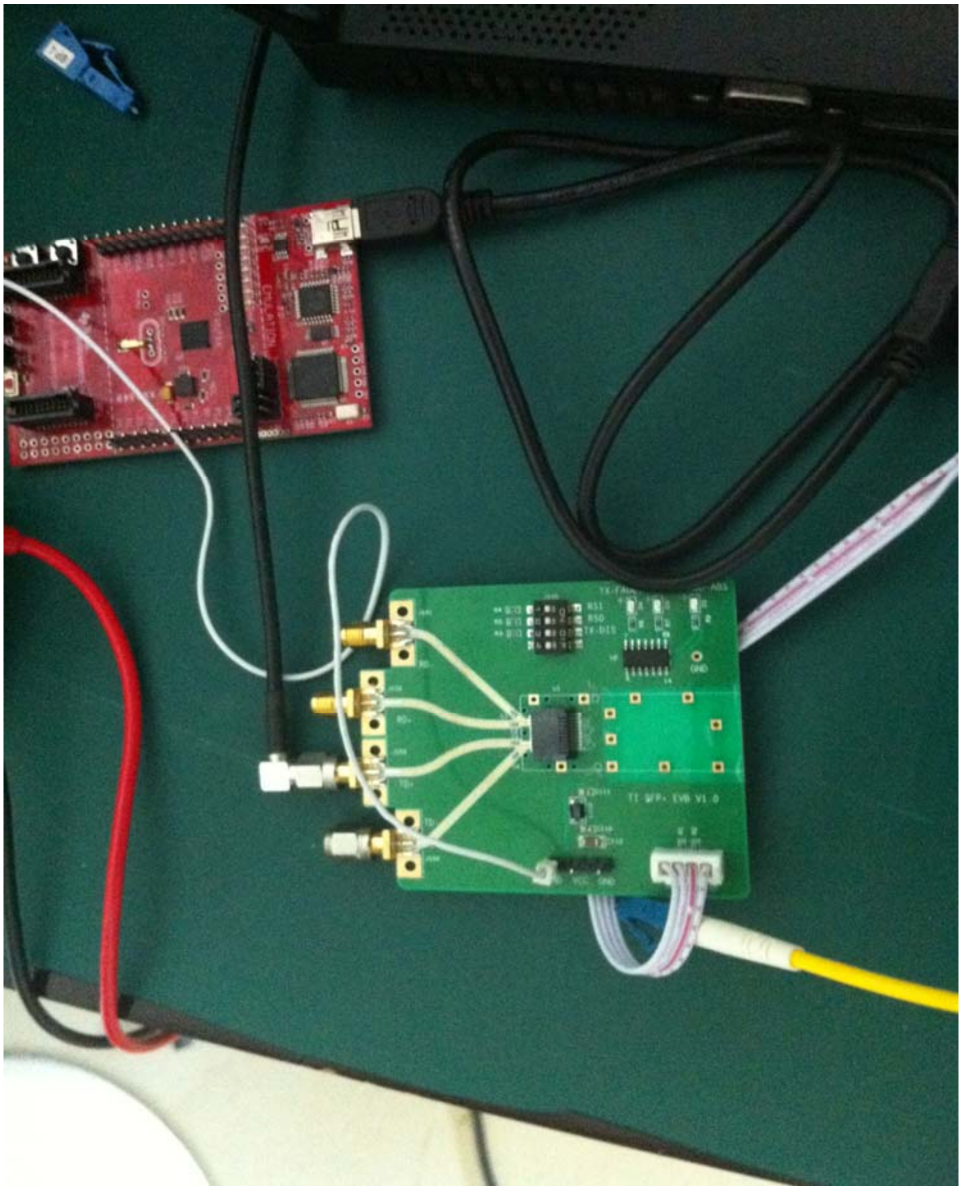
6 Test Configuration

To evaluate performance of an assembled board, this application note also describes a complete test configuration, includes setup, hardware (evaluation board), and software (GUI).

6.1 Test Setup



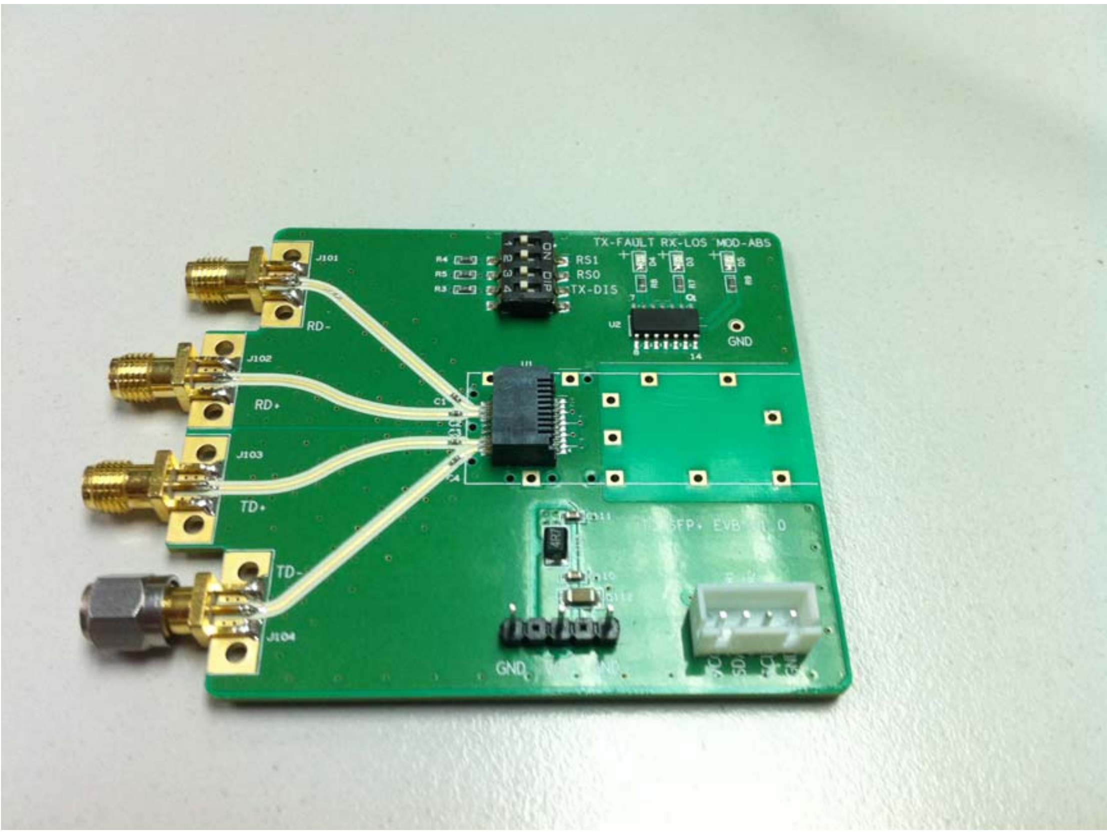




6.2 Evaluation Board

This high-speed, SFP+ host board is designed for evaluating SFP+ modules that operate at data rates up to 11.3 Gbps.

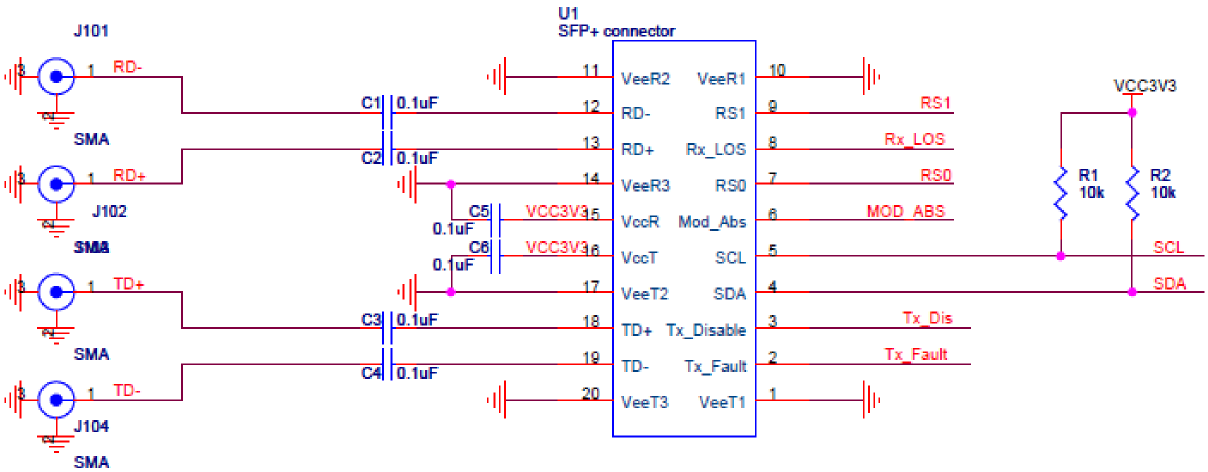
The host board can be used to test SFP+ and demo additional features for testing, monitoring, and programming TI SFP+ total solution.

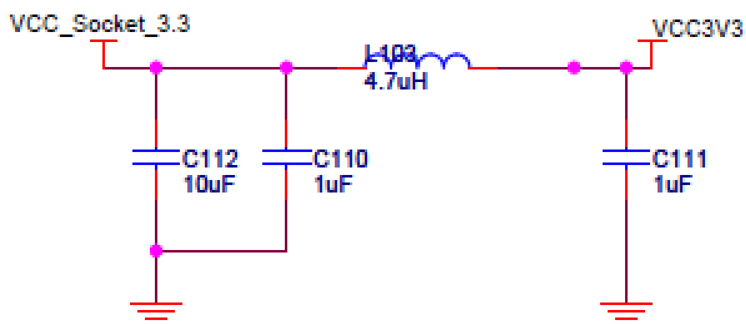


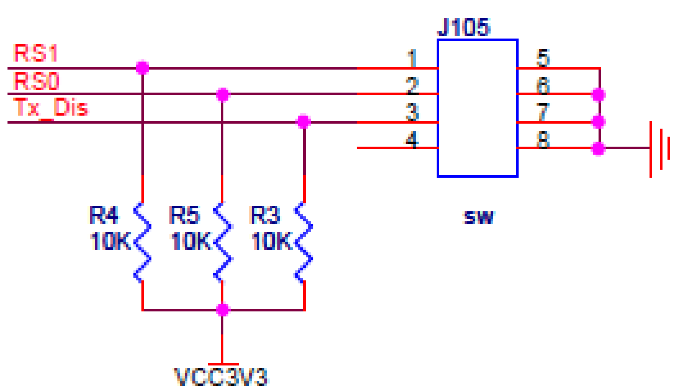
The evaluation board provides microstrip transmission lines and SMA connectors for transmitted and received data.

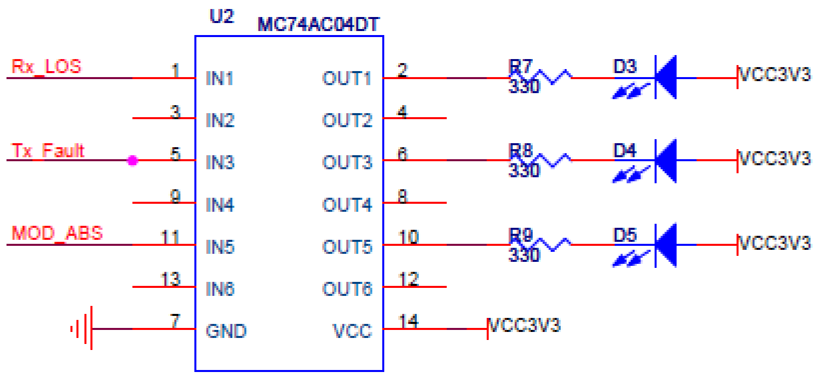
Supply current monitors, voltage monitors, and some digital I/O control/monitoring are provided through hardware (also the GUI).

6.3 Schematic









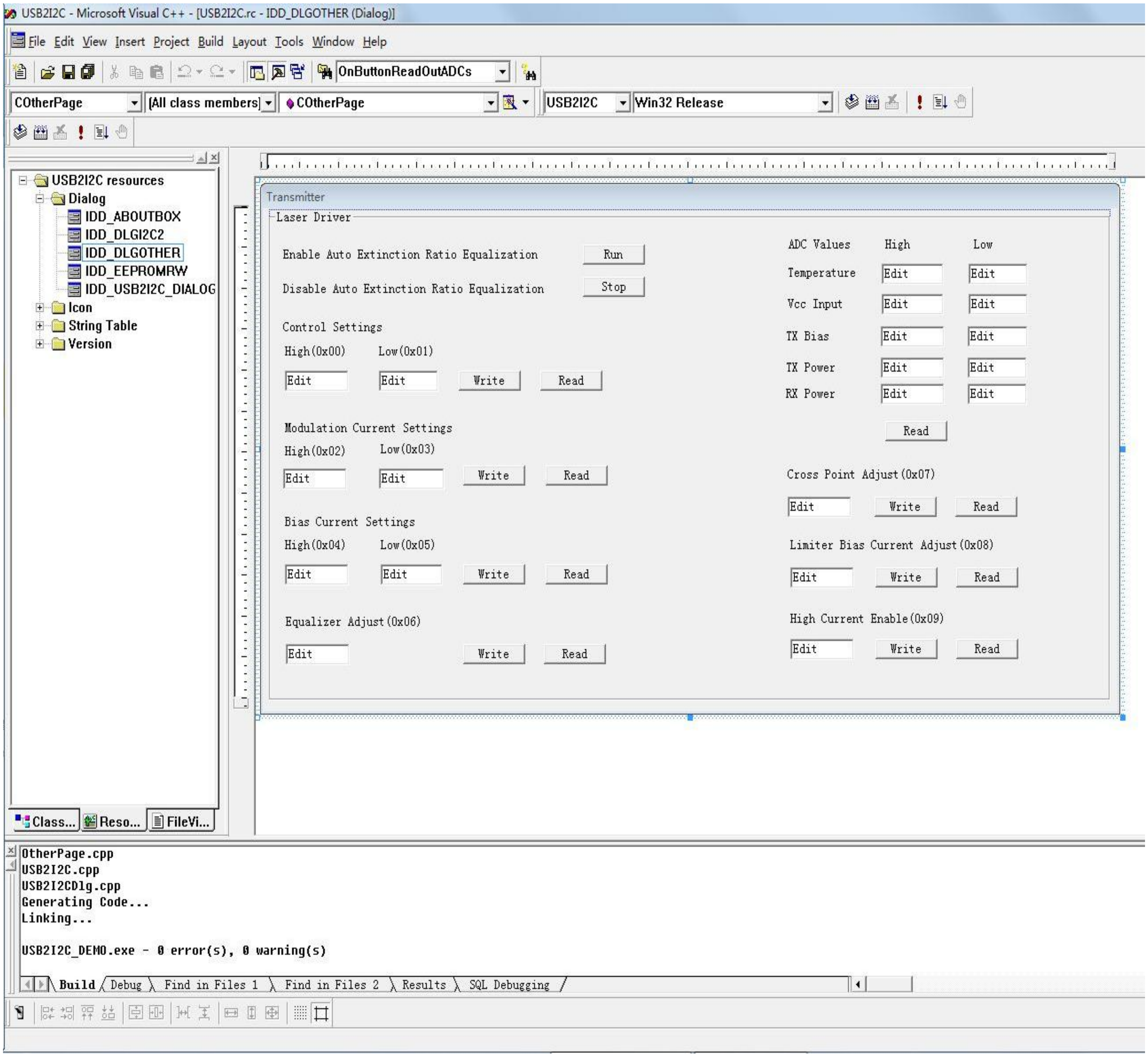
6.4 PCB Layout

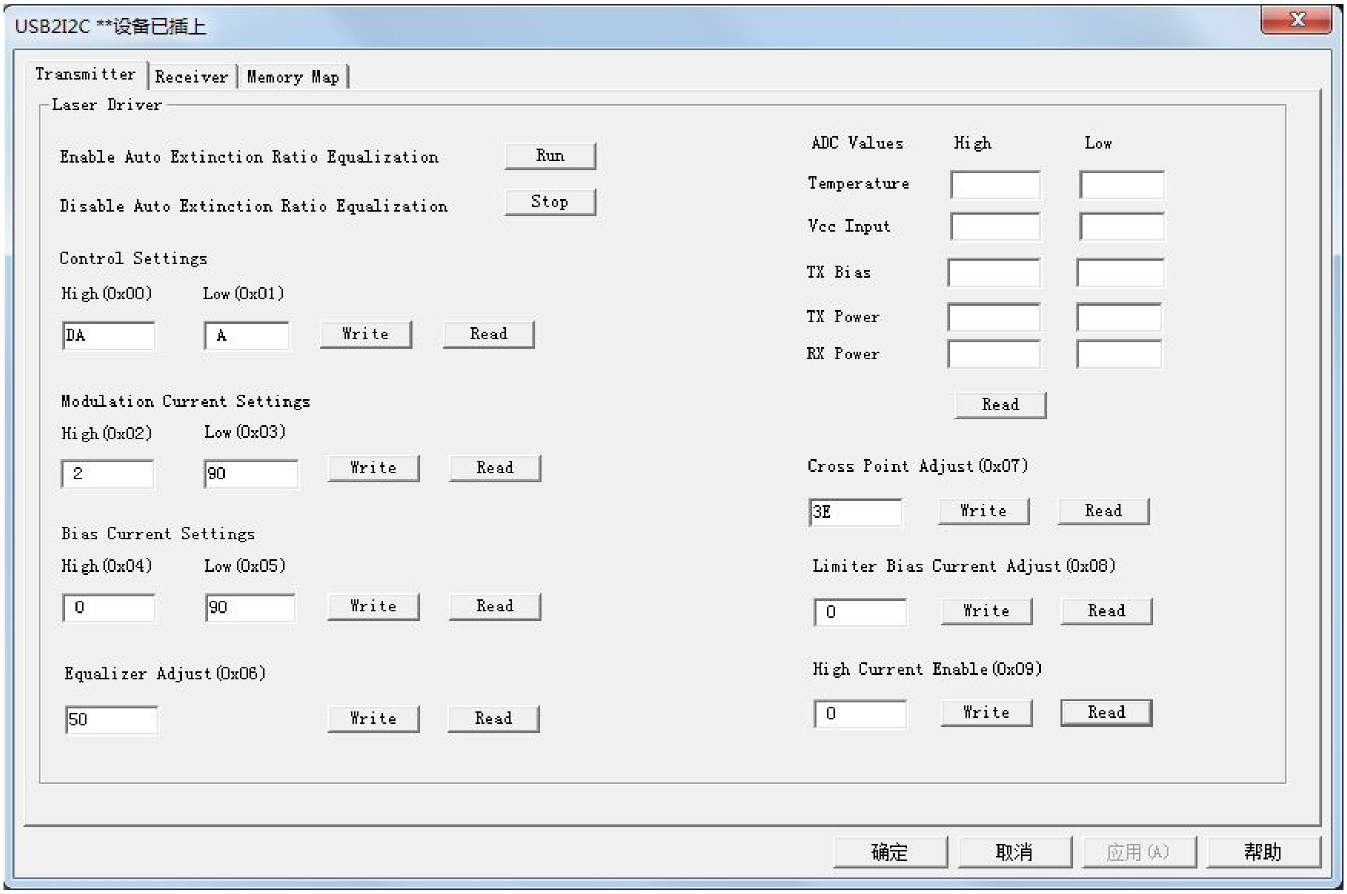
The evaluation board designed to use single-ended transmission lines.

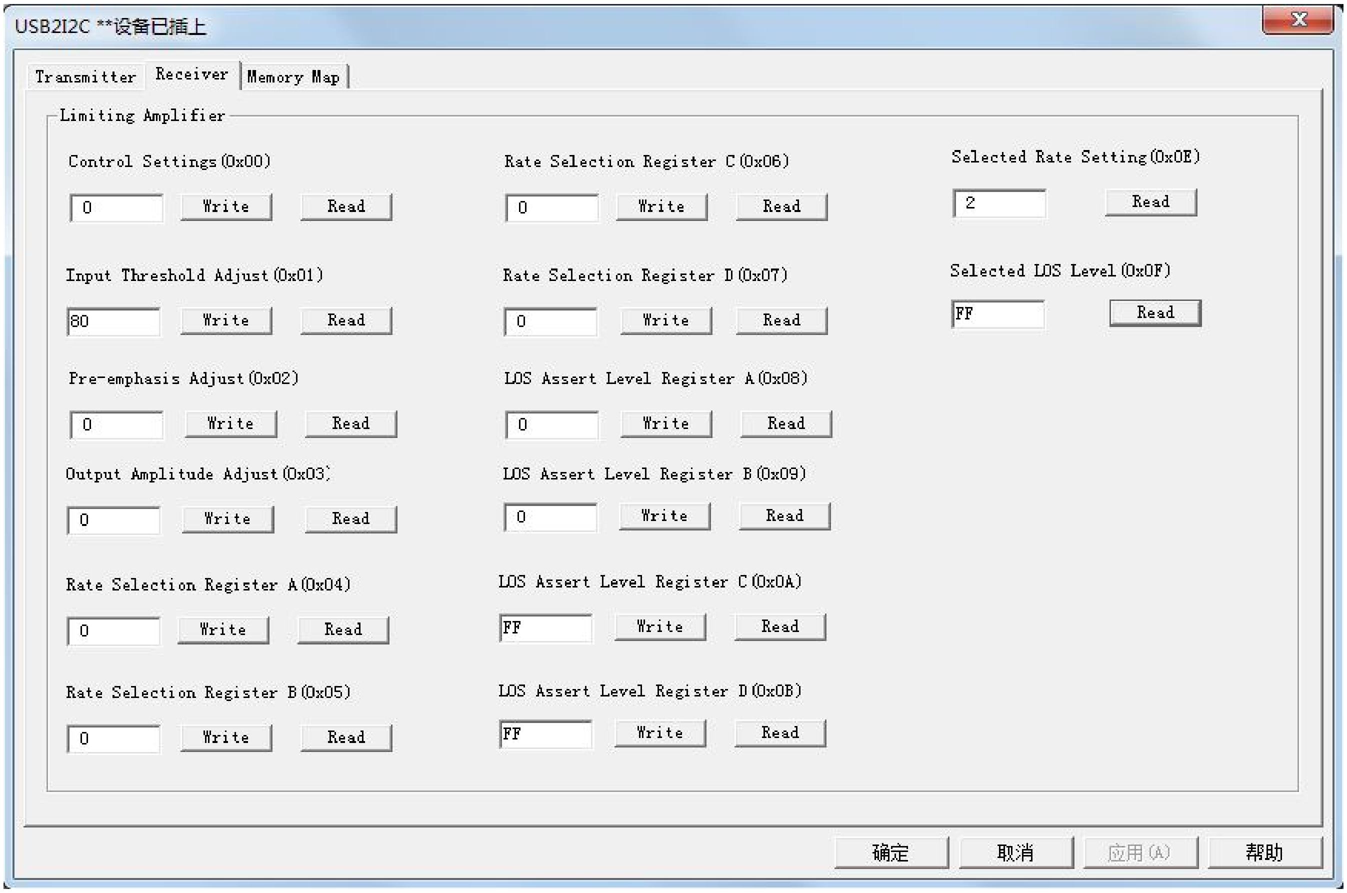
Changing the PCB layer profile can affect the impedance of these transmission lines and, therefore, the performance.

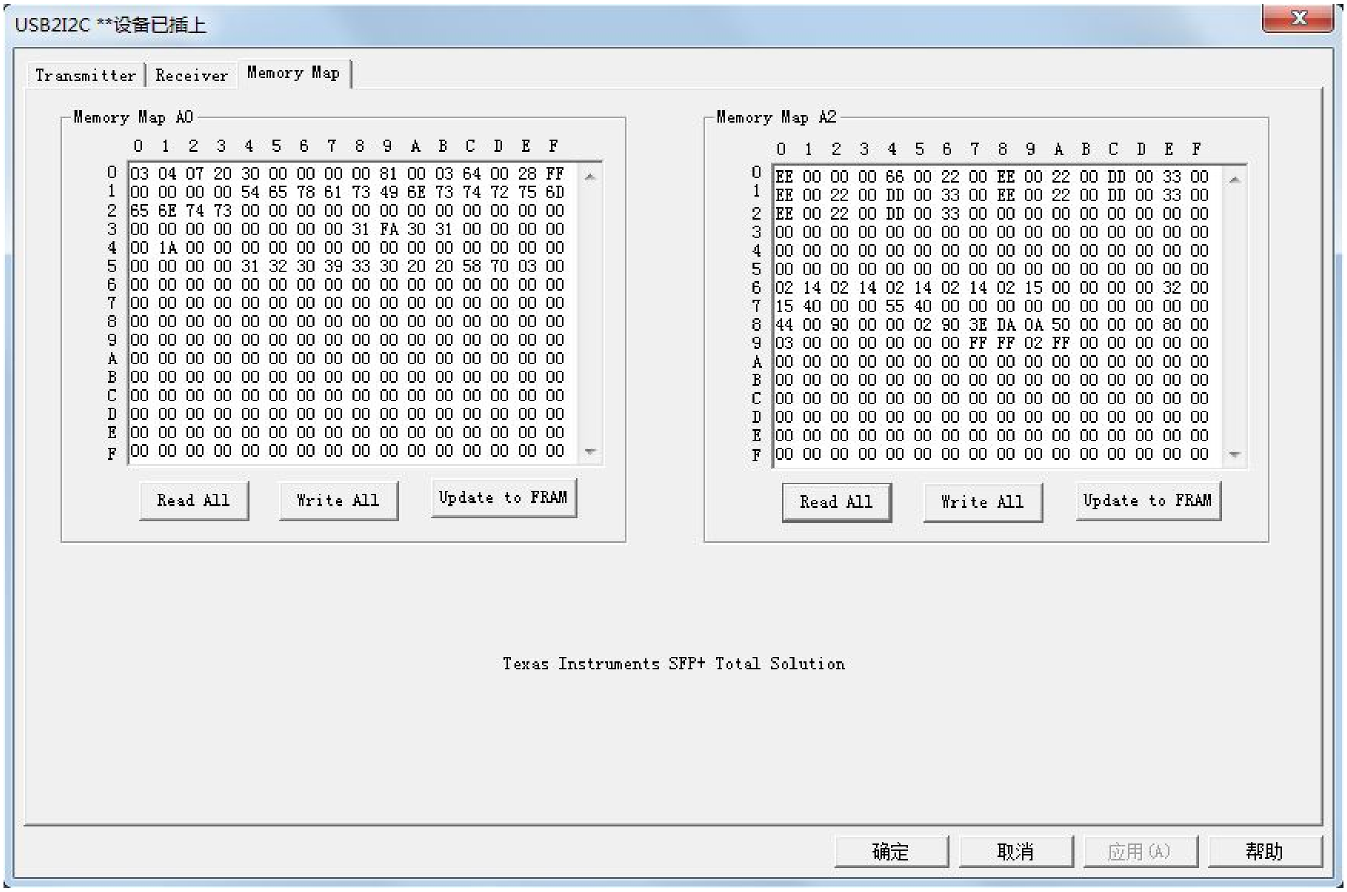
6.5 GUI

The GUI software is developed under VC++. It is compiled by VC++ 6.0.




USB2I2C **设备已插上
Transmitter
Receiver
Memory Map
Laser Driver
Enable Auto Extinction Ratio Equalization
Run
Disable Auto Extinction Ratio Equalization
Stop
Control Settings
High (0x00)
Low (0x01)
DA
A
Write
Read
Modulation Current Settings
High (0x02)
Low (0x03)
2
90
Bias Current Settings
High (0x04)
Low (0x05)
0
90
Equalizer Adjust (0x06)
50
ADC Values
High
Low
Temperature
Vcc Input
TX Bias
TX Power
RX Power
Cross Point Adjust (0x07)
3E
Limiter Bias Current Adjust (0x08)
0
High Current Enable (0x09)
0
确定
取消
应用 (A)
帮助


USB2I2C **设备已插上
Transmitter
Receiver
Memory Map
Limiting Amplifier
Control Settings(0x00)
0
Write
Read
Input Threshold Adjust(0x01)
80
Write
Read
Pre-emphasis Adjust(0x02)
0
Write
Read
Output Amplitude Adjust(0x03)
0
Write
Read
Rate Selection Register A(0x04)
0
Write
Read
Rate Selection Register B(0x05)
0
Write
Read
Rate Selection Register C(0x06)
0
Write
Read
Rate Selection Register D(0x07)
0
Write
Read
LOS Assert Level Register A(0x08)
0
Write
Read
LOS Assert Level Register B(0x09)
0
Write
Read
LOS Assert Level Register C(0x0A)
FF
Write
Read
LOS Assert Level Register D(0x0B)
FF
Write
Read
Selected Rate Setting(0x0E)
2
Read
Selected LOS Level(0x0F)
FF
Read
确定
取消
应用(A)
帮助



7 References

1. *TI SLLA311 Considerations for PCB Layout and Impedance Matching Design in Optical Modules*, Daniel Long
2. *TI ONET1101 with Various TOSAs*, Alex Davidson

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