

## **TI Optical Module 10G SFP+ Total Solution**

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### **ABSTRACT**

TI 10G optical module SFP+ total solution is a complete demonstrated-working optical transceiver solution targeted for the small form factor pluggable (SFP+).

This solution reduces customer design time, thus saving customer cost without compromising performance. This is achieved by combining TI's laser driver ONET1101, limiting amplifier ONET8501 and powerful MCU MSP430 into an SFP+ multisource agreement standard package, with convincing design files and test results.

This application note provides the schematics, PC-board layout, Gerber files, bill of materials (BOM), firmware, and a graphical user interface (GUI); not only for the module but also for the evaluation board. Test setup, test data, and typical performance for assembled boards are also included in this solution.

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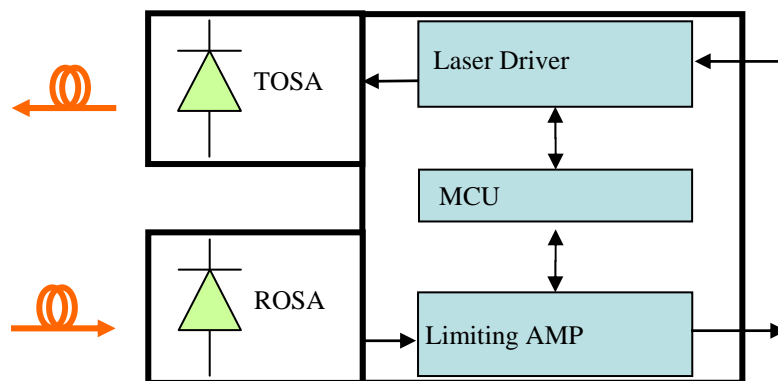
## 1 Introduction

The enhanced small form-factor pluggable (SFP+) is a compact, hot-pluggable transceiver used for 10G telecommunication and data communications applications. It is a popular industry format jointly developed and well supported by many system component vendors. The form factor and electrical interface are specified by a multisource agreement (MSA).

With complete portfolio for optical transceiver application of laser drivers, limiting amplifiers; combining with TI powerful MCU, TI is able to provide customers a total solution for SFP+ design. ONET1101, 11.3G laser driver, ONET8501, limiting amplifier, MSP430, MCU are chosen for this 10G SFP+.

This application note covers 10km 10G DML base SFP+ design details and test solution: includes module side schematic, PCB layout, firmware, BOM, debugging tips; also evaluation board schematic, PCB layout, GUI, BOM, and test results.

## 2 SFP+ Block Diagram



SFP+ consists of a transmitter (laser driver ONET1101 + DML NEC NX8341), a receiver (ROSA + limiting amplifier ONET8501) and a control block (MCU MSP430FR5738).

### 3 Transmitter

The transmitter converts electrical signals to optical signals.

Laser driver ONET1101 amplifies the input signal as modulation and provides DC current to DML as bias.

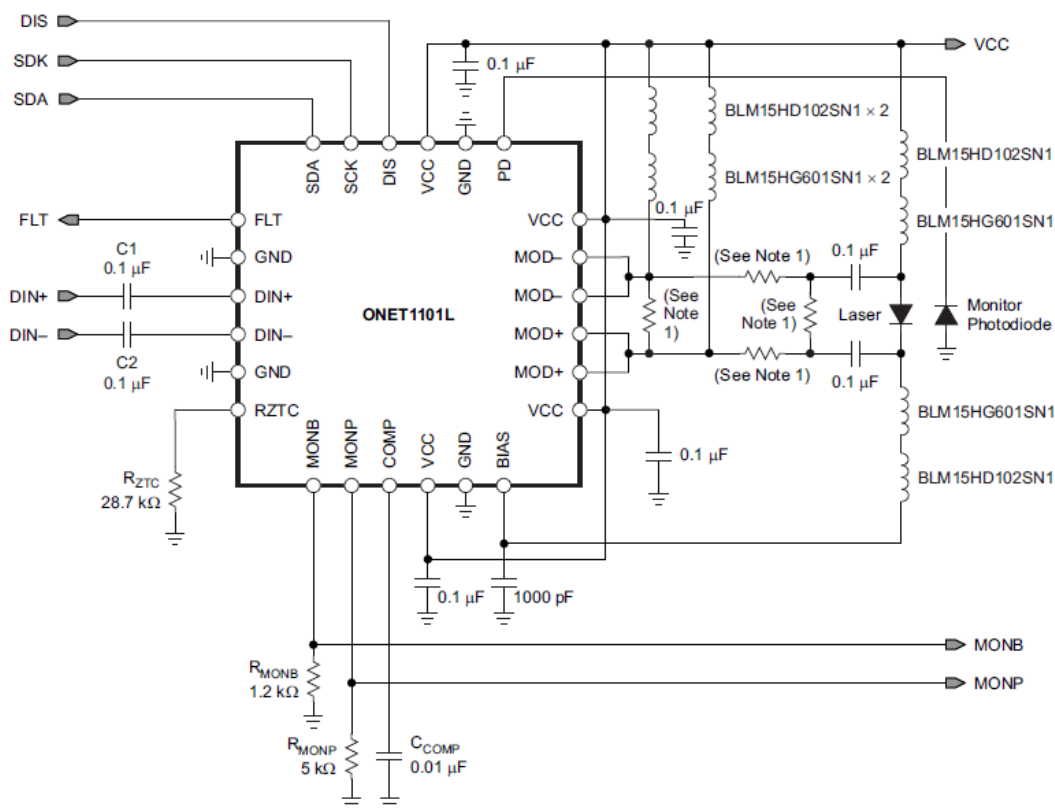
The ONET1101L is a high-speed, 3.3-V laser driver designed to directly modulate a laser at data rates from 2 to 11.3 Gbps.

#### 3.1 Transmitter Schematic:

ONET1101L provides a 2-wire serial interface that helps digital control of the modulation, plus bias currents and cross-point, thus eliminating the need for external components. ONET1101L also includes an integrated automatic power control (APC) loop, plus circuitry to support laser safety and transceiver management systems.

With the digital control interface feature, ONET1101L enables designer focus on high-speed path and impedance matching for best eye performance.

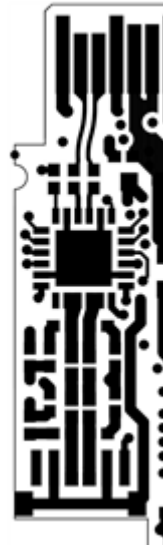
The following schematic shows the optimum impedance structure for typical DML.



### 3.2 PCB Layout

- A distributed feedback (DFB) laser is a low-resistance component, typically ranging from 7  $\Omega$  to 10  $\Omega$ .
- The flexible PCB cable is commonly a 25- $\Omega$ , single-ended trace.
- There is a reflection at the interconnection between the flex cable and the TOSA.
- A careful layout and impedance match circuit is critical for better performance.

This solution gives demonstrated-working layout, as shown below:



### 3.3 Calculations

The ONET1101L laser diode driver is optimized to drive 50- $\Omega$  differential output transmission impedance.

For a low-power design, it has a 500- $\Omega$  differential back termination. Because the LR DFB TOSA has only 10- $\Omega$  impedance (approximately), the reflection is much worse if there is no transfer circuit added. The purpose of the transfer circuit is to drive the load impedance close to 50  $\Omega$  from the driver side.

Output impedance: differential resistance seen by the MOD $\pm$  outputs is:

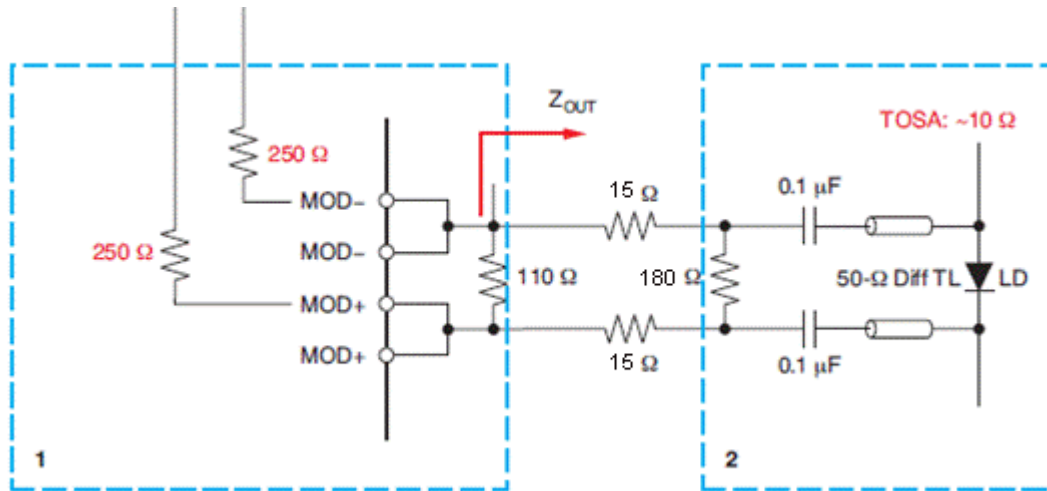
$$Z_{OUT} = R1 // (R2 + R3 + R4 // R_{TOSA})$$

A typical  $R_{TOSA}$  is approximately 10  $\Omega$ , optimized R1~R4 are:

$R1 = 110 \Omega$ ,  $R2 = R3 = 20 \Omega$ ,  $R4 = 180 \Omega$ ,

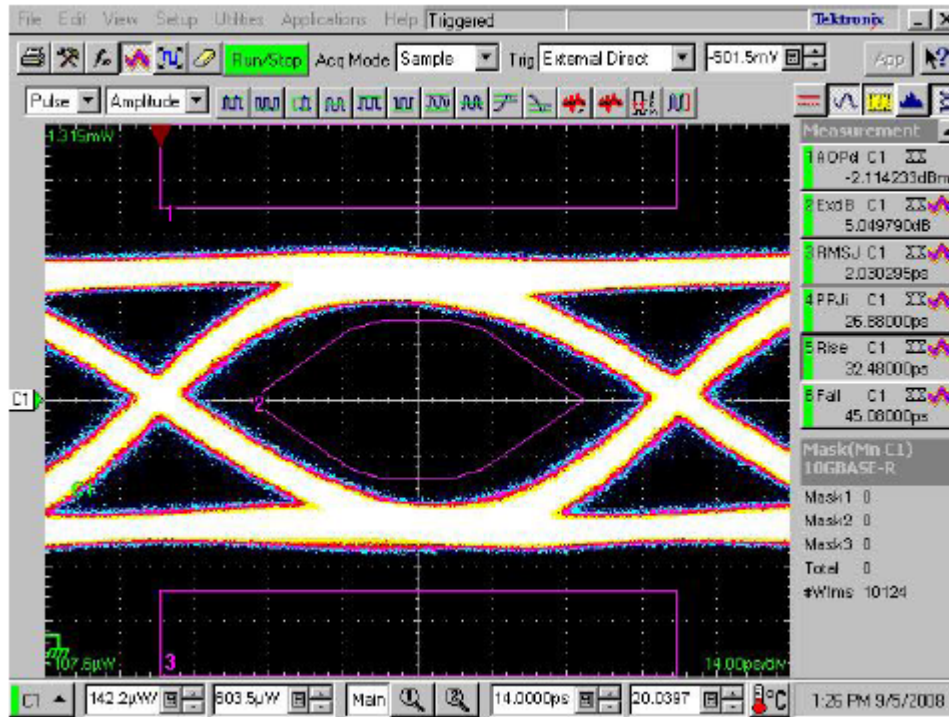
then  $Z_{OUT}$  is:

$$110 // (40 + 180 // 10) = 35 \Omega$$



### 3.4 Test Result

- TOSA: NEC NX8431
- VCC = 3.12 V;
- ICC = 150 mA;
- Room temperature;
- 10.3G PRBS31
- Mask margin 30%



## 4 Receiver

The receiver converts optical signals to electrical signals.

Limiting amplifier ONET8501PB amplifies the converted electrical signal as output of the receiver.

The ONET8501PB is a high-speed, 3.3-V limiting amplifier for multiple fiber-optic and copper cable applications with data rates from 2 to 11.3 Gbps.

### 4.1 Receiver Schematic

ONET8501PB provides a 2-wire serial interface, which allows digital control of the bandwidth, output amplitude, output pre-emphasis, input threshold voltage (slice level), and the loss of signal assert level.

Predetermined settings for bandwidth and LOS assertion levels can also be selected with external rate selection pins.

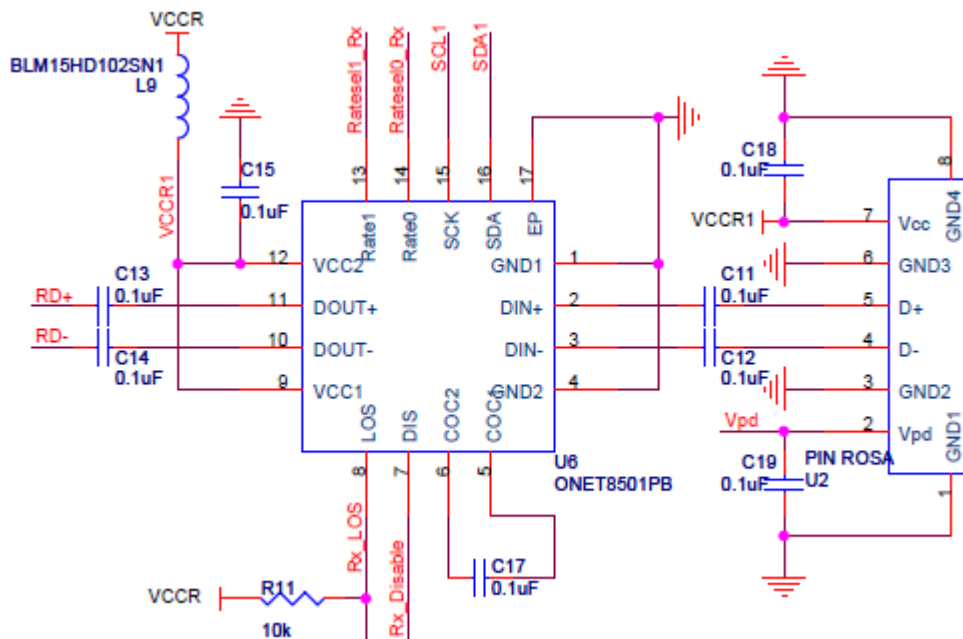
ONET8501PB also provides a gain of about 34 dB, which ensures a fully differential output swing for input signals as low as 20 mV<sub>p-p</sub>.

The output amplitude can be adjusted to 350 mV<sub>pp</sub>, 650 mV<sub>pp</sub>, or 850 mV<sub>pp</sub>.

To compensate for frequency-dependent loss of microstrips or strip-lines connected to the output of the device, programmable pre-emphasis is included in the output stage.

A settable loss of signal detection and output disable are also provided.

With the digital control and high gain feature of the ONET8501PB, designers can achieve high-sensitivity performance.



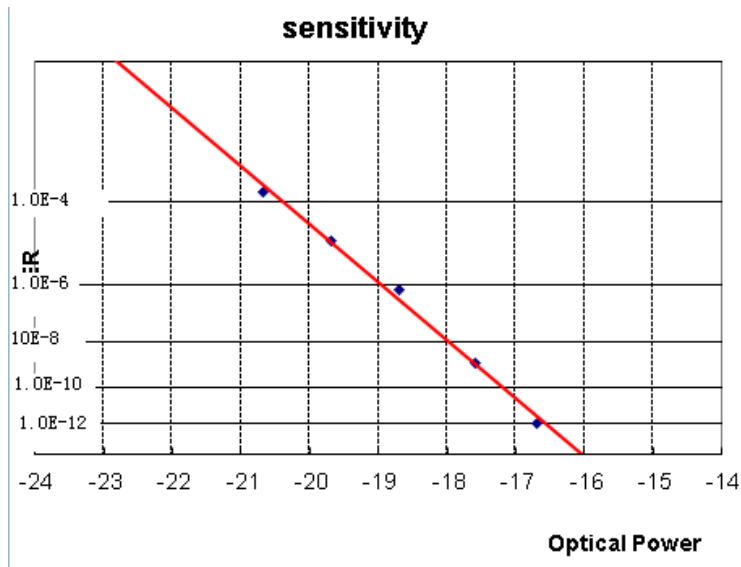
## 4.2 PCB Layout



## 4.3 BER Curves

Test results of two modules:

No.1	Optical Power	Ext.R		
	-0.33dbm	5.0dB	-16.7	0
			-17.6	1.30E-09
			-18.7	6.50E-07
			-19.7	1.40E-05
			-20.7	1.60E-04



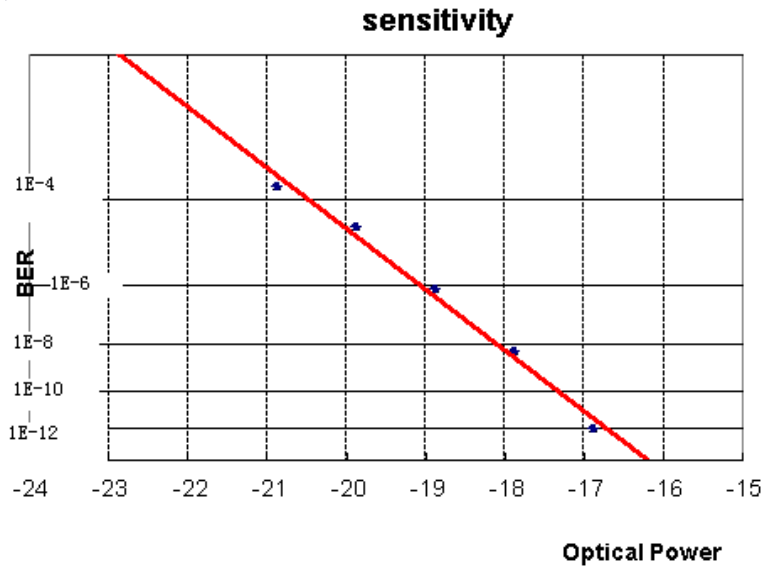
Sensitivity -16.6465



No.2 -0.27 5.15dB

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-16.9	0
-17.9	5.80E-09
-18.9	7.30E-07
-19.9	2.80E-05
-20.9	1.80E-04



Sensitivity -16.8258

## 5 Firmware

The firmware running in the MSP430FR5738 finishes the following main tasks:

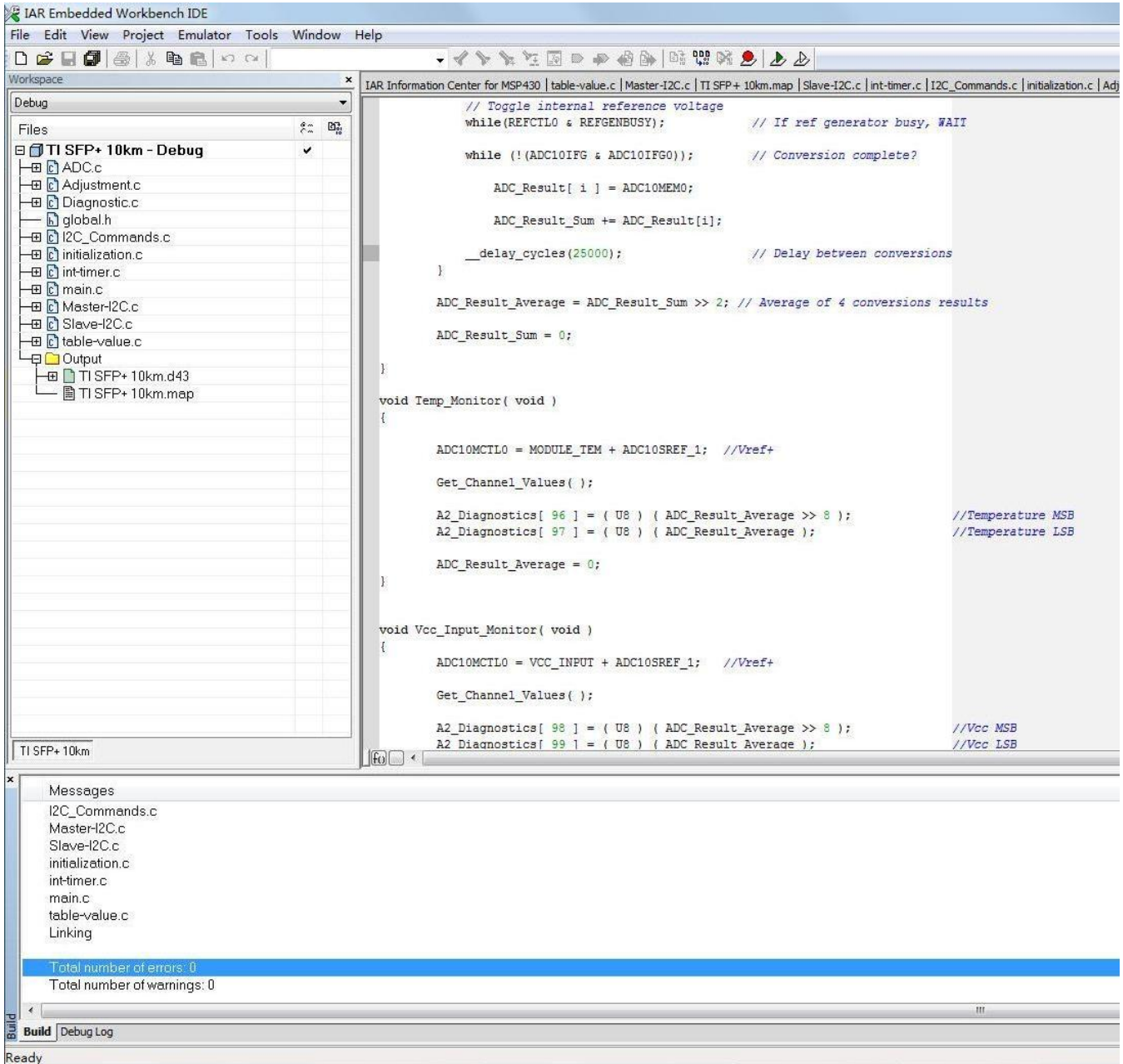
- Monitor ADCs: temperature, input voltage, TX bias, TX power, RX power
- Monitor the analog values to determine whether they exceed the settings; set the alarm and warning flags.
- Calculate the compensatory values and auto-run extinction ratio equalization.
- Act as IIC master to read out and control the laser driver and limit amplifier.
- Act as IIC slave, communicate with the upper control center via IIC bus, send out the monitoring values, the alarm and warning values, pins status, vendor information and other real time information of the SFP+ module, and receive command and execute.

### 5.1 Firmware Main Flowchart



## 5.2 Compilation environment

The firmware is compiled and debugged under the IAR IDE environment.



### 5.3 Simulate and Debug

Run the simulation and debug the firmware using the TI MSP430FR57xx simulator connected with the target board.

The screenshot displays the IAR Embedded Workbench IDE interface. The main window shows the source code for `main.c` with the following content:

```
#include "global.h"

U8 Control_Start, Control_Data, Control_Add, Control_Read_Out_Data;

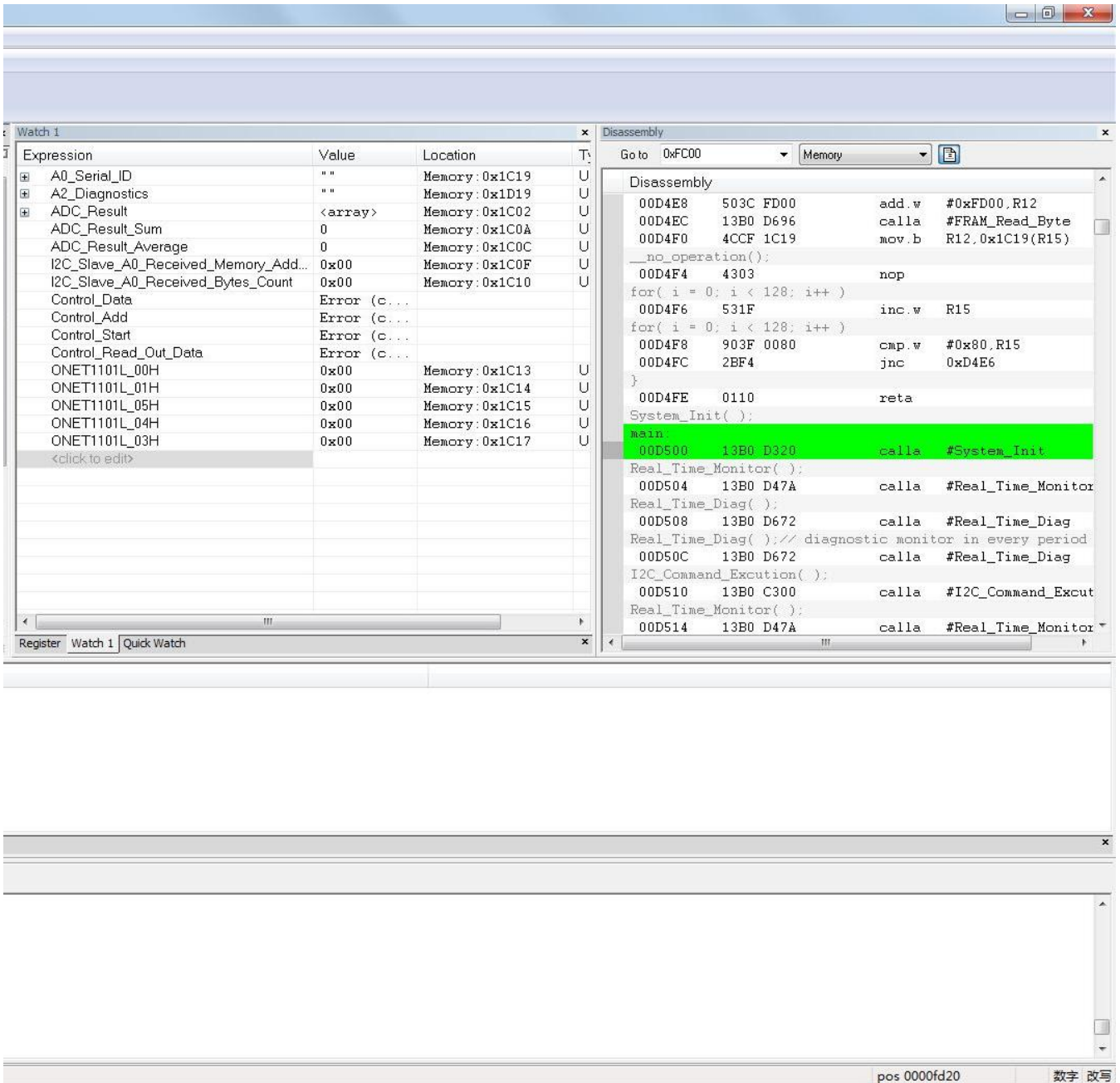
void main( void )
{
    System_Init();
    #if 1
        Real_Time_Monitor( );
        Real_Time_Diag( );
    #endif
    while( 1 )
    {
        #if 0
            __no_operation();
        #endif
        if( Control_Start )
        {
            I2C_Master_1101L_Random_Write( Control_Data, Control_Add
            Control_Start = 0;
            Control_Read_Out_Data = I2C_Master_1101L_Random_Read( Con
        }
        else
            __no_operation();
    }
}
#endif
```

The workspace on the left shows a project named "TI SFP+ 10km - De..." with files including `ADC.c`, `Adjustment.c`, `Diagnostic.c`, `global.h`, `I2C_Commands.c`, `initialization.c`, `int-timer.c`, `main.c`, `Master-I2C.c`, `Slave-I2C.c`, `table-value.c`, and `Output`.

The Debug Log window at the bottom shows the following messages:

```
Log
Wed Sep 26, 2012 09:56:19: Interface dll version 2.4.9.1
Wed Sep 26, 2012 09:56:19: Device : MSP430FR5738
Wed Sep 26, 2012 09:56:19: External voltage : 0.0 V
Wed Sep 26, 2012 09:56:19: VCC voltage : 3.5 V
Wed Sep 26, 2012 09:56:21: Download complete.
Wed Sep 26, 2012 09:56:21: Loaded debuggee: K:\TI\SFP+\Code\SFP+ Firmware\10km\IAR Project\Debug\Exe\TI SFP+ 10km.d43
Wed Sep 26, 2012 09:56:21: Target reset
```

The Memory window at the bottom shows a memory dump for the FRAM (Flash Read Only Memory) starting at address `fcf0`. The dump shows hexadecimal values and their corresponding ASCII characters, including "0", "TexasInstrum", "ents", "1.01", and "120930 Xp".



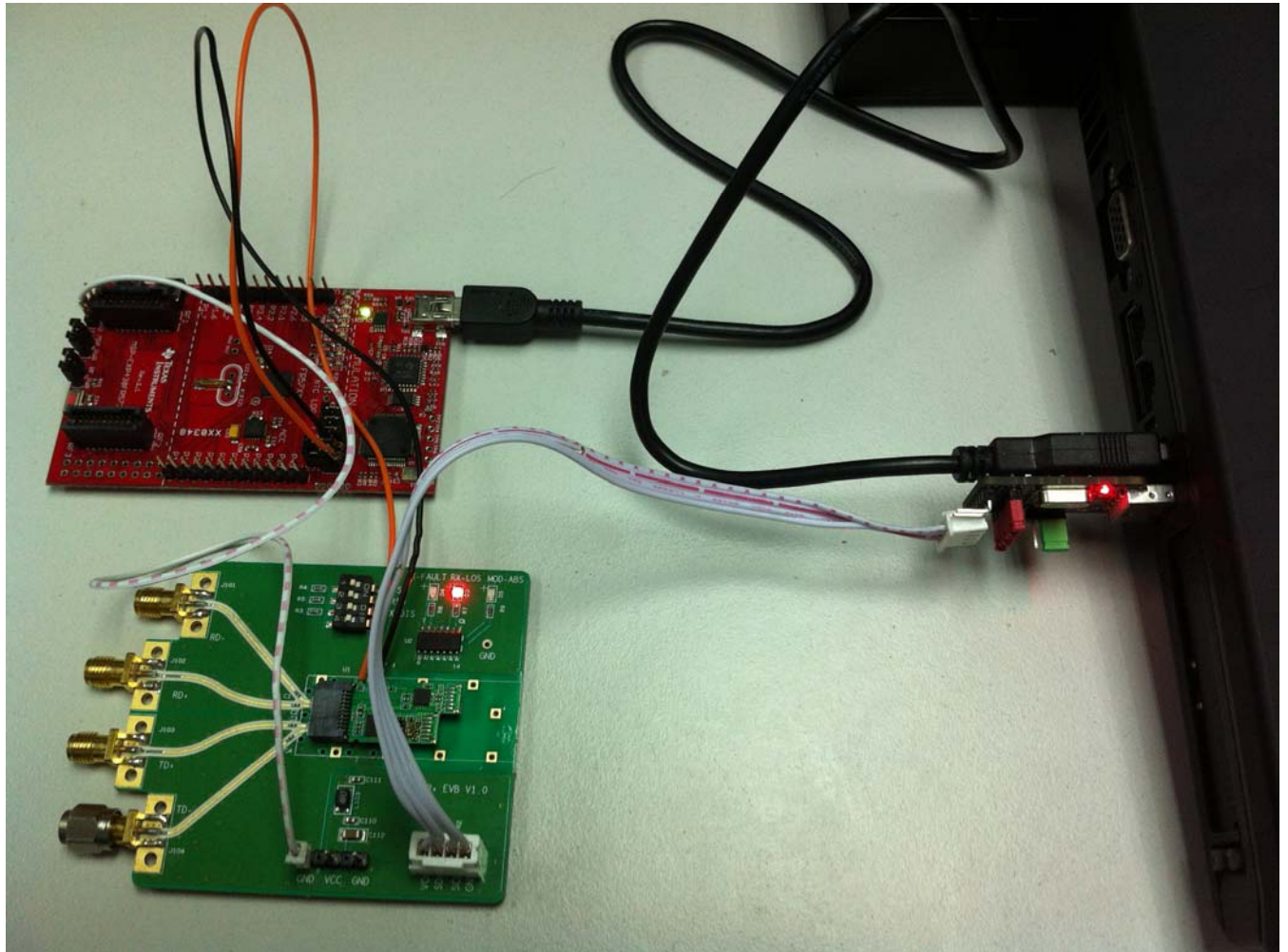
The screenshot displays two windows from a development environment:

- Watch 1:** A table showing the current values and memory locations of various variables.
 

Expression	Value	Location	T
A0_Serial_ID	""	Memory: 0x1C19	U
A2_Diagnostics	""	Memory: 0x1D19	U
ADC_Result	<array>	Memory: 0x1C02	U
ADC_Result_Sum	0	Memory: 0x1C0A	U
ADC_Result_Average	0	Memory: 0x1C0C	U
I2C_Slave_A0_Received_Memory_Add...	0x00	Memory: 0x1C0F	U
I2C_Slave_A0_Received_Bytes_Count	0x00	Memory: 0x1C10	U
Control_Data	Error (c...		
Control_Add	Error (c...		
Control_Start	Error (c...		
Control_Read_Out_Data	Error (c...		
ONET1101L_00H	0x00	Memory: 0x1C13	U
ONET1101L_01H	0x00	Memory: 0x1C14	U
ONET1101L_05H	0x00	Memory: 0x1C15	U
ONET1101L_04H	0x00	Memory: 0x1C16	U
ONET1101L_03H	0x00	Memory: 0x1C17	U
<click to edit>			
- Disassembly:** Shows assembly code for a function named 'main'. The code includes several function calls:
 

```

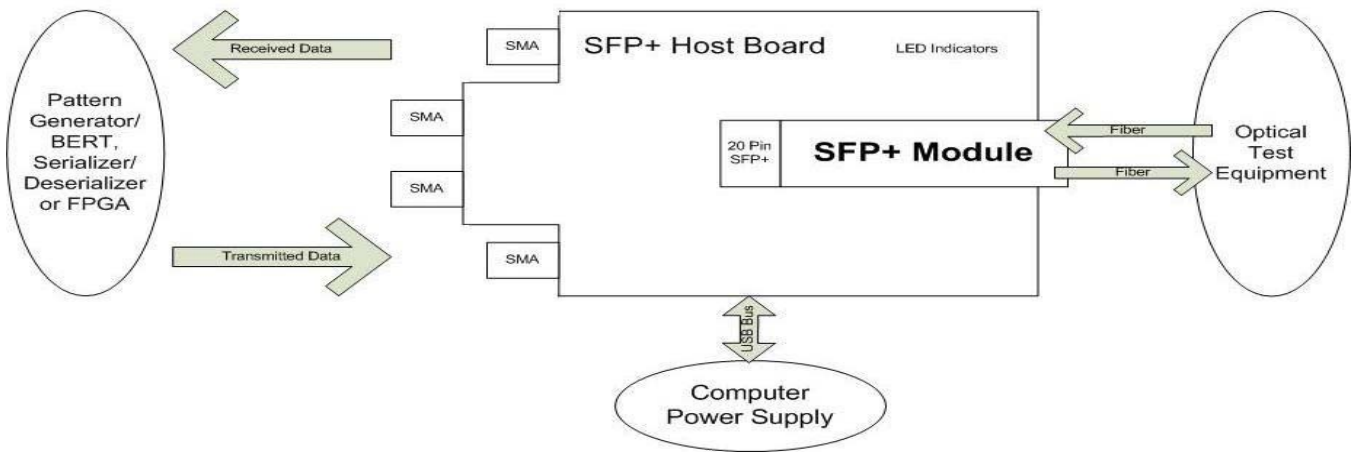
main:
00D500 13B0 D320      calla #System_Init
Real_Time_Monitor( );
00D504 13B0 D47A      calla #Real_Time_Monitor
Real_Time_Diag( );
00D508 13B0 D672      calla #Real_Time_Diag
Real_Time_Diag( );// diagnostic monitor in every period
00D50C 13B0 D672      calla #Real_Time_Diag
I2C_Command_Excution( );
00D510 13B0 C300      calla #I2C_Command_Exc
Real_Time_Monitor( );
00D514 13B0 D47A      calla #Real_Time_Monitor
            
```



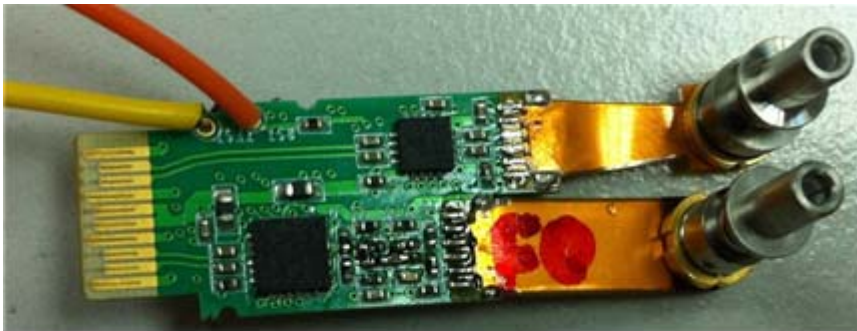
## 6 Test Configuration

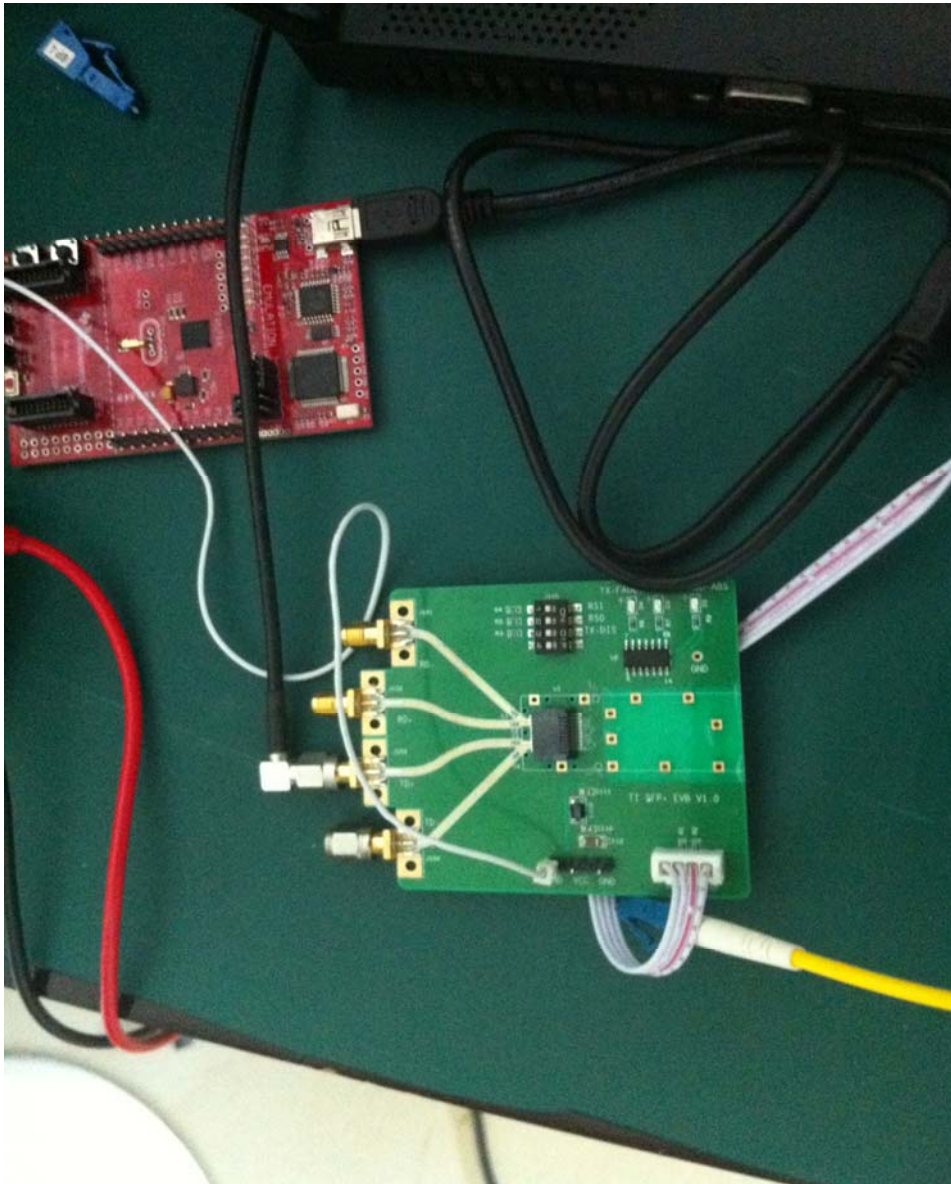
To evaluate performance of an assembled board, this application note also describes a complete test configuration, includes setup, hardware (evaluation board), and software (GUI).

### 6.1 Test Setup





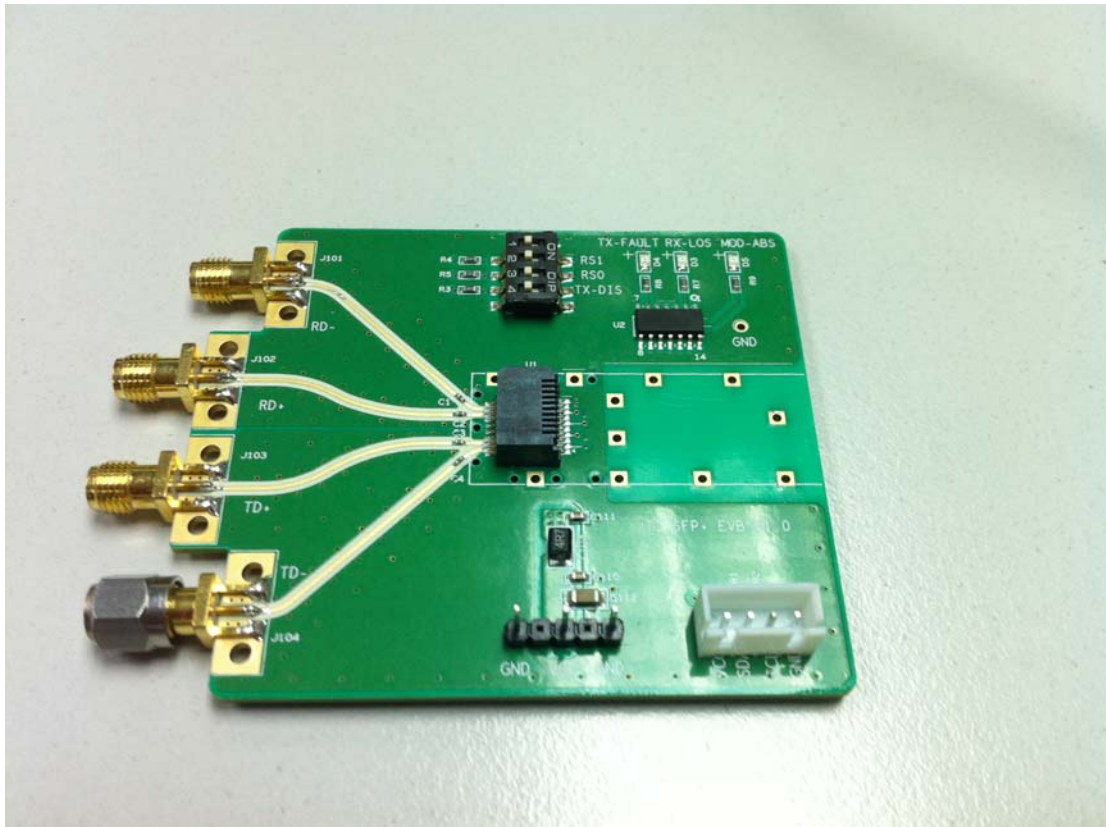




## 6.2 Evaluation Board

This high-speed, SFP+ host board is designed for evaluating SFP+ modules that operate at data rates up to 11.3 Gbps.

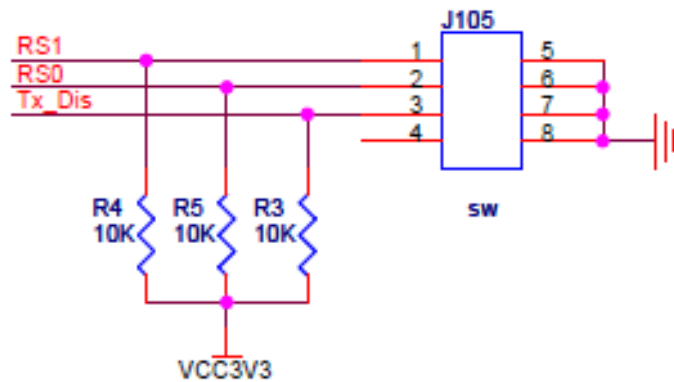
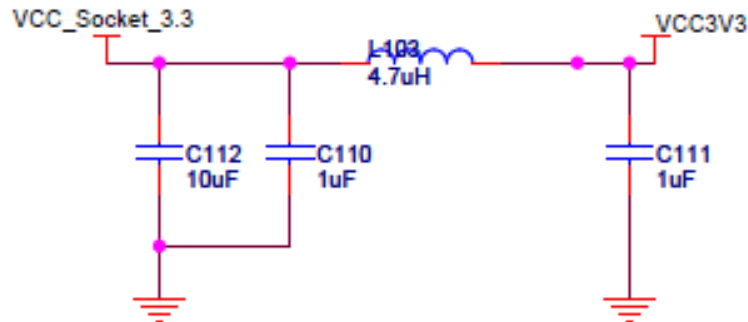
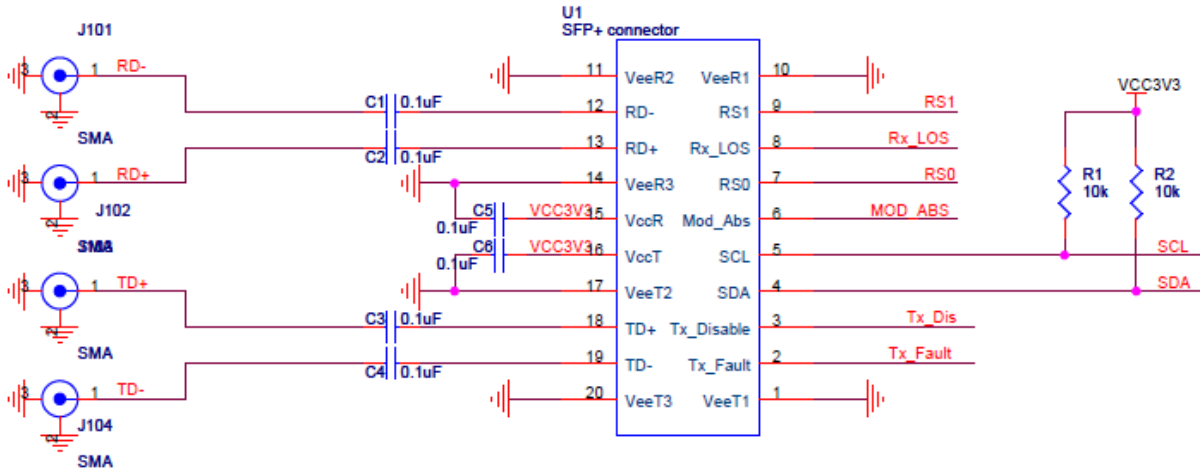
The host board can be used to test SFP+ and demo additional features for testing, monitoring, and programming TI SFP+ total solution.

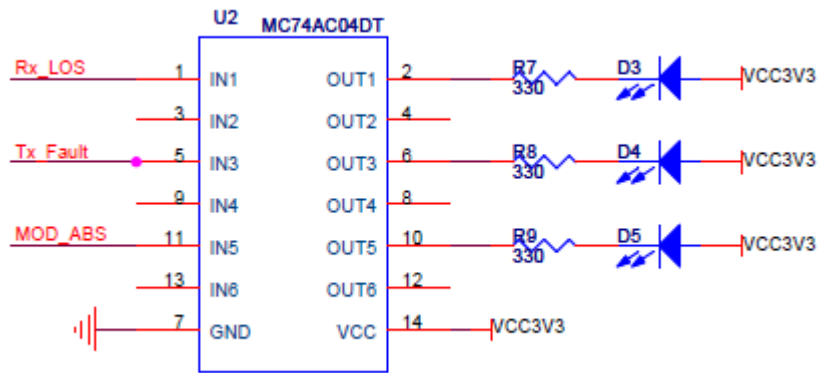


The evaluation board provides microstrip transmission lines and SMA connectors for transmitted and received data.

Supply current monitors, voltage monitors, and some digital I/O control/monitoring are provided through hardware (also the GUI).

### 6.3 Schematic





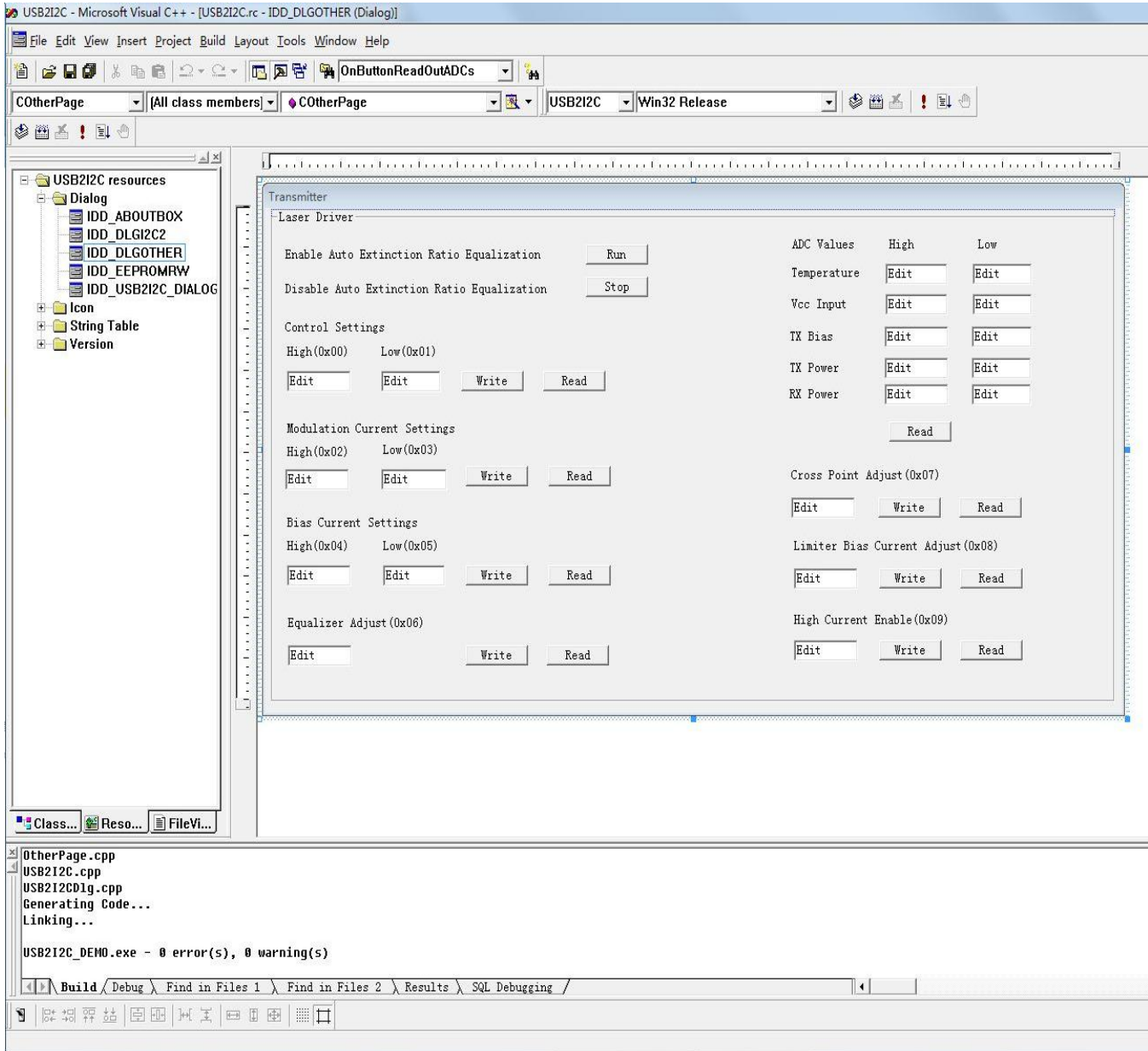
## 6.4 PCB Layout

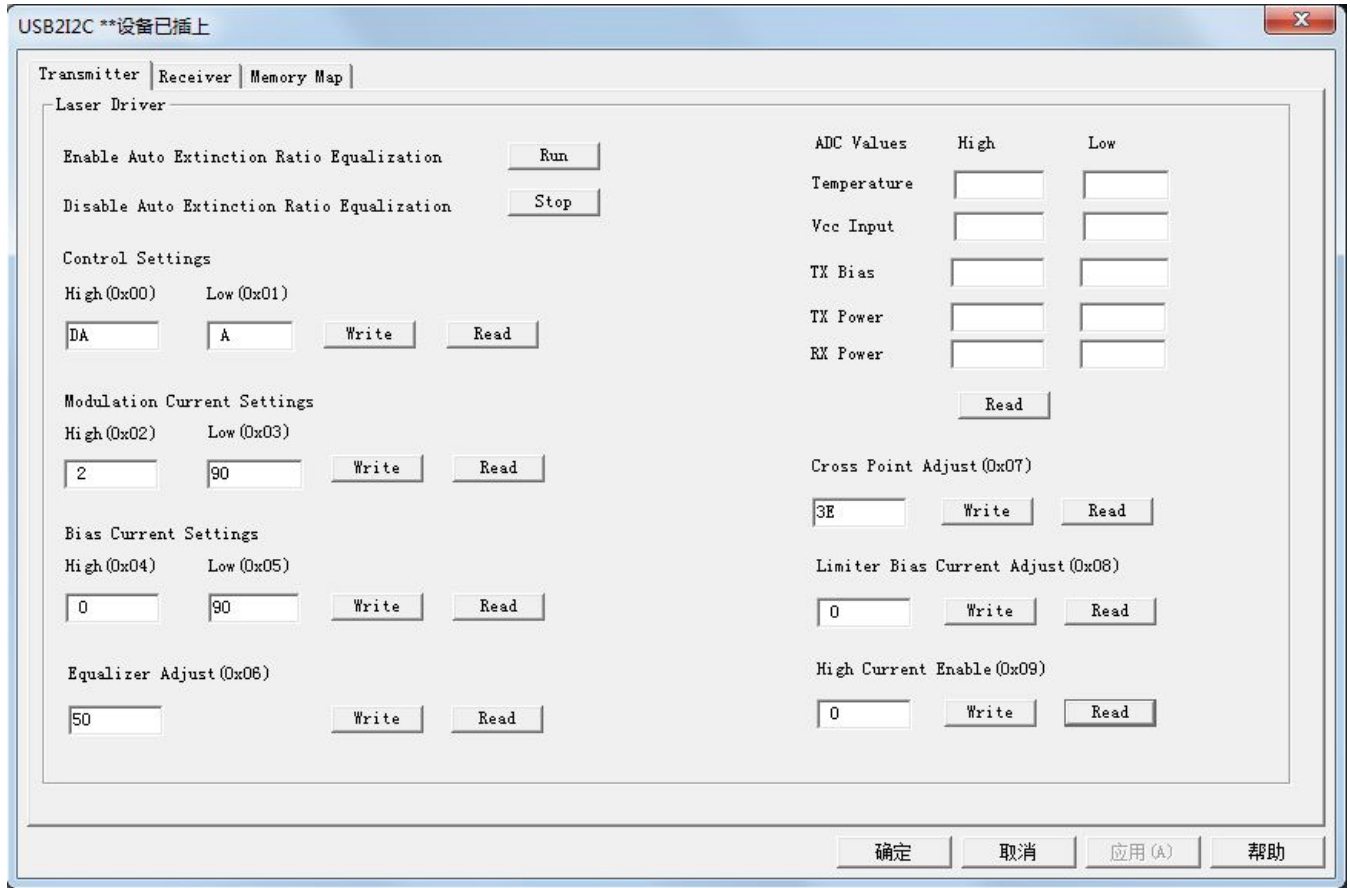
The evaluation board designed to use single-ended transmission lines.

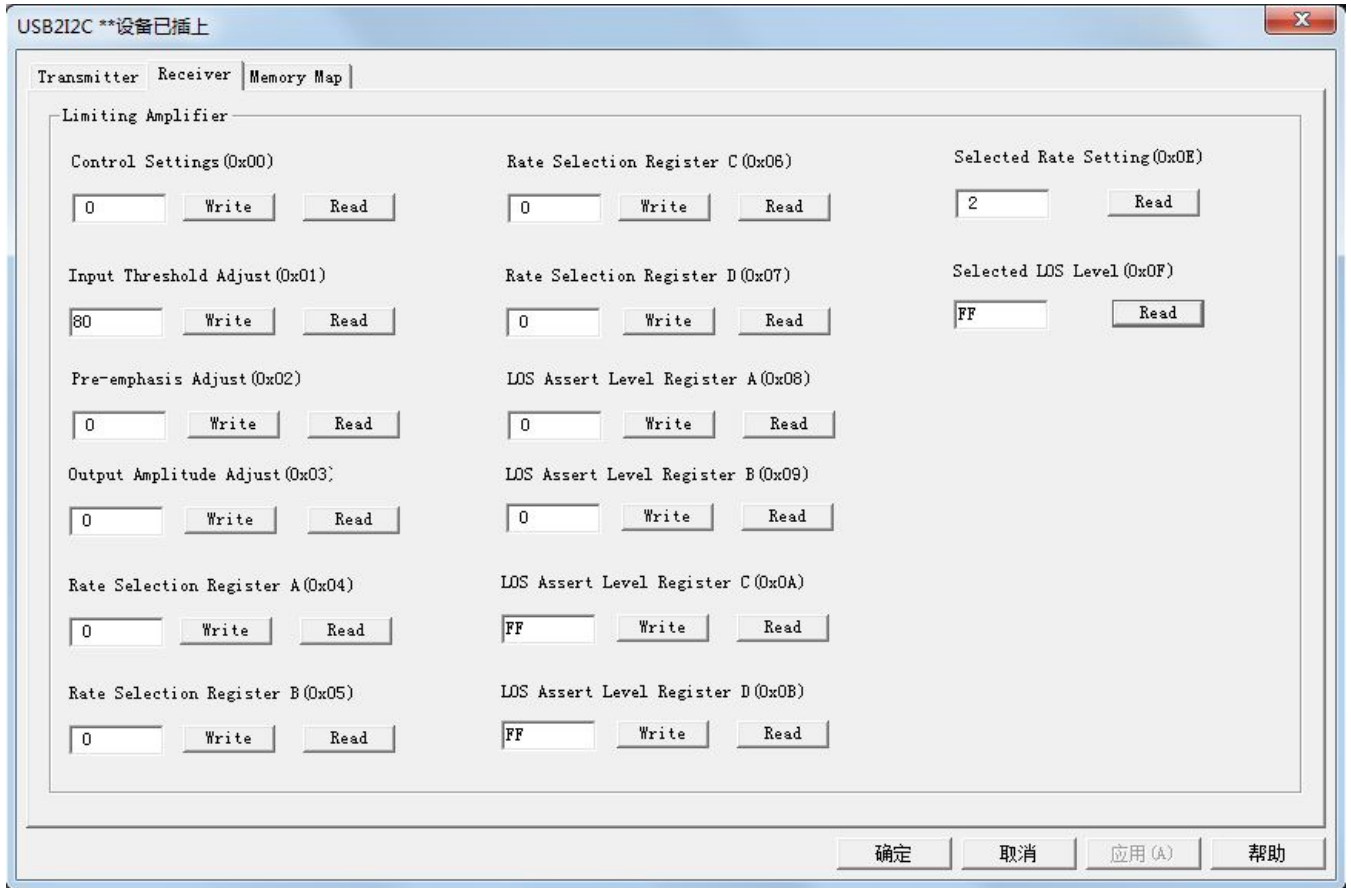
Changing the PCB layer profile can affect the impedance of these transmission lines and, therefore, the performance.

## 6.5 GUI

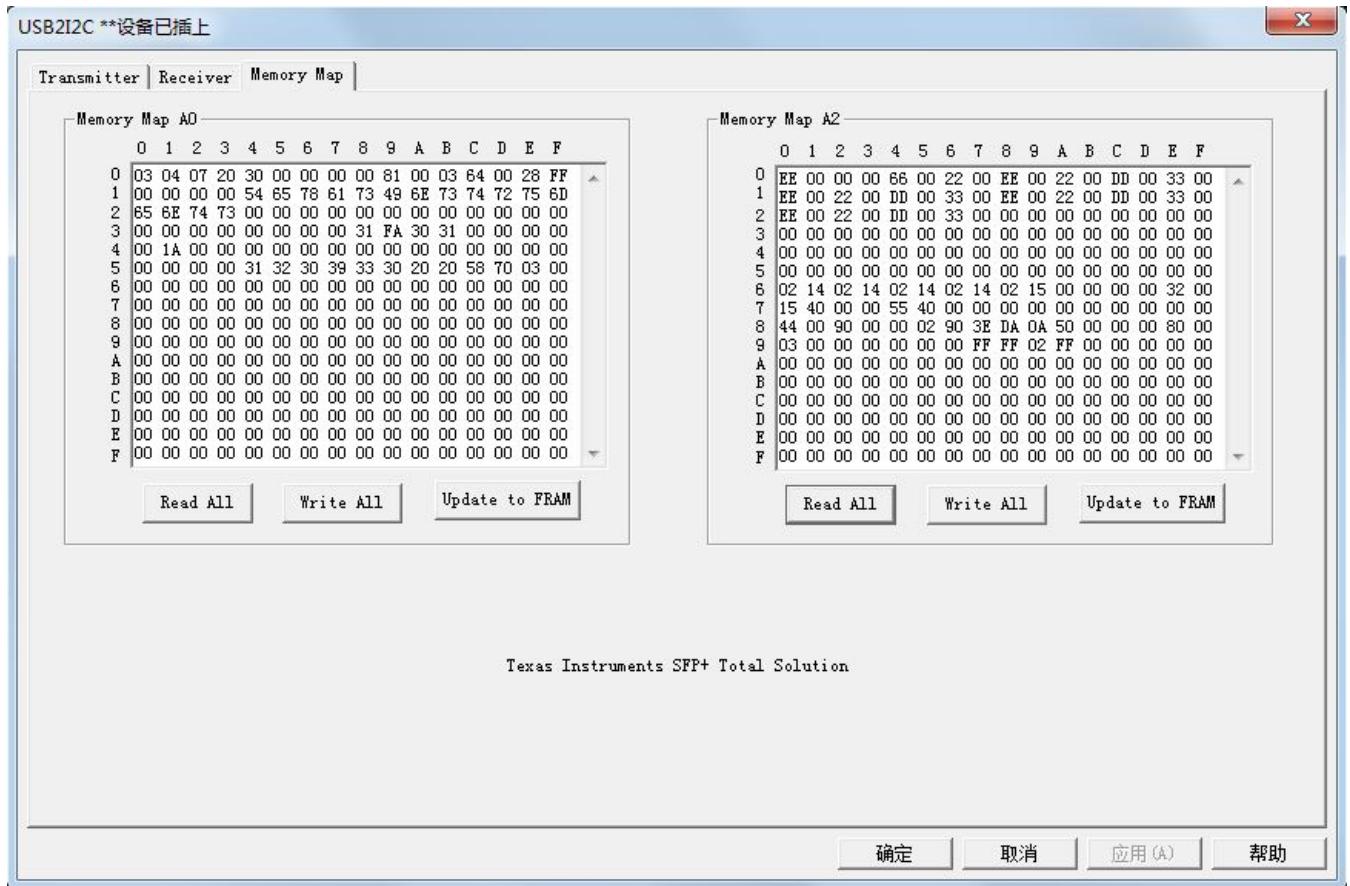
The GUI software is developed under VC++. It is compiled by VC++ 6.0.











## 7 References

1. *TI SLLA311 Considerations for PCB Layout and Impedance Matching Design in Optical Modules*, Daniel Long
2. *TI ONET1101 with Various TOSAs*, Alex Davidson

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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