Application Report
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SN65DSI83, SN65DSI84, and SN65DSI85 Hardware Implementation Guide

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ABSTRACT

This document includes guidelines and recommendations for implementing the SN65DSI83, SN65DSI84, or SN65DSI85 in system hardware. These recommendations are only guidelines and it is the designer's responsibility to consider all system characteristics and requirements. The engineers should refer to the datasheets for technical details such as device operation, terminal description, and so forth.

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1 Overview

1.1 What are SN65DSI83, SN65DSI84 and SN65DSI85?

The three devices: SN65DSI83, SN65DSI84 and SN65DSI85 will be referred to as *SN65DSI8X* in this document. SN65DSI8X is an MIPI DSI-to-LVDS bridge device that supports video modes in forward direction. The SN65DSI8X is primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format. The SN65DSI8X can be used between a GPU with DSI output and a video panel with LVDS inputs.

All three devices share the same pin out and package.

Table 1 lists a summary of the feature sets on these devices.

Table 1. SN65DSI8X Features Summary[(1)]

Part Name	Description	Max Resolution
SN65DSI83	Single Channel DSI to Single-Link LVDS	Suitable 1366x768/1280x800 60 fps at 24 bpp/18 bpp
SN65DSI84	Single Channel DSI to two Single-Link LVDS	1920x1200 60 fps at 24 bpp/18 bpp
SN65DSI85	Dual Channel DSI to two Single-Link LVDS	2560x1600 60 fps, 1920x1080p 120 fps at 24 bpp /18 bpp

(1) Each DSI Channel has 4 DSI data lanes + 1 CLK lane. Each LVDS link has 4 data lanes + 1 CLK lane.

2 Hardware Implementation Guidelines

2.1 Layout Recommendation

2.1.1 Parts and Component Placement

2.1.1.1 VCORE Pin

This pin outputs 1.1 V from the internal voltage regulator. The pin MUST have a 1-µF external capacitor to GND.

2.1.1.2 REFCLK

A series resistor is recommended near the RECLK source for EMI reduction purpose. If possible, bury the REFCLK trace in the inner layer, or minimize the trace length from the REFCLK terminal to the CLK source by placing the source near the SN65DSI8X REFCLK terminal, or do both.

2.1.1.3 Decoupling Capacitors

Decoupling capacitors should be placed near the power plane and power rails for the SN65DSI8X. The trace length between decoupling capacitors must be minimized to avoid large current loops and trace inductance. The use of four ceramic capacitors (two 0.1 µF and two 0.01 µF) near the SN65DSI8X is recommended.

2.1.2 Critical Routes

- DA*P/N and DB*P/N pairs should be routed together with controlled-differential 100-Ω impedance. Keep away from other high speed signals. Keep lengths within 5 mil of each other. Keep traces on layers adjacent to ground plane. The number of VIAS should be kept to a minimum. Each pair should be separated at least by 3 times the signal trace width. Route all differential pairs on the same group of layers (outer layers or inner layers) if not on the same layer.
- A_Y*P/N and B_Y*P/N pairs should be routed together with controlled differential 100-Ω impedance. Keep away from other high speed signals. Keep lengths within 5 mil of each other. Keep traces on layers adjacent to ground plane. The number of VIAS should be kept to a minimum. Each pair should be separated at least by 3 times the signal trace width. Route all differential pairs on the same group of layers (outer layers or inner layers) if not on the same layer.
- Ref CLK trace should be routed as short as possible.

2.1.3 Spread Spectrum CLK

The system is allowed to provide the center spread CLK input to the REFCLK or DSI CLK for EMI reduction purpose. The center spread CLK input to the REFCLK or DSI CLK is passed through to the LVDS CLK output A_CLKP/N or B_CLKP/N. The spread depth can be 0.5% to 2% with 30 Hz to 50 Hz of modulation frequency range.

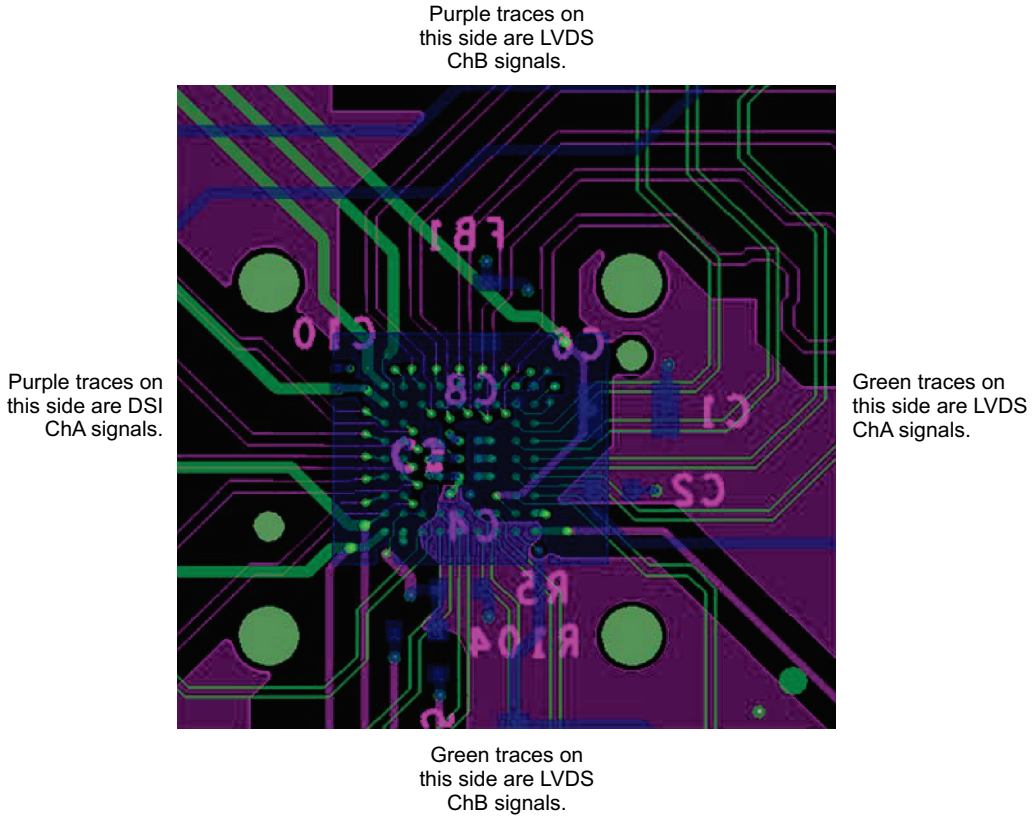

Figure 1. SN65DSI85 Layout Example

The layer stack up of the board in Figure 1 is as shown in the following:

6-layer PCB
Layer 1: Top component side
Layer 2: GND
Layer 3: Signal Route
Layer4: Power
Layer 5: GND
Layer 6: Bottom component side

2.2 RESET Implementation

The SN65DSI8X is reset by controlling the EN terminal (pin B1). The reset implementation defined in the datasheet should be followed for correct operation of the device after the reset.

Figure 2 and Figure 3 depict the reset timing. User should refer to the datasheet for further details on reset operation.

Figure 2 shows the EN implementation during cold start when the device is first powered on. T_{enable} must be always greater than T_{vcc}. In case of using the passive reset circuitry, this timing must be insured by using the correct values of R and C which could vary depending on the ramp up time of the system. The internal R value on the EN is 200 kΩ.

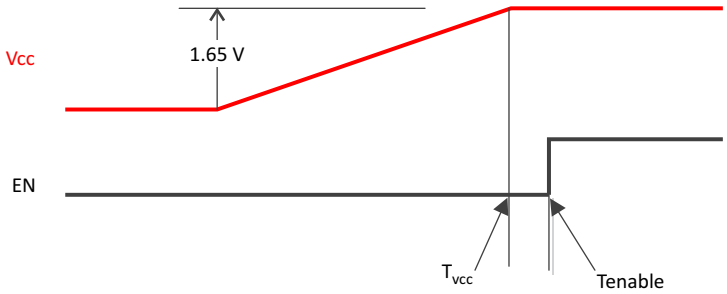

Figure 2. Cold Start Vcc Ramp Up to EN

Figure 3 shows the EN implementation while the device is powered on. The following timing must be met when the SN65DSI8X transitions from a normal operation state to a RESET or SHUTDOWN state while Vcc remains high.

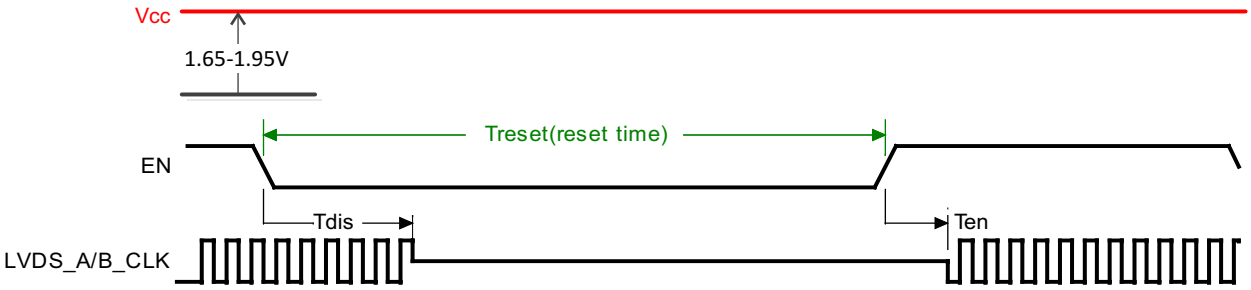

Figure 3. RESET or SHUTDOWN Timing When Vcc = HIGH

2.3 ADDR

The ADDR determines the least significant bit of the I^2C ADDR for the SN65DSI8X. This bit should be pulled high or low through a resistor depending on the I^2C address the system chooses to use for the SNDSI85. When this pin is pulled low, the device address is 0x2C, high 0x2D.

NOTE: When it is pulled high, it must be tied to the device Vcc such that this pin does not remain high when the device power is removed.

2.4 LVDS REVERSE Routing Option

The SN65DSI85 allows reversing or swapping the order of the LVDS pins via the register bit control at address 0x1A per the definitions below.

2.4.1 LVDS Even Odd Swap Option

By setting the 0x1A bit6 EVEN_ODD_SWAP bit in the CSR, the routing of even and odd pixels can be swapped. When this bit is set to 0 (default), odd pixels are routed to LVDS Channel A (A_Y*P/N) and even pixels routed to LVDS Channel B (B_Y*P/N). When this bit is set to 1, odd pixels are routed to LVDS Channel B (B_Y*P/N) and even pixels routed to LVDS Channel A (A_Y*P/N).

2.4.2 LVDS Reverse Pin Order Option

The order of the LVDS pins for LVDS Channel A or Channel B can be reversed by CSR configurations at the address 0x1A bits 5 CHA_REVERSE_LVDS and bit4 CHB_REVERSE_LVDS.

Table 2. Channel A LVDS Reverse Pin Order

Pin Number	CHA_REVERSE_LVDS=0 (Default)	CHA_REVERSE_LVDS=1
C8	A_Y0P	A_Y3P
C9	A_Y0N	A_Y3N
D8	A_Y1P	A_CLKP
D9	A_Y1N	A_CLKN
E8	A_Y2P	A_Y2P
E9	A_Y2N	A_Y2N
F8	A_CLKP	A_Y1P
F9	A_CLKN	A_Y1N
G8	A_Y3P	A_Y0P
G9	A_Y3N	A_Y0N

Table 3. Channel B LVDS Reverse Pin Order

Pin Number	CHB_REVERSE_LVDS=0 (Default)	CHB_REVERSE_LVDS=1
B3	B_Y0P	B_Y3P
A3	B_Y0N	B_Y3N
B4	B_Y1P	B_CLKP
A4	B_Y1N	B_CLKN
B5	B_Y2P	B_Y2P
A5	B_Y2N	B_Y2N
B6	B_CLKP	B_Y1P
A6	B_CLKN	B_Y1N
B7	B_Y3P	B_Y0P
A7	B_Y3N	B_Y0N

2.5 Unused DSI Channels or Lanes

Unused DSI input terminals (DA*N/P, DB*N/P) should be left unconnected or driven to LP11 state.

2.6 RSVD Pins

The RSVD1 and RSVD2 are reserved pins. Leave these unconnected for normal operation.

3 References

SN65DSI8X Datasheets (SLLSEB9, SLLSEC1, SLLSEC2)

4 Reference Schematics

Figure 4 schematics for the SN65DSI8X reference design.

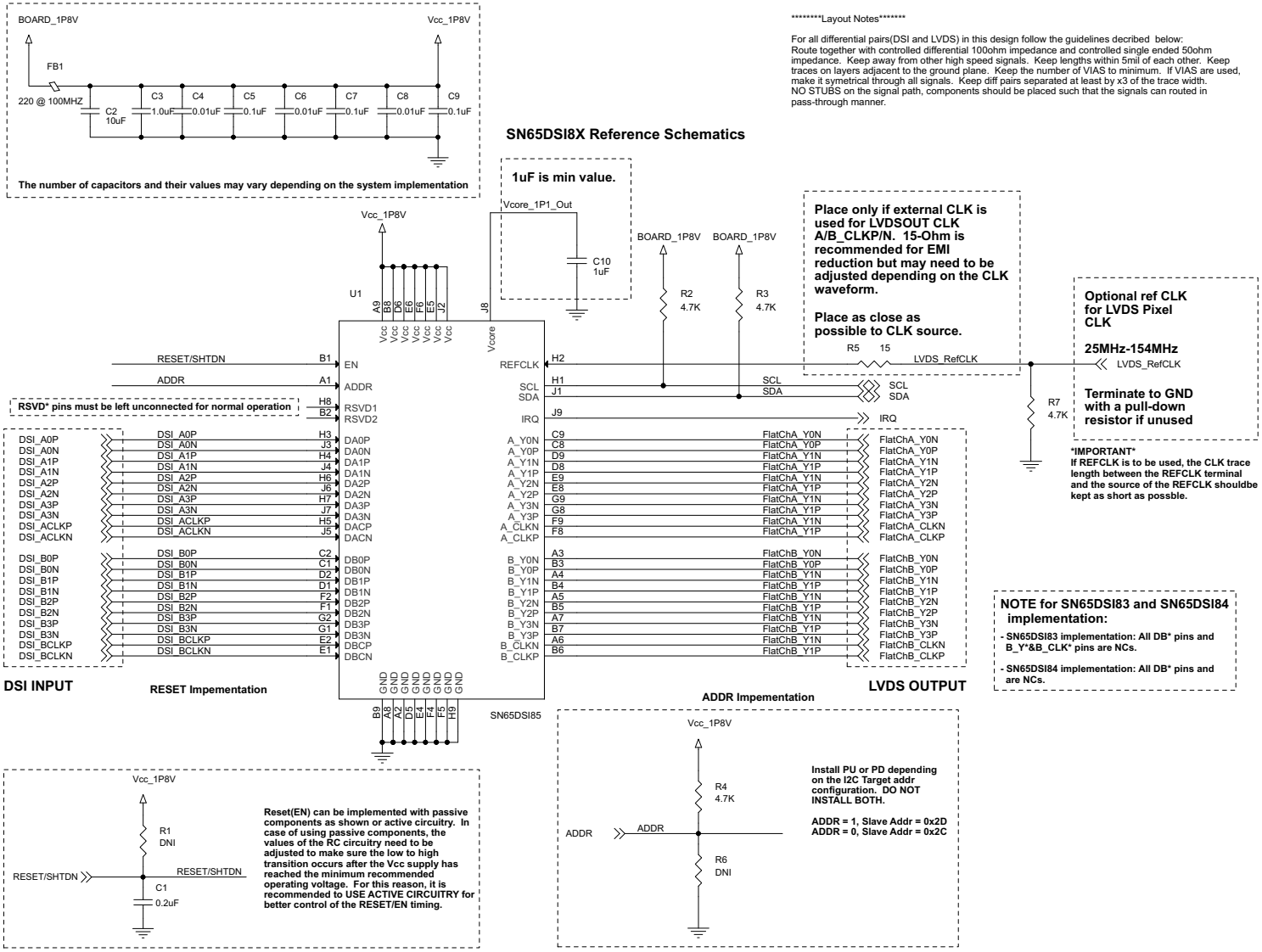

Figure 4. SN65DSI8X Reference Schematics

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