Application Report
SLLA402–May 2018

SN65LVPE502A Schematic Checklist

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ABSTRACT

The SN65LVPE502A is a dual-channel, single-lane USB 3.0 Gen 1 redriver and signal conditioner. Its supports data rates up to 5 Gbps. This device complies with USB 3.0 specification revision 1.0 supporting electrical idle condition. It complies with low frequency periodic signals (LFPS) for USB 3.0 power management modes. The schematic checklist shows an explanation of each device pin. The schematic checklist gives the recommended configuration for default operation. Use this information to check the connectivity for each SN65LVPE502A on a system schematic.

This document aids design at the system level for general applications. It should not be the only resource used. In addition to this list, customers are advised to use the information in the SN65LVPE502A datasheet to gain a full understanding of device functionality. Project collateral discussed in this application report can be downloaded from the following URL: www.ti.com/lit/zip/SLLA402.

Trademarks

1 SN65LVPE502A Schematic Checklist

Table 1. SN65LVPE502A Schematic Checklist

Pin Name	Pin Number(s) (RGE Packages)	Pin Description	Recommendation
Power Pins			
VCC	1,13	3.3 V (±10%) Positive Power Supply	Parallel array of one 1 µF and two 0.1 µF capacitors to GND.
GND	6, 10, 18, 21, PAD	Ground	Connected to Ground.
Configuration Pins			
EQ1	2	Tri-level configuration input pins for CH 1 Equalization.	Use 47 kΩ pull-down resistor for 3 dB of gain on CH 1. Refer to Table 1 in the datasheet for additional configurations. To avoid over equalizing data start at the lowest settings and increase until desired eye is achieved.
EQ2	17	Tri-level configuration input pins for CH 2 Equalization.	Use 47 kΩ pull-down resistor for 3 dB of gain on CH 2. Refer to Table 1 in the datasheet for additional configurations. To avoid over equalizing data start at the lowest settings and increase until desired eye is achieved.
DE1	16	Tri-level configuration input pins for CH 1 De-emphasis.	Use 47 kΩ pull-down resistor for 0 dB of de-emphasis on CH 1 output. Refer to Table 1 in the datasheet for additional configurations. To avoid over equalizing data start at the lowest settings and increase until desired eye is achieved.
DE2	3	Tri-level configuration input pins for CH 2 De-emphasis.	Use 47 kΩ pull-down resistor for 0 dB of de-emphasis on CH 2 output. Refer to Table 1 in the datasheet for additional configurations. To avoid over equalizing data start at the lowest settings and increase until desired eye is achieved.
OS1	15	Tri-level configuration input pins for CH 1 Output Swing.	Use 47 kΩ pull-down resistor for 0.9 x Vpp on CH 1 output. Refer to Table 1 in the datasheet for additional configurations. To avoid over equalizing data start at the lowest settings and increase until desired eye is achieved.
OS2	4	Tri-level configuration input pins for CH 2 Output Swing.	Use 47 kΩ pull-down resistor for 0.9 x Vpp on CH 1 output. Refer to Table 1 in the datasheet for additional configurations. To avoid over equalizing data start at the lowest settings and increase until desired eye is achieved.
EN_RXD	5	Active hgih device enable, has an internal 660-kΩ pull-down resistor.	Add a 4.7 KΩ Pull up to VCC for normal operation. Resets state machine when toggled.

Table 1. SN65LVPE502A Schematic Checklist (continued)

Pin Name	Pin Number(s) (RGE Packages)	Pin Description	Recommendation
USB Data Lines			
Device_TX1+	22	Differential output for 5 Gbps signal connected to a USB 3.0 Device.	Connect to the USB3.1 RXP/N terminals from an USB3 HOST, HUB or DEVICE using 0.1 uF AC coupling capacitors or connect to the TXP/N terminals from an USB3 connector using 0.1 uF AC coupling capacitors. These pins allow polarity swapping.
Device_TX1-	23		
Host_RX1+	12	Differential output for 5 Gbps signal connected to a USB 3.0 Host.	
Host_RX1-	11		
Host_TX2+	9	Differential input for 5 Gbps signal connected to a USB 3.0 Host.	Connect to the USB3.1 TXP/N terminals from an USB3 HOST, HUB or DEVICE using 0.1µF AC coupling capacitors or connect to the RXP/N terminals from an USB3 connector. NO AC coupling capacitors. These pins allow polarity swapping.
Host_TX2-	8		
Device_RX2+	19	Differential input for 5 Gbps signal connected to a USB 3.0 Device.	
Device_RX2-	20		
Misc. Pins			
RSVD	14	Reserved	Leave no-connected.
NC	2,3,4,6,14,18,24	No Connection	Leave no-connected.
Notes: Common mode chokes placed as close as possible to the USB connectors. Verify the pinout of the USB connectors. Verify pin-out of TUSB522P matches datasheet. Always refer to the datasheet of this device for complete descriptions of each pin. This document is made for RGE Packages.			

2 References

- SN65LVPE502x Dual Channel USB 3.0 Redriver and Equalizer Datasheet

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