Migrating From DS92LV1021A/DS92LV1212A 10-Bit SerDes to SN65LV1023A/SN65LV1224B

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TEXAS INSTRUMENTS

This document describes the main differences between the 10-bit Serializer/Deserializer (SerDes) pairs available from TI. While these SerDes pairs have the same functionality, there are some differences between them. Some of these differences may impact some applications and must be kept in mind when migrating from one device to another.

Introduction

A 10-bit SerDes pair consists of a 10-bit serializer and 10-bit deserializer that are usually used together as a chipset as shown in Figure 1. The SerDes pairs compared in this document are:

- SN65LV1023A Serializer and SN65LV1224B Deserializer
- DS92LV1021A Serializer and DS92LV1212A
 Deserializer
- DS92LV1023E Serializer and DS92LV1224
 Deserializer

These 3 pairs have the same functionality and are offered in the same 28-pin SSOP package and share the same pinouts. It is possible in many cases to interchange devices from different pairs. However, the serializer and deserializer devices from these 3 pairs are not identical and there are some differences between them which are outlined in the subsequent sections.

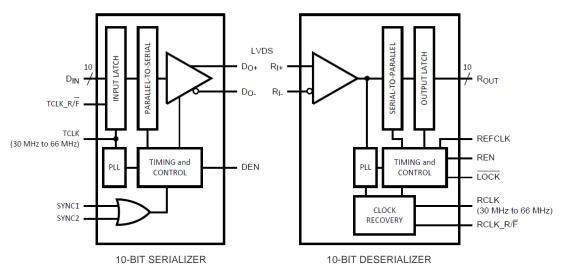
DS92LV1021A/DS92LV1212A vs. DS92LV1023E/DS92LV1224

The DS92LV1021A/DS92LV1212A and DS92LV1023E/DS92LV1224 have very similar characteristics except for 1 notable difference, which is the supported clock frequency range (and consequently the data throughput). The DS92LV1021A/DS92LV1212A pair supports a clock frequency of 16 to 40 MHz, while the DS92LV1023E/DS92LV1224 pair supports a clock frequency of 30 to 66 MHz. Table 1 lists some of the main differences between these 2 pairs. There are other minor differences in the values of some parameters. Refer to the *Electrical Characteristics* and *Switching Characteristics* tables in the respective data sheets for details.

The devices from these 2 pairs will be lumped together in the comparisons of the subsequent sections.

Table 1. Differences Between DS92LV1021A/ DS92LV1212A and DS92LV1023E/DS92LV1224

PARAMETER	DS92LV1021A/ DS92LV1212A	DS92LV1023E/ DS92LV1224
Clock Frequency	16 – 40 MHz	30 – 66 MHz
Short Circuit Current (Max)	40 mA / 85 mA	90 mA / 85 mA
Powerdown Supply Current (Max)	300 µA / 1 mA	500 µA / 1 mA







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Deserializer Comparison

The main differences between the deserializer devices are summarized in Table 2. As can be seen from the table, the SN65LV1224B has several enhancements over the DS92LV1212A and DS92LV1224, including a wider operating frequency range, an on-chip fail-safe feature, and a higher ESD rating. However, the tolerance spec on the REFCLK frequency for SN65LV1224B is much tighter than it is for DS92LV1212A and DS92LV1224. This may be significant for some applications. If an existing application using the DS92LV1212A or DS92LV1224 uses a REFCLK that is not within ±100 ppm of the operating transmission frequency (determined by TCLK on the serializer), then it is not possible to swap the DS92LV1212A or DS92LV1224 with the SN65LV1224B without changes to the design.

The power consumption of these devices is similar. The data sheets list I_{CC} values at the minimum and maximum frequencies supported by each device which vary from device to device, and hence the I_{CC} values listed also vary.

There are several other minor differences in the values of some parameters. Refer to the *Electrical Characteristics* and *Switching Characteristics* tables in the data sheets for details.

PARAMETER	SN65LV1224B	DS92LV1212A/ DS92LV1224	NOTES
Clock Frequency	10 – 66 MHz	16 – 40 MHz / 30 – 66 MHz	
REFCLK Tolerance	±100 ppm	±5% (0.95/t _{RCP} to 1.05/t _{RCP})	This is a potentially important difference
Failsafe Feature	On-chip	Need external PU/PD resistors	
Input Current (Max)	200 µA	15 µA	SN65LV1224B is higher due to on-chip failsafe biasing on LVDS side
Output Transition Time (Max)	2.5 ns	4 ns	LVTTL/LVCMOS output
PLL Lock Time (Max)	0.303 µs	1 µs / 0.8 µs	Powered up, with SYNCPAT, REFCLK = 66 MHz (40 MHz for DS92LV1212A)
ESD (HBM)	6 kV	2 kV	

Table 2. Differences Between Deserializers

Serializer Comparison

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The main differences between the serializer devices are summarized in Table 3. As can be seen from the table, the SN65LV1023A has several enhancements over the DS92LV1021A and DS92LV1023E, including a wider operating frequency range, integrated pullup/pulldown resistors on LVTTL inputs, and a higher ESD rating. The DS92LV1021A and DS92LV1023E are Bus-LVDS (BLVDS) devices with a higher current drive than typical LVDS drivers, producing a differential voltage of 270 mV (typical) over a 27- Ω load. The SN65LV1023A also has a high current drive LVDS driver producing 450 mV (typical) over a 27- Ω load.

Notice that the SN65LV1023A has a TCLK tolerance of ±100ppm, while the DS92LV1021A and DS92LV1023E do not have a tolerance spec for TCLK. The tolerance of ±100ppm for the SN65LV1023A is required if paired with the SN65LV1224B, because the latter requires tight tolerance on the REFCLK relative to the transmission clock which is dictated by TCLK of the serializer. For example, when using the SN65LV1023A with the SN65LV1224B and the desired transmission frequency is 50 MHz, TCLK of the SN65LV1023A must be 50 MHz ±100ppm and REFCLK of the SN65LV1224B must be 50 MHz ±100ppm. If any of the 3 serializers is paired with the DS92LV1212A or DS92LV1224 deserializer, then TCLK of the serializer can be any value in the supported frequency range and REFCLK of the deserializer has to be within ±5% of TCLK.

There are other minor differences in the values of some parameters. Refer to the *Electrical Characteristics* and *Switching Characteristics* tables in the data sheets for details.

Table 3. Differences	Between Serializers
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PARAMETER	SN65LV1023A	DS92LV1021A/ DS92LV1023E	NOTES
Clock Frequency	10 – 66 MHz	16 – 40 MHz / 30 – 66 MHz	
LVDS Differential output (RL = 27 Ω)	Typ: 450 mV Min: 350 mV	Typ: 270mV Min: 200mV	
Offset Voltage (Typ)	1.2 V	1.1 V	
Input Current (Max)	200 µA	10 µA / 15 µA	SN65LV1023A is higher due to pullup and pulldown resistors on the LVTTL/LVCMOS inputs
Output Transition Time (Max)	0.4 ns	0.75 ns / 0.4 ns	SN65LV1023A and DS92LV1023E have faster transition times on LVDS outputs to support the higher frequency
PLL Lock Time (Min)	1026 × t _{TCP}	510 x t _{TCP}	
TCLK Tolerance	± 100 ppm	N/A	See discussion above
ESD (HBM)	6 kV	2 kV	

It is important to note that despite the differences described in this document, the serializer and deserializer from different pairs can interoperate with each other in most cases. Intermixing devices from different pairs has been demonstrated on EVMs and by customers. Additionally, it is possible to replace one device (or pair) with another without making any changes to the design in most, but not all, applications.

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