TDP158 Configuration Guide

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ABSTRACT

The purpose of this document is to provide a quick start-up guide for the TDP158 device.

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1   Device Configuration Guide

1. **Choose I2C mode or pin-strap mode via I2C_EN:**
   - When I2C_EN is high, the device is in I2C mode and the configuration is done through I2C.
   - When I2C_EN is low, the device is in pin-strap mode and the configuration is done through the device pins.

2. **Choose transmit termination via TERM:**

   In pin-strap mode, when the TERM pin is configured as NC, there will be no transmit termination. When the TERM pin is connected low, the transmit termination will be set to 150- to 300-Ω. When the TERM pin is connected high, the transmit termination will be set to 75- to 150-Ω
   - For data rates greater than 3.4 Gbps, set TERM high.
   - For data rates less than 3.4 Gbps, set TERM as NC or low.

   When configured in I2C mode, TERM bits (Register 0x0Bh, bits [4:3]) need to be set manually.

3. **Choose clock slew rate settings via SLEW:**
   - In pin-strap mode, when the SLEW pin is configured as NC, the slew rate will be at its midrange value of 1–180 ps.
   - When SLEW is connected low, the slew rate is at its slowest at 203 ps.
   - When SLEW is connected high, the slew rate is at its fastest at 122 ps.
   - SLEW can also be configured with bits [7:6] in register 0x0Bh in I2C mode for the clock, and bits [1:0] in register 0x0Ah for the data. 2'b00 is the slowest and 2'b11 is the fastest.

4. **Choose input receive equalization via A0/EQ1 and A1/EQ2:**

For fixed equalization options, see Table 1.

Table 1. Receiver EQ Programming and Values

RX EQ (dB)	Pin Control [1]	Global I2C Control	Independent Lane Control I2C Control [2]			
	{EQ2,EQ1}	P0_Reg0D[6:3]	D2 P0_Reg4E[3:0]	D1 P0_Reg4E[7:4]	D3 P0_Reg4F[3:0]	CLK[2][3] P0_Reg4F[7:4]
2	2'b00	4'b0000	4'b0000	4'b0000	4'b0000	4'b0000
3	2'b0Z	4'b0001	4'b0001	4'b0001	4'b0001	4'b0001
4		4'b0010	4'b0010	4'b0010	4'b0010	4'b0010
5	2'b01	4'b0011	4'b0011	4'b0011	4'b0011	4'b0011
6.5	2'bZ0	4'b0100	4'b0100	4'b0100	4'b0100	4'b0100
7.5		4'b0101	4'b0101	4'b0101	4'b0101	4'b0101
8.5	2'bZZ	4'b0110	4'b0110	4'b0110	4'b0110	4'b0110
9		4'b0111	4'b0111	4'b0111	4'b0111	4'b0111
10	2'bZ1	4'b1000	4'b1000	4'b1000	4'b1000	4'b1000
11	2'b10	4'b1001	4'b1001	4'b1001	4'b1001	4'b1001
12		4'b1010	4'b1010	4'b1010	4'b1010	4'b1010
13		4'b1011	4'b1011	4'b1011	4'b1011	4'b1011
14		4'b1100	4'b1100	4'b1100	4'b1100	4'b1100
14.5	2'b1Z	4'b1101	4'b1101	4'b1101	4'b1101	4'b1101
15		4'b1110	4'b1110	4'b1110	4'b1110	4'b1110
15.5	2'b11	4'b1111	4'b1111	4'b1111	4'b1111	4'b1111

[1] For Pin Control 0 = 1-kΩ pulldown resistor to GND, 1 = 1-kΩ pullup resistor to VCC, Z = Floating (No Connect)
[2] Individual Lane control is based upon the pin names with no swap
[3] The CLK EQ in HDMI mode is controlled by register P0_Reg0D[2:1]

5. **Choose pre-emphasis settings via SDA_CTL/PRE:**

- In pin-strap mode, when the SDA_CTL/PRE pin is configured as low, no pre-emphasis is applied. When PRE_SEL is connected high, 3.5-dB pre-emphasis is applied.
- Pre-emphasis settings can also be configured in register 0x0Ch in I2C mode.

2   Summary

The guidelines in this application report serve as a starting point for configuring the TDP158 device for your application.

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