TIOS101 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TIOS101DMW (VSON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

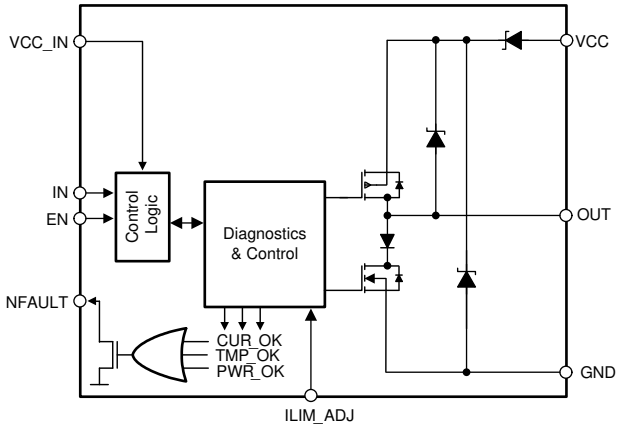

Figure 1. Functional Block Diagram

The TIOS101DMW was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TIOS101DMW based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS, ASIC, Analog & Mixed ≤ 50 V Supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TIOS101DMW in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open or HiZ	15%
OUT stuck high or low	20%
OUT functional, not in specification voltage or timing	60%
NFAULT false trip or fails to trip	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TIOS101DMW. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to supply (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the TIOS101DMW pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TIOS101DMW datasheet.

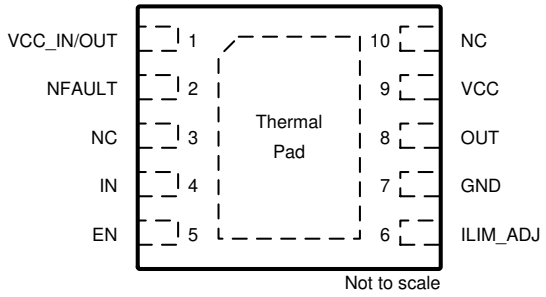

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All conditions meet recommended operating conditions.

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC_IN	1	VCC_IN forced low.	B
NFAULT	2	High ICC current during normal NFAULT inactive internal logic conditions. Constant external Fault active indication	B
NC	3	None	D
IN	4	High side output switch is stuck high when EN(pin 5) is high	B
EN	5	Device Driver is always tri-stated	B
ILIM_ADJ	6	Device operates at maximum current limit	D
GND	7	None	D
OUT	8	High ICC current during logic high output transitions due to supply crowbar conditions.	A
VCC	9	Device is unpowered	B
NC	10	None	D

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC_IN	1	Device logic will not function	B
NFAULT	2	No NFAULT information provided to the Sensor FE/Micro	C
NC	3	None	D
IN	4	No data can be transmitted from the Sensor FE/Micro to the output	B
EN	5	Device is always tri-stated	B
ILIM_ADJ	6	Device operates at maximum current limit	D
GND	7	Device is unpowered	B
OUT	8	No communication from Sensor FE/Micro to bus takes place	B
VCC	9	Device is unpowered	B
NC	10	None	D

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCC_IN	1	NFAULT	NFAULT stuck high and high ICC current during internal NFAULT active conditions	B
NFAULT	2	NC	None as long as NC is not connected to anything external to the device	D
NC	3	IN	None as long as NC is not connected to anything external to the device	D
IN	4	EN	If IN and EN are driven to different states communication and device state can be compromised	B
EN	5	NA	None	D
ILIM_ADJ	6	GND	Device operates at maximum current limit	D
GND	7	OUT	High ICC current during logic high output transitions due to supply crowbar conditions.	A
OUT	8	VCC	High ICC current during logic low output transitions due to supply crowbar conditions.	A
VCC	9	NC	None as long as NC is not connected to anything external to the device	D
NC	10	NA	None	D

Table 8. Pin FMA for Device Pins Short-Circuited to supply VCC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC_IN	1	Absolute maximum operating condition exceeded	A
NFAULT	2	Absolute maximum operating condition exceeded	A
NC	3	None as long as NC is not connected to anything external to the device	D
IN	4	Absolute maximum operating condition exceeded	A
EN	5	Absolute maximum operating condition exceeded	A
ILIM_ADJ	6	Absolute maximum operating condition exceeded	A
GND	7	Absolute maximum operating condition exceeded	A
OUT	8	High ICC current during logic low output transitions due to supply crowbar conditions.	A
VCC	9	NA	D
NC	10	None as long as NC is not connected to anything external to the device	D

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