Application Brief

Converting SPI to GPIO Through Digital Isolators

Digital isolators like the ISO7741 are widely used in PLC I/O modules for high-speed communication between field and back-end side electronics. Serial protocols like SPI are transparently isolated with data rates up to 50 Mbit. If isolation of general purpose input/output (GPIO) signals at lower speed and low channel count is required, optocouplers still play an important role as the cost per channel may be an advantage.

Digital isolator for GPIO isolation

The advantage of the optocoupler disappears with the increasing number of isolating channels as each signal needs separate isolation. A digital isolator method with a shift register becomes interesting as the number of isolated channels remains constant. Figure 1 shows a block diagram of a 16-channel digital output module with diagnostics feedback.

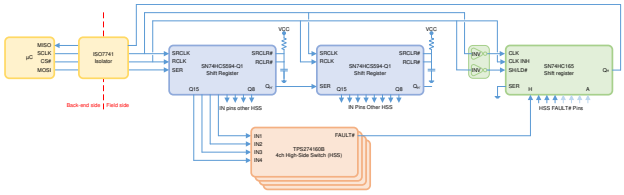

Figure 1. Block Diagram

The microcontroller provides the serial interface (here SPI), which is isolated by the ISO7741 with four channels. Three channels (SCLK, CS#, and MOSI) are isolated in the forward direction towards the field side, one channel (MISO) isolates in the reverse direction.

The blueish parts in the block diagram support general-purpose output functionality and control the INx pins of the eight 4-channel high-side driver TPS274160. The serial-to-parallel shift register SN74HCS594-Q1 receives the data bits at the SER pin. Data bits are shifted-out with a delay of eight SCLK cycles at pin QH'. Two daisy chained SN74HCS594-Q1 require a data frame with a length of 16 bit to provide a new set of data to the shift registers (see also Figure 2). The 16 INx signals are updated simultaneously with the rising CS# edge. The SN74HCS594-Q1 features Schmitt-trigger inputs for enhanced noise immunity. After power-up all outputs are set low.

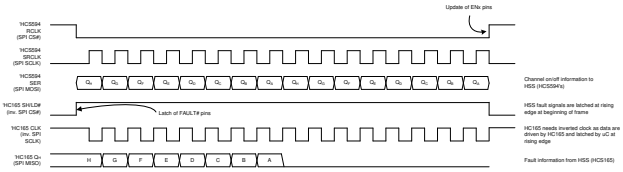

Figure 2. Timings

The greenish parts in the block diagram support general-purpose input functionality (FAULT# pins of the four TPS274160 devices) with the parallel-to-serial shift register SN74HCS165. The data bits are shifted-out at pin QH at the rising edge of CLK. As the SPI uses the same edge to shift-in receiving data, the SCLK signal needs to be inverted for the SN74HCS165. To provide most recent FAULT# pin levels to the controller the FAULT# pins are latched at the beginning of the transfer with the falling CS# edge. As the input pins are latched at the rising edge of SH/LD# pin the CS# signal needs also inversion. Parts with two inverters per package are available, such as the SN74LVC2G14 with Schmitt-trigger inputs. The CLK INH pin is connected to the CS# signal to ignore unwanted SCLK transition outside a data frame.

The SPI implementation of the MSP430 family allows the selection of the polarity during inactive state and the latching and driving edge of SLCK. A SCLK inactive low with latch of data on the first edge is required to satisfy the interface for the SN74HCS594-Q1 device.

The maximum update rate for the INx and FAULT# is dependent on the maximum SCLK switching frequency, the setup and hold timings of the SPI signals, the delay of the isolator and the supply voltage of the logic. Detailed calculations are out of the scope of this document, but an update rate of 100 kHz (minimum) is possible with a power supply of 3.3 V, sufficient for a standard digital output module.

Comparison of the silicon-based isolation vs. optocoupler

The control of a larger number of independent GPIO signals by a digital isolator brings the following advantages compared to a per-channel isolation using an optocoupler.

Power consumption

The power consumption is independent of the channel count and the inputs of the digital isolator provide high-impedance inputs. Optocoupler power consumption can be 10 × of a digital isolator when configured in an SPI interface. The current is provided either by a transistor or directly from the control signal of the controller.

Size and height

The digital isolator ISO7741 is available in a small 5-mm × 6-mm SOIC package; the shift registers in TSSOP packages. The example application requires a board space of about 100 mm^2 while the same solution with optocouplers (6 devices with 4 channels per package) requires about 275 mm^2.

Update rate

For this example, the SPI clock speed must be at least 17 × the update rate of the required INx and FAULT# update rate. The delay of a standard optocoupler is in the same ball park and dependent on the load resistance, but also on internal storage, rise and fall times.

Processor resources

Processor resources for the introduced approach are independent of the channel count. Only four processor pins for the SPI are required. Most SPI implementations today are buffered, that is, cycle-accurate back-to-back transfers are possible. Controller including a direct memory access (DMA) triggered by SPI interrupts reducing the software overhead to a memory read or write. In contrast, each optocoupler requires a separated controller GPIO line. GPIO control by port pin may not be as accurate as software is involved. Even an interrupt-driven implementation normally cannot guarantee a cycle-accurate update of the controller port pins.

Scalability

The solution is expandable in multiples of 8 by adding shift registers to the signal chain. As shown, no review of processor resources is needed if the channels count changes.

BOM count

The BOM is limited to the ISO7741DBQ and one or more serial shift register, one dual-inverter for the input functionality, and some bypass capacitors. The amount of optocouplers is given be the isolating channels, but an optocoupler with multiple channels per device are available. Each optocoupler needs at least a current-limiting resistor at the input and a pullup resistor at the output if an open-collector output is used.

Aging

Digital isolators are more reliable as optocouplers, which is important especially in industrial 24 hours per day, 7 days per week applications with long runtimes.

References

- ISO7741 product page
- TPS274160 product page
- SN74HCS594-Q1 product page
- SN74HCS165 product page
- SN74LVC2G14 product page

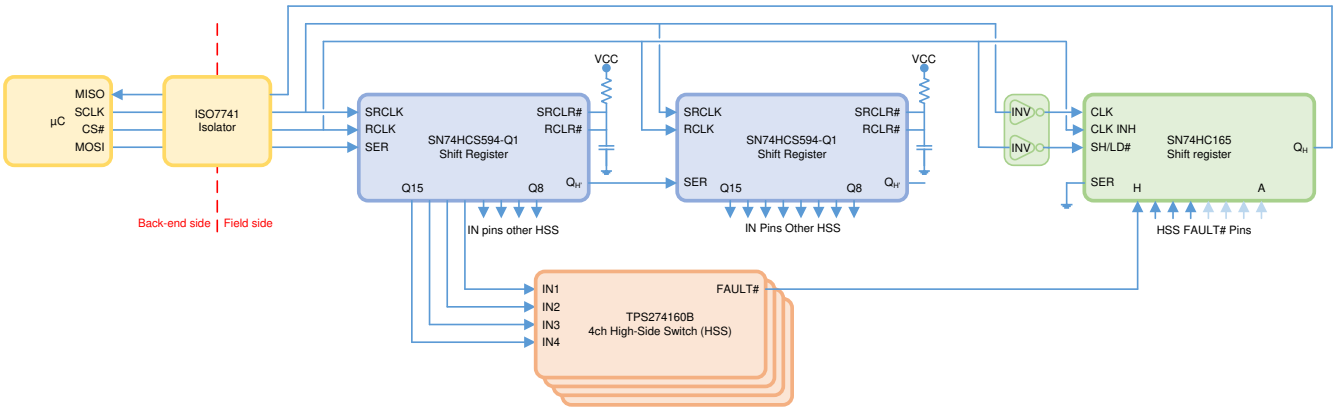

Figure 3. Block Diagram

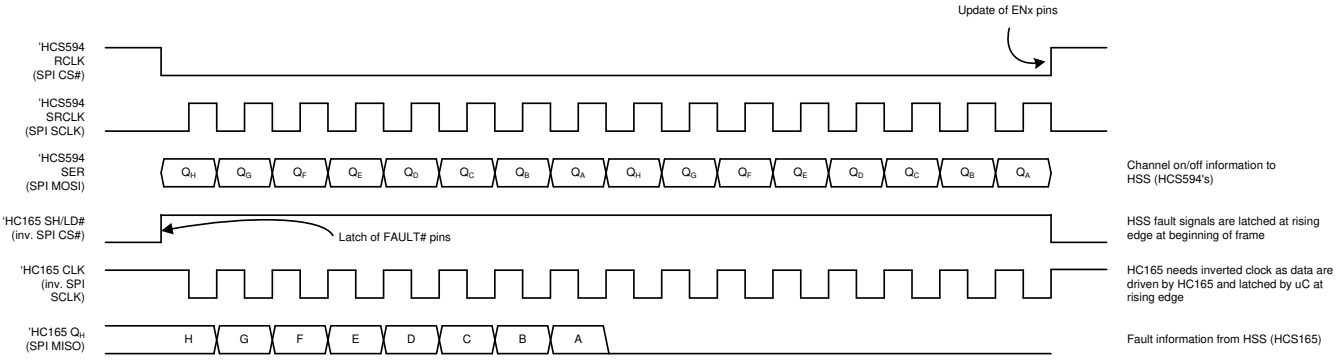

Figure 4. Timings

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