Application Report

Power On Reset Requirement of HD3SS2522

Brian Zhou, Roy Hsu

ABSTRACT

This application report reviews the power on reset circuit of HD3SS2522 device and describes the requirements of proper power on reset of the device. An external capacitor with the right value is recommended on RST pin as well.

Table of Contents

List of Figures

Trademarks

1 Introduction

HD3SS2522 is a high speed USB3 multiplexer with integrated DFP CC controller. The device provides Configuration Channel (CC) logic for determining USB port attach/detach, cable orientation, and VCONN sourcing. The HD3SS3220 can be configured as a Downstream Facing Port (DFP). There is a MCU MSP430 inside HD3SS2522, this MCU handles control of CC logic and associated GPIO operation which include power on reset circuit.

This article presents the power on reset circuit of HD3SS2522 and the requirement of power on reset.

2 Power On Reset Circuit

Figure 2-1 shows the system reset circuitry for power-on reset (POR) . Different events trigger these reset signals and different initial conditions exist depending on which signal was generated.

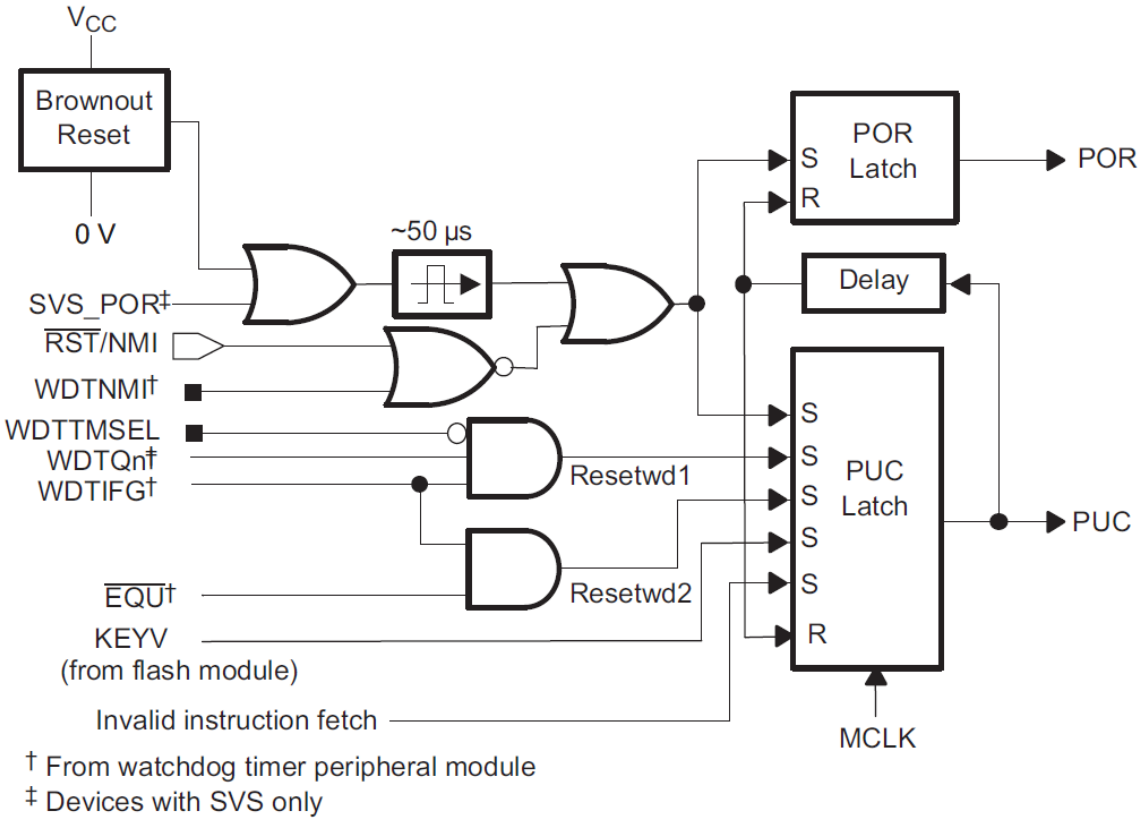

Figure 2-1. Power On Reset Circuit

POR is a device power on reset. A POR can be generated by the following two events:

- Powering up the device (BOR).
- A low signal on the RST pin when configured in the reset mode.

The brownout reset circuit (BOR) detects low supply voltages such as when a supply voltage is applied to or removed from the VCC terminal. The brownout reset circuit resets the device by triggering a POR signal when power is applied or removed. The operating levels are shown in Figure 2-2.

The POR signal becomes active when VCC crosses the VCC(start) level. It remains active until VCC crosses the V(B_IT+) threshold and the delay t(BOR) elapses.

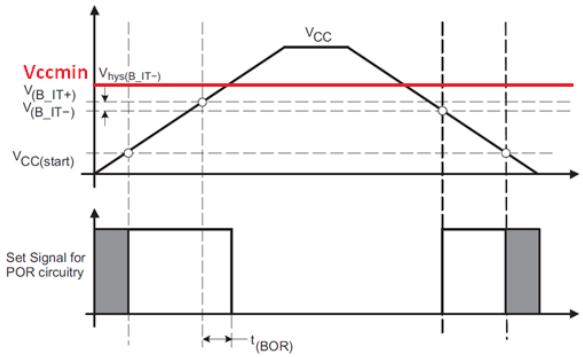

Figure 2-2. POR and BOR vs. Supply Voltage

Another way to generate POR is RST. At power-up, the RST pin is configured in the reset mode. The function of the RST pins is selected in the watchdog control register WDTCTL. If the RST pin is set to the reset function, the CPU is held in the reset state as long as the RST pin is held low. After the input changes to a high state, the CPU starts program execution at the word address stored in the reset vector, 0FFFEh, and the RSTIFG flag is set.

3 Power On Reset Requirement

From above power on reset circuit, two events will generate POR signal: BOR and RST.

During power up, the CPU begins code execution following a period of td(BOR) after VCC= V(B_IT–)+ Vhys(B_IT–). The default settings must not be changed until VCC≥VCC(min), where VCC(min) is the minimum supply voltage for the desired operating condition.

But there could be a condition when POR signal is getting released before Vcc has reached a min value for a very slow ramping Vcc, device may get unexpected execution.

Based on MSP430 data sheet, typical V(B_IT–) is 1.35 V, Vhys(B_IT–) is 140mv and VCC(min) is 1.8 V. So if POR signal is released between 1.49 V and 1.8 V, device is in uncertainty condition. To make sure device getting successful power on reset, td(BOR) should be longer than Vcc reaching 1.8 V.

BOR is fixed for each device, typical td(BOR) is 2ms. If Vcc ramping is slow, RST can be used to delay td(BOR), either controlled by external GPIO or adding external RC circuit on RST pin as shown in Figure 3-1.

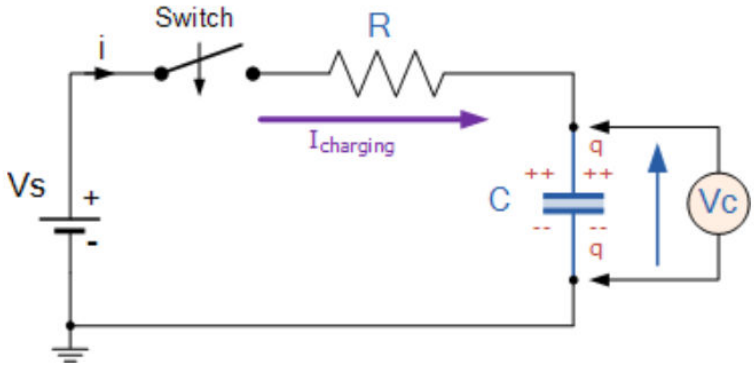

Figure 3-1. RC Charging Circuit

To calculate the RC value, let's look at the RC charging curve below. Assume RC time constant T=RC and Vs is 3.3 V. To reach Vmin =1.8 V, time delay is about 0.8T. So RC is equal to Td/0.8, Td is the time delay for Vcc to reach 1.8 V. To get C value, we need to measure Td for each system.

When R is 10k and Td is 5ms, we can get RC=5ms/0.8 and C is 0.625uf.

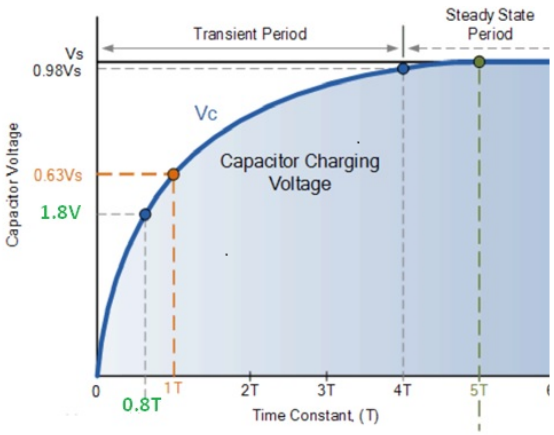

Figure 3-2. RC Charging Circuit Curve

4 Summary

There is an internal power on reset circuit BOR inside HD3SS2522 which trigger POR signal, but POR signal could be released before power supply reaching the min working voltage 1.8 no-break for a slow ramping supply. To get device reset properly, an external capacitor with the right value is recommended on RST pin.

5 References

- Texas Instruments, *MSP430x2xx Family User's Guide*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265