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ABSTRACT

The TCAN455x family of devices are Controller Area Network Flexible Data Rate (CAN FD) controllers with integrated transceivers and a SPI interface. A 20 MHz or 40 MHz clock is required with either a crystal resonator placed between the OSC1 and OSC2 pins, or a single-ended clock input from the microprocessor or some other clock source can be supplied to the OSC1 pin while the OSC2 pin is grounded. Due to the support of both types of clock inputs, when a crystal resonator is used, some extra care must be taken to optimize the circuit components to guarantee stable operation. This application report discusses the crystal resonator optimization procedures, but assumes the reader has some basic understanding of crystal oscillators.

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1 Introduction

The TCAN455x family of devices uses a Pierce oscillator based design that operates in the inductive region between a crystal's parallel and series resonant frequencies for a wide range of quartz crystals up to 40 MHz with a maximum ESR of 60 ohms and with load capacitance (CL1=CL2) requirements ranging between 8 pF and 24 pF. It is also capable of operating with a single-ended clock source instead of a quartz crystal supplied to the OSC1 pin, automatically detecting when a single-ended clock is used, and disabling the quartz crystal amplifier and biasing circuit.

This design creates flexibility for how the device is used in the end application, but results in a few additional design requirements that need to be understood to ensure stable operation. This document discusses these requirements and serves as a guide on optimizing the oscillator clock circuit components.

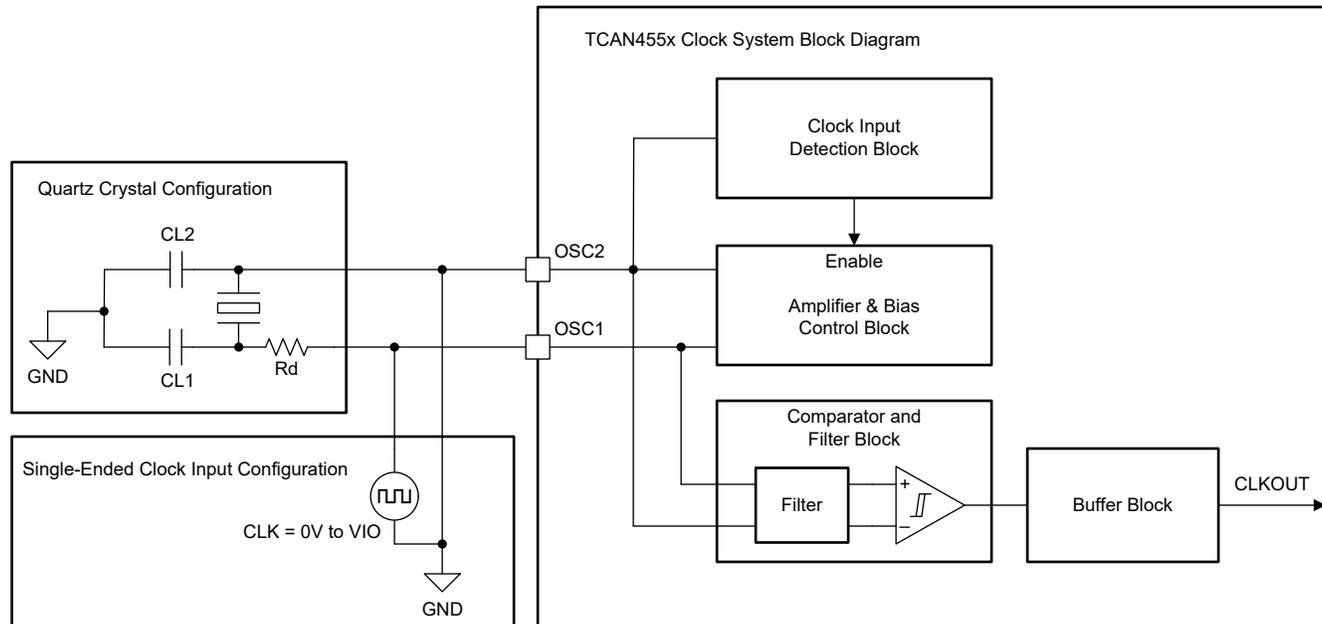


Figure 1-1. TCAN455x Clock Simplified Block Diagram

2 Crystal Oscillator Oscillation Concept

A crystal-based oscillator is formed by placing a crystal in the feedback loop of an oscillator circuit that provides sufficient gain and phase shift around the loop to start and sustain stable oscillations. A detailed explanation of crystal oscillator operation will not be covered here. However, to support the reader's interpretation of the guidance and recommendations contained in this application note, some essential aspects of the crystal oscillator circuit model are presented and explained here. A simple model of a crystal is shown in [Figure 2-1](#). The model has R-L-C series components, called motional resistance (R_m), motional capacitance (C_m), and motional inductance (L_m). The capacitor in parallel, C_0 , is called the shunt capacitance, and models the package capacitance. [Figure 2-2](#) illustrates a simple oscillator model, consisting of an inverting amplifier and crystal, and its equivalent circuit model.

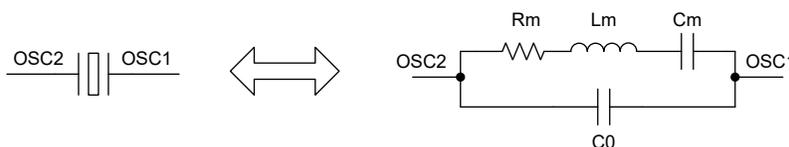


Figure 2-1. Oscillator Model

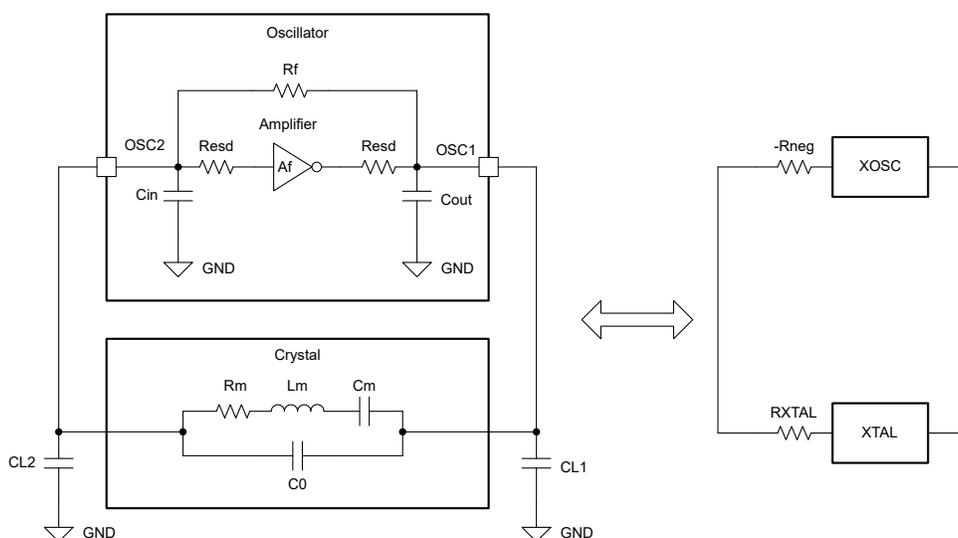


Figure 2-2. Crystal Oscillator Model

The circuit model in [Figure 2-2](#) is useful for understanding the necessary conditions for oscillation. These are:

$$X_{XTAL} + X_{OSC} = 0 \quad (1)$$

$$R_{XTAL} + R_{neg} = 0 \quad (2)$$

Where:

X_{XTAL} = the imaginary part of the impedance represented by the crystal.

R_{XTAL} = the real part of the impedance represented by the crystal.

X_{OSC} = the imaginary part of the impedance represented by the oscillator.

R_{neg} = the real part of the impedance represented by the oscillator.

Mathematically, R_{neg} is a *negative resistance*. It represents a circuit that supplies power rather than dissipating power, for example, an amplifier. Consequently, a simple interpretation is that the amplifier must have enough gain to compensate for the losses represented by the crystal and load capacitance. The concept of negative resistance is important to crystal oscillator design and will be revisited later in this app note.

3 TCAN455x Clock Structure

The TCAN455x clock circuit contains three main blocks, an Amplifier and Bias Control block, a Filter and Comparator block, and a Clock Input Detection block as shown in [Figure 1-1](#). A Comparator is used to compare the voltage difference between the OSC1 and OSC2 pins and generate the Clock Output signal used by the device when either a quartz crystal or single-ended clock input is used. The positive input of the comparator is connected to the OSC1 pin, and the negative input is connected to the OSC2 pin. When a single-ended clock is used, the clock signal is applied to the positive input of the comparator through the OSC1 pin, and the negative input of the comparator is held low by connecting the OSC2 pin to ground.

The Amplifier and Bias Control block provides the source current needed to start and sustain the crystal oscillation through the OSC1 pin when a quartz crystal is used, but it must be disabled when a single-ended clock input is used instead of a crystal. This is handled by the Clock Input Detection block that monitors the voltage level on the OSC2 pin and disables the Amplifier block if the voltage is below the detection threshold which is typically between $90mV$ to $150mV$, such as when the pin is connected to ground. If the OSC2 pin is not connected to ground, the current supplied by the Amplifier and Bias block through the crystal will ideally keep the minimum voltage level of the oscillation waveform above $400mV$ and includes a peak detector circuit that will sense the oscillation envelope formed by the voltage difference between the OSC1 and OSC2 pins.

The crystal oscillator transconductance amplifier adjusts the amplifier bias current to maintain a consistent and stable oscillation when the voltage amplitude of the OSC1 and OSC2 waveforms are nominally $1 V_{pp}$ for each of the individual OSC1 and OSC2 signals, or $2 V_{pp}$ between the differential OSC1 and OSC2 signal resulting from their 180° phase shift. However, the actual voltage levels will depend on the total load connected to the TCAN455x oscillator circuit.

When the total external load on the amplifier created by the reactance of the load capacitance and the crystal equivalent series resistance is too small, the amplifier's minimum output current may cause the oscillation voltage amplitude levels to become too large by allowing too much power to flow through the crystal. If the voltage amplitude on the OSC2 pin becomes too large, the minimum peak voltage level of the signal could drop below the single-ended clock input detection threshold causing the amplifier and bias block to become disabled and stop the oscillation. When the external load is configured properly, the amplifier will be able to adjust the bias current to maintain a smaller voltage amplitude level in the nominal range and ensure the single-ended clock detection circuit will not disable the amplifier and bias control block.

Establishing the proper balance in the oscillation circuit is critical to stable reliable operation, preventing mechanical damage to the crystal, and guarantee several other factors not previously discussed. Ensuring the frequency of oscillation and the gain in the transconductance amplifier has enough margin to create the negative resistance needed to reliably establish the crystal oscillation must also be considered when selecting the values of the components used in the circuit. The remainder of this document will discuss how to avoid unreliable operation and determine the proper component values needed to meet all parametric concerns through a combination of measurements and calculations.

Common schematic representations of the Basic Pierce Oscillator circuit are shown in the following figure with the key components identified.

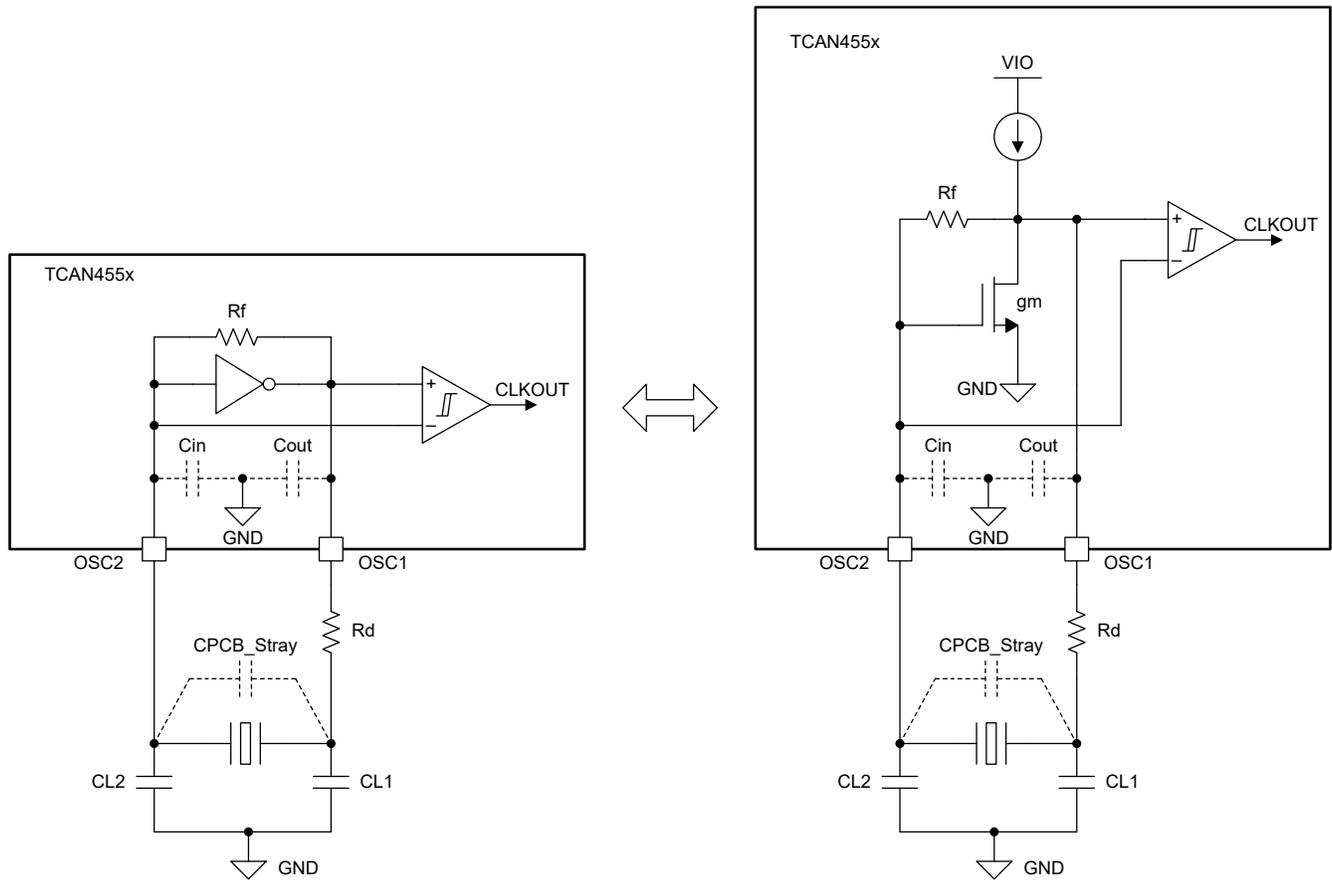


Figure 3-1. TCAN455x Pierce Oscillator Simplified Circuit Representations

4 Calculate the Load Capacitance

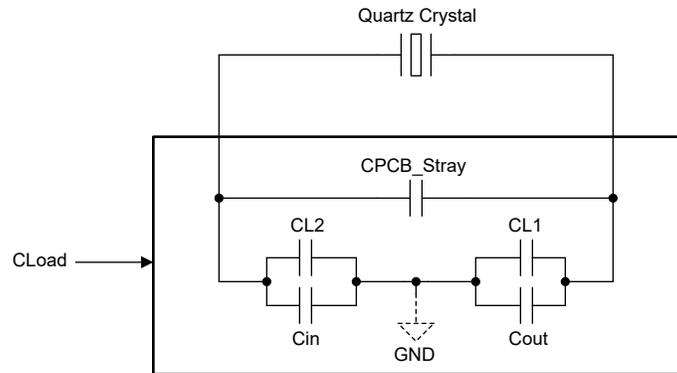


Figure 4-1. Crystal Load Capacitance

Without a TCAN455x device, crystal, and load capacitors mounted on the board, measure the parasitic capacitance between the crystal footprint pads. If series resistors are used, include those on the board when making the measurement. This becomes the PCB stray capacitance that will be used in calculations C_{PCB_Stray} .

The TCAN455x OSC1 Output Pin Capacitance C_{out} is typically **10 pF**

The TCAN455x OSC2 Input Pin Capacitance C_{in} is typically **9 pF**

Calculate the load capacitance presented to the crystal by the following formula:

$$C_{Load} = \left(\frac{[C_{in} + C_{L2}] \times [C_{L1} + C_{out}]}{[C_{in} + C_{L2} + C_{L1} + C_{out}]} \right) + C_{PCB_Stray} \quad (3)$$

Where the OSC1 pin capacitance C_{out} is in parallel with the C_{L1} external load capacitance since they are both with respect to ground on the amplifier output side of the crystal and therefore added together.

$$[C_{L1} + C_{out}] \quad (4)$$

Where the OSC2 pin capacitance C_{in} is in parallel with the C_{L2} external load capacitance since they are both with respect to ground on the amplifier input side of the crystal and therefore added together.

$$[C_{in} + C_{L2}] \quad (5)$$

Where the capacitance on both sides of the crystal are in series with each other relative to the crystal due to the common connection through the ground plane. Therefore they are calculated as capacitance in series.

$$\left(\frac{[C_{in} + C_{L2}] \times [C_{L1} + C_{out}]}{[C_{in} + C_{L2} + C_{L1} + C_{out}]} \right) \quad (6)$$

Where the parasitic capacitance of the PCB between the OSC1 and OSC2 pins is in parallel with the capacitance of the components and is therefore added to component capacitance.

$$C_{PCB_Stray} \quad (7)$$

Adjust the value of the external capacitors C_{L1} and C_{L2} to achieve a total load capacitance C_{Load} of the recommended value specified in the crystal data sheet.

5 Measure the Oscillation Frequency

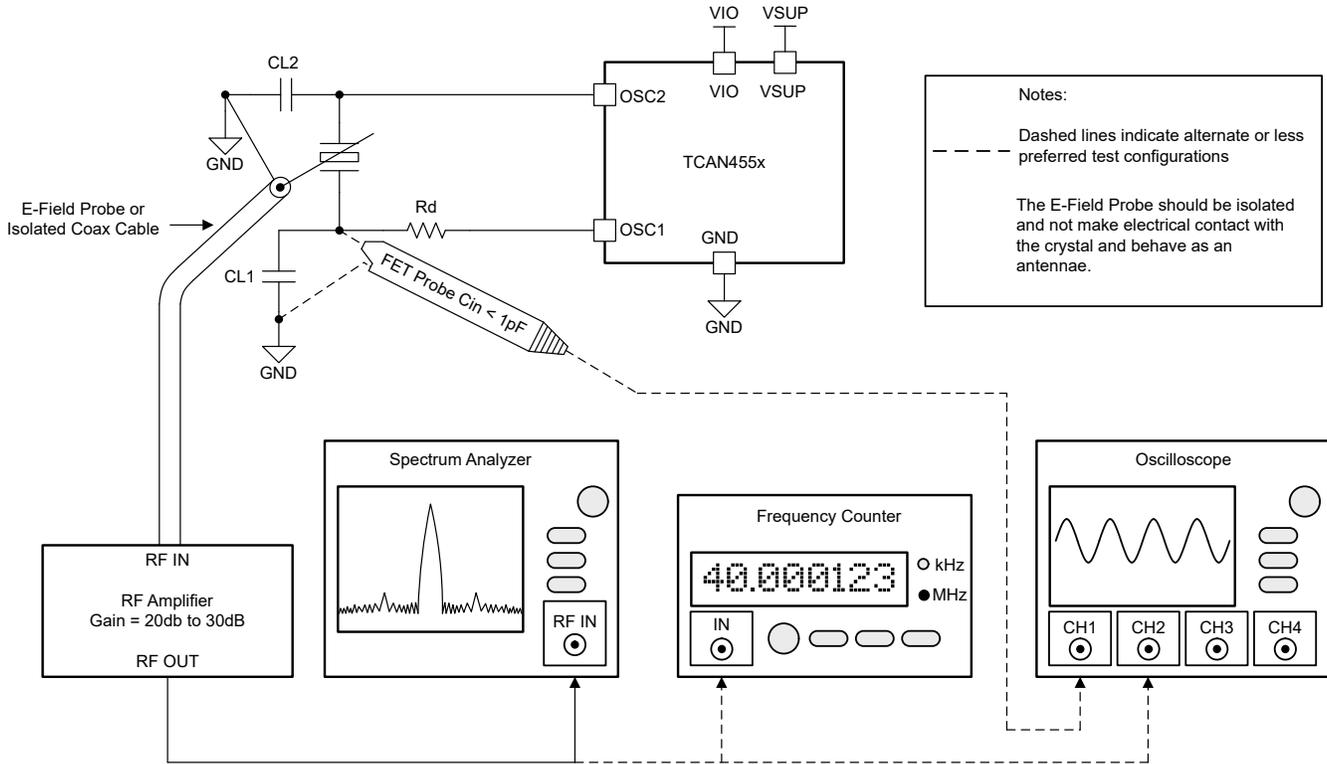


Figure 5-1. Oscillation Frequency Test Setup

Check for the motional parameters C_0 , C_m , resonant frequency (f_s) and ESR on the data sheet of the crystal manufacturer. Calculate the resonant frequency of the crystal and of the crystal with the load capacitance.

Where the resonant frequency and motional inductance of the crystal is:

$$f_s = \frac{1}{2\pi \times \sqrt{L_m \times C_m}} \rightarrow L_m = \frac{1}{4\pi^2 \times f_s^2 \times C_m} \quad (8)$$

Where the resonant frequency of the crystal and capacitive load is:

$$f_l = f_s \times \sqrt{1 + \frac{C_m}{C_0 + C_{Load}}} \quad (9)$$

Because the oscillator frequency is determined by load capacitance which is a product of the crystal's shunt capacitance C_0 , the crystal's Motional capacitance C_m , and the load capacitance of the board and external capacitors C_{Load} , it will shift according to the following formula:

$$\frac{dF}{F} = \frac{-C_m}{2(C_0 + C_{Load})} \quad (10)$$

Measure the oscillation frequency using an E-Field probe, sometimes called either a sniffer probe or antennae probe, connected to a RF Amplifier to strengthen the signal detected by the oscillation of the crystal, and a Spectrum Analyzer or Frequency Counter to display the frequency of the signal detected. This method does not place a direct load on the oscillation circuit that will alter the frequency of oscillation through additional resistance or capacitance inserted into the circuit by a directly connected voltage probe.

If an E-Field probe is not available, one can be made by exposing the conductor on one end of a coax cable that will act as an antenna, insulating it with heat shrink tubing to prevent electrical contact with any components on the board, and placing the insulated conductor directly on top of the crystal. The shield of the coax cable

should be electrically connected to a ground location near the crystal to improve the signal quality and provide a reference for the test equipment.

The signal detected will likely have low amplitude and may need to be amplified with an RF Amplifier for a more reliable measurement by the spectrum analyzer. The amplitude of the signal is not important and it simply needs to be large enough for the spectrum analyzer to measure the frequency.

Tune the spectrum analyzer with a center frequency at the nominal crystal frequency and with a fairly narrow span such as 100 kHz so that there is enough resolution to capture the oscillation signal and accurately measure the center frequency.

If a spectrum analyzer is not available, a High Resolution Frequency Counter with a minimum of 7 to 8 digits of precision may be used if the signal has enough amplitude and is free of enough noise to return an accurate frequency count.

An alternative measurement can be done with an oscilloscope through a very low capacitance and high impedance active probe. The probe will add an additional capacitive/resistive load on the circuit and will slightly alter the oscillation frequency. Less than 1pF of probe capacitance is needed to minimize the frequency shift caused by the probe.

Oscilloscope measurements may not have enough resolution to get a high precision measurement of the exact oscillation frequency. A more accurate measurement can be obtained by using a High Resolution Frequency Counter.

Verify the frequency of oscillation is within the required specification and adjust the external capacitors to shift the frequency if needed. Increasing the capacitance will lower the frequency, and likewise reducing the capacitors will increase the frequency.

Re-calculate the load capacitance if the external capacitor values have been adjusted.

6 Calculate the Load Resistance

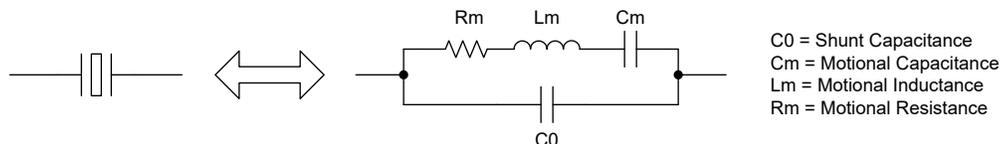


Figure 6-1. Quartz Crystal Electrical Model

Identify the crystal's shunt capacitance C_0 and motional resistance R_m from the crystal's data sheet or ask the crystal vendor if this is not specified.

Some crystal data sheets specify the R_m as the crystal's maximum Equivalent Series Resistance or ESR. Other crystal data sheets use the term ESR to specify the total load resistance under the specified Capacitive Load which is greater than the motional resistance of the crystal itself as defined in the next step.

Calculate the combined load of the series resistance in the crystal and the reactance of the capacitance placed on the oscillator circuit. This will be the total Load Resistance R_{Load} which is different than the crystal's motional resistance R_m . Both are sometimes referred to as the *ESR* and therefore there can be great confusion about what the term *ESR* is referring to. In calculations and for clarity the term *ESR* will not be used in this document. The crystal's motional resistance will be designated by R_m and the total Load resistance will be designated by R_{Load} .

$$R_{Load} = R_m \times \left(1 + \frac{C_0}{C_{Load}}\right)^2 \rightarrow R_m = \frac{R_{Load}}{\left[1 + \frac{C_0}{C_{Load}}\right]^2} \quad (11)$$

If the Motional Resistance R_m of the crystal is unknown, this can be approximated by using the maximum *ESR* listed in the data sheet (for example, 50 ohms), but this may not be accurate and is only a rough estimation that will cause the results to be larger than the actual or typical value (for example, 20 ohms).

7 Calculate the Negative Resistance

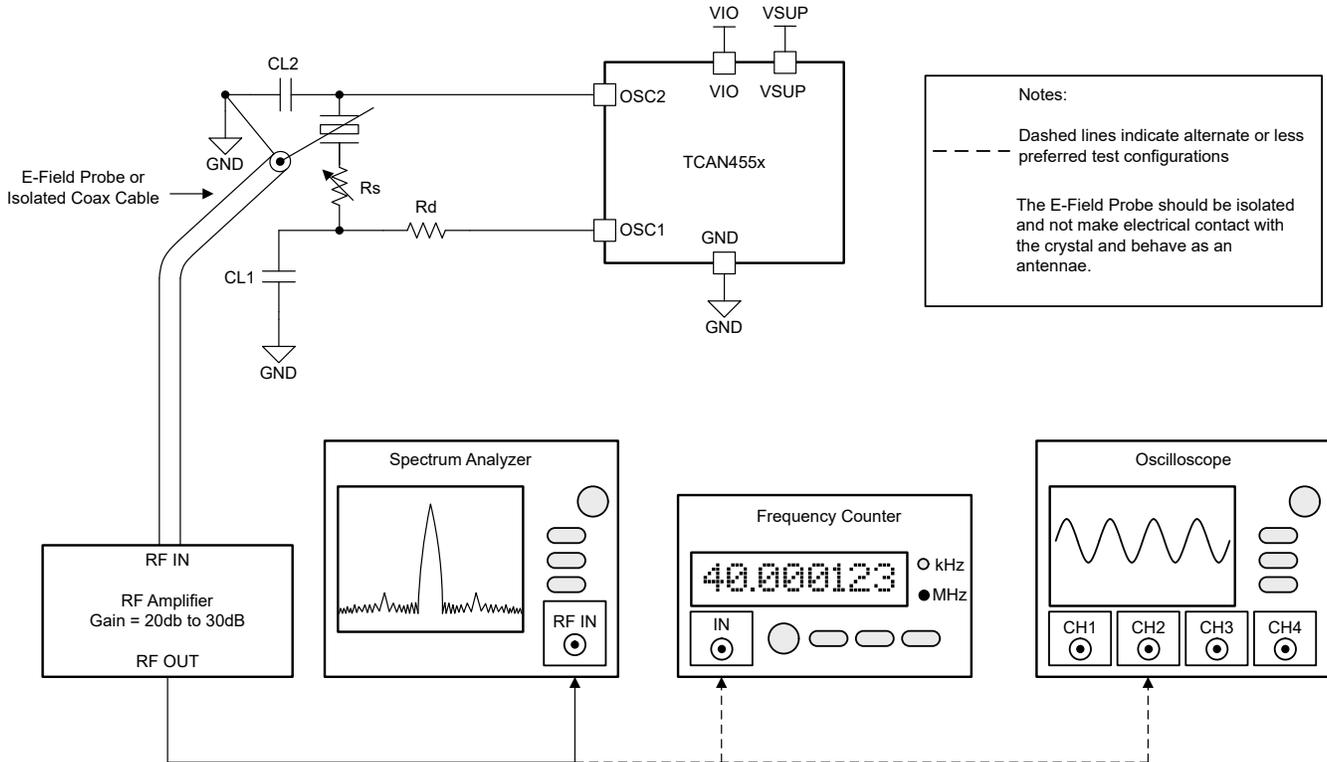


Figure 7-1. Negative Resistance Measurement Test Setup

The typical transconductance (g_m) of the TCAN455x Pierce Oscillator circuit is **6.6 mS**

Calculate the negative resistance by the following formula:

$$R_{neg_calc} = - \frac{g_m}{\omega^2 \times (2 \times C_{Load})^2} \quad (12)$$

Measure the negative resistance by inserting a series resistor (R_s) in between the crystal pin and the CL1 external load capacitor on the amplifier output (OSC1) side of the crystal. Monitor the crystal oscillation frequency and increase the resistor value until the oscillation stops. The total negative resistance is equal to the Load Resistance plus the added series resistance.

This requires the crystal to be removed from the PCB so that the resistor can be inserted, while maintaining the electrical connections with the other components with as little additional inductive, resistive, and capacitive impact as possible.

A cermet potentiometer, which is ceramic based and non-inductive, could be used instead of replacing the series resistors with discrete resistors of increasing value. However, the potentiometer chosen should have low capacitance so that the capacitive reactance does not alter the total load resistance and load capacitance of the circuit in a significant way. Once the oscillation stops, the resistance across the potentiometer can be measured.

The amount of negative resistance in the system can be calculated by the following formula:

$$|R_{neg}| = R_{Series} + R_{Load} \quad (13)$$

Compare the previously calculated negative resistance that was calculated with the typical transconductance value g_m , to the value calculated using the resistor measurement method. If the values do not match, adjustments may be needed to the transconductance (g_m), frequency (f_s), R_{Load} , or C_{Load} values. Check the R_{Load} and C_{Load} calculations for accuracy and solve for a more accurate transconductance value g_m .

It is important that there is enough negative resistance to overcome changes in the circuit as a result of component tolerance differences on key parameters and shifting values due to environmental conditions such as temperature and humidity. If there is not enough margin between the amount of negative resistance and the load resistance, there is a chance the oscillation in the circuit can stop or fail to start when power is applied to the circuit. Verify the magnitude of the negative resistance is 3 to 5 times larger than the Load Resistance by the following formula. This is commonly referred to as the Safety Factor.

$$R_{\text{Safety}} = \frac{|-R_{\text{neg}}|}{R_{\text{Load}}} \quad (14)$$

If the negative resistance margin is too low, the load resistance R_{Load} is too large for ensured safe operation of the oscillation circuit. The load capacitance may need to be adjusted by using larger external capacitor values in order to lower the total load resistance.

If the capacitors are adjusted to improve the negative resistance margin, the oscillation frequency will shift. Re-measure the oscillation frequency to ensure it is still within specification. Re-calculate the load capacitance and load resistance values that will be needed in other calculations.

If the external load capacitors cannot be adjusted to an appropriate level, then a crystal with more appropriate motional properties may be needed.

It is important to reduce the parasitic PCB capacitance $C_{\text{PCB_Stray}}$ as much as possible with proper layout techniques to allow greater margin and room for adjustment with different values of components.

8 Evaluate the Crystal for Margin

If a crystal with more appropriate motional properties is needed, it is possible to evaluate the compatibility of a crystal resonator with the oscillator based on the motional properties of the crystal.

The critical transconductance (gm_{crit}) is the minimum transconductance required by the oscillator to maintain a stable oscillation for a given crystal and load capacitance that can be calculated by the following formula:

$$gm_{\text{crit}} = 4 \times R_{\text{load}} \times \omega^2 \times (C_0 + C_L)^2 \quad (15)$$

$$\text{Where: } R_{\text{load}} = R_m \times (1 + (C_0 + C_{\text{Load}}))^2 \text{ and } \omega = 2\pi f \quad (16)$$

The gain margin ($\text{Gain}_{\text{margin}}$) can then be calculated by the following formula and the resulting ratio should be greater than 5 to ensure there is enough margin to start and maintain oscillation.

$$\text{Gain}_{\text{margin}} = \frac{gm}{gm_{\text{crit}}} \quad (17)$$

9 Calculate the Startup Time and Quality Factor

The ability of the crystal to sustain oscillation can be determined by the Quality Factor (Q) which is the ratio of the initial stored energy and the amount of energy lost in one radian cycle of oscillation. A higher Q factor will have less energy loss and longer sustained oscillation before the resonance dies out. Calculate the Quality factor (Q) by the following formula:

$$Q = \frac{2\pi \times F_s \times L_m}{R_m} \quad (18)$$

The time it takes the oscillations to start and stabilize is also of importance. Several factors such as the drive level, load resistance, and the magnitude of the closed loop gain can impact the startup time (τ) of the oscillations which can be calculated by the following formula:

$$\tau = \frac{2 \times L_m}{R_{\text{Load}} + R_{\text{neg}}} \quad (19)$$

10 Calculate the Drive Level

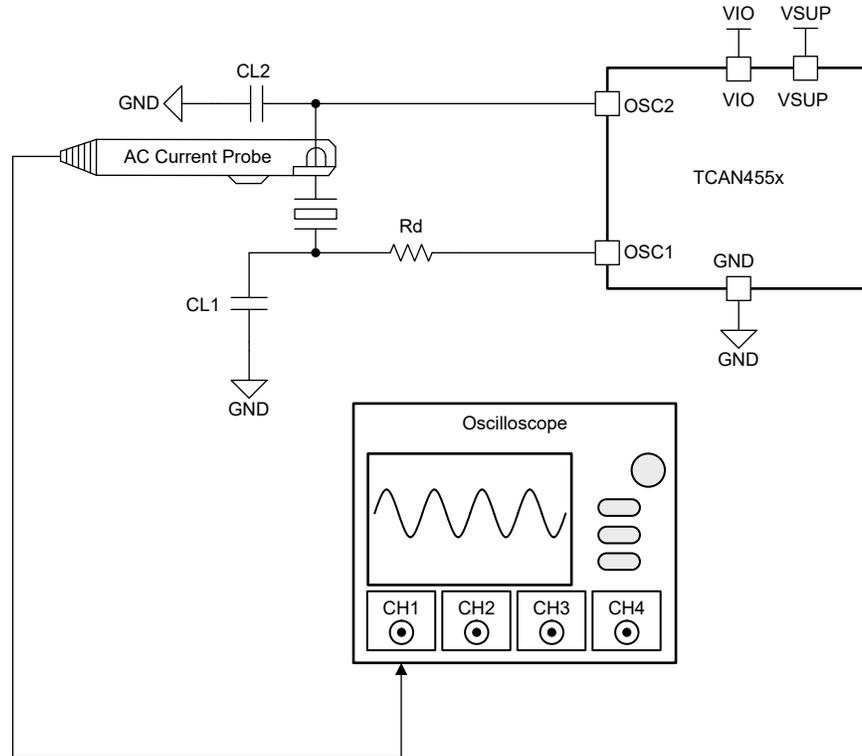


Figure 10-1. Drive Level Measurement Test Setup with Current Probe

The power dissipated in the crystal is called the drive level and will determine the amount of mechanical vibration inside the crystal. If the drive level, and mechanical vibrations, are too high, the crystal can suffer mechanical damage and cause it to fail or experience a shortened lifetime. The crystal data sheet typically specifies a maximum drive level in μW that should not be exceeded. It cannot be directly measured and must be calculated after determining the RMS current (I_{RMS}) through the crystal which can be obtained by several methods.

Method 1: Current Probe

Measure the RMS current (I_{RMS}) through the crystal using a current probe. This method provides the least external load on the oscillator circuit that would result in measurement error, but it requires board level modifications to accommodate the current probe.

Carefully remove the crystal from the board and insert a wire between the crystal pin and the PCB long enough to insert a current probe around the wire. Using a scope, measure the RMS current and or peak-to-peak current.

The RMS current can be calculated from the peak or peak-to-peak current by the following formula:

$$I_{\text{RMS}} = \frac{I_{\text{pk}}}{\sqrt{2}} = \frac{I_{\text{pk-pk}}}{2\sqrt{2}} \quad (20)$$

Calculate the Drive Level by the following formula:

$$D_L = I_{\text{RMS}}^2 \times R_{\text{Load}} \quad (21)$$

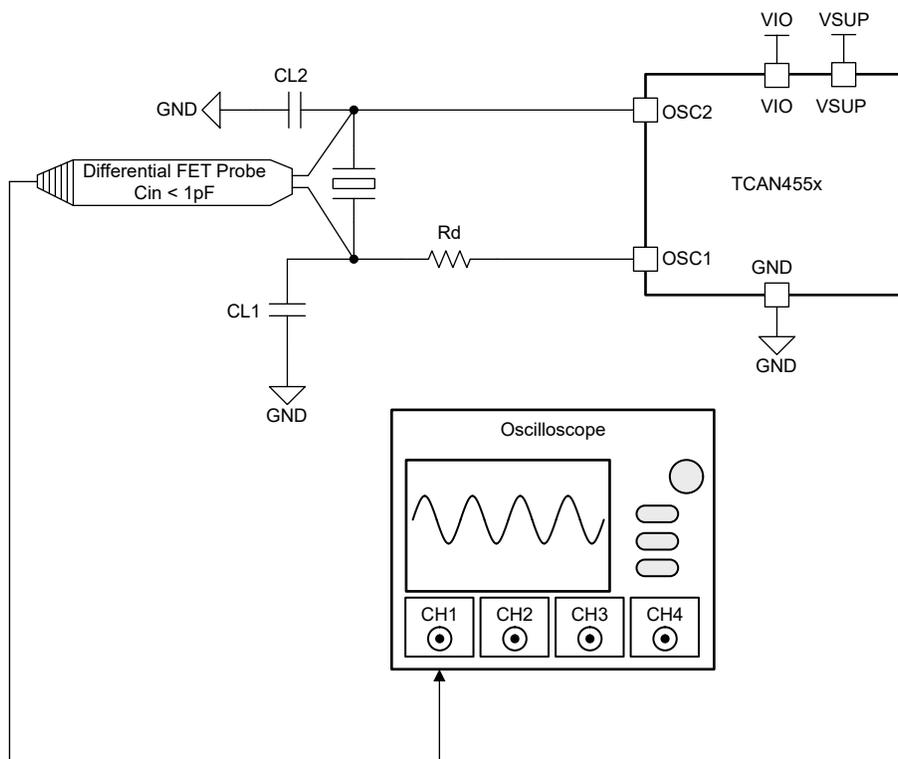


Figure 10-2. Drive Level Measurement Test Setup with Differential FET Probe

Method 2: Differential Active FET Probe

An alternative method is to calculate the I_{RMS} current by measuring the voltage swing across the crystal with a differential active FET probe that has less than 1pF of capacitance. The probe capacitance will need to be factored into the calculation because it will add error to the measurement.

Measure the RMS voltage or peak-to-peak voltage across the crystal.

The RMS voltage can be calculated from the peak-to-peak voltage by the following formula:

$$V_{RMS} = \frac{V_{pp}}{2\sqrt{2}} \quad (22)$$

The RMS current can be calculated from the RMS voltage by the following formula:

$$I_{RMS} = \frac{V_{RMS}}{R} = \frac{V_{RMS}}{X_c} = \frac{V_{RMS}}{\frac{1}{2\pi F C}} = 2\pi F \times V_{RMS} \times C_{total} \quad (23)$$

$$I_{RMS} = 2\pi F \times V_{RMS} \times C_{total} \quad (24)$$

$$\text{Where: } C_{total} = C_{Load} + C_0 + C_{probe} \quad (25)$$

The Drive Level (D_L) can then be calculated by the following formula:

$$D_L = \frac{(\pi \times F \times C_{total})^2 \times V_{pp}^2 \times R_{Load}}{2} \quad (26)$$

If the Drive Level exceeds the maximum level specified by the crystal manufacturer, the total load capacitance may need to be adjusted to reduce R_{Load} , or an external series dampening resistor (R_d) needs to be added between the amplifier output and the crystal + CL1 net.

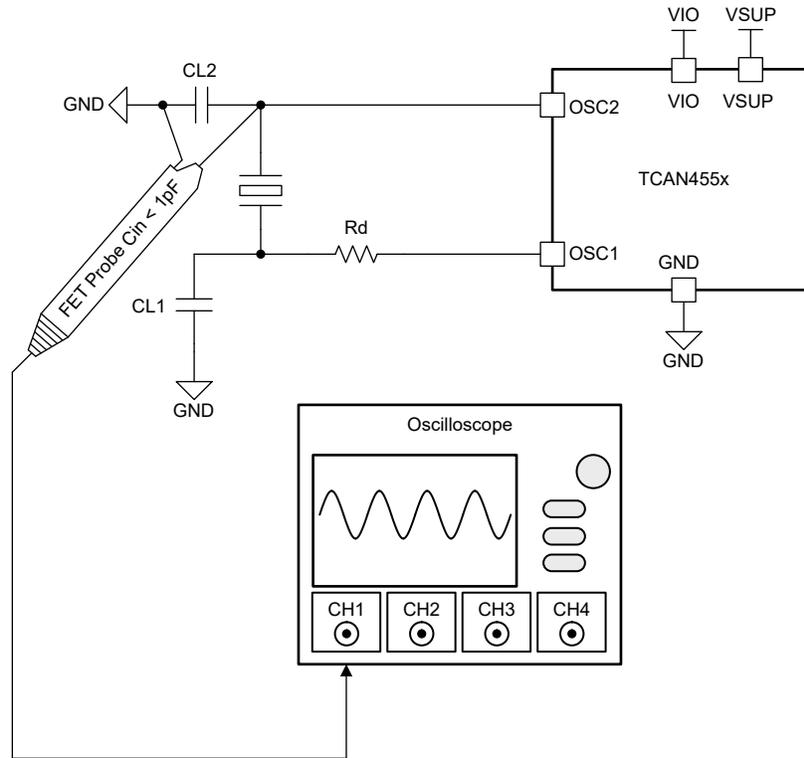


Figure 10-3. Drive Level Measurement Test Setup with Single-Ended FET Probe

Method 3: Single-ended Active FET Probe

Another alternative method is to calculate the I_{RMS} current by measuring the voltage swing at the input to the amplifier with an active FET probe that has less than 1pF of capacitance. The probe capacitance will need to be factored into the calculation because it will add error to the measurement. Measure the RMS voltage or peak-to-peak voltage across the CL2 capacitor on the amplifier input side of the crystal. The current flowing through this capacitor is approximately equal to the current flowing through the crystal with only a negligible amount flowing into the amplifier which can usually be neglected.

The RMS voltage can be calculated from the peak-to-peak voltage by the following formula:

$$V_{RMS} = \frac{V_{pp}}{2\sqrt{2}} \quad (27)$$

The RMS current can be calculated from the RMS voltage by the following formula:

$$I_{RMS} = \frac{V_{RMS}}{R} = \frac{V_{RMS}}{X_c} = \frac{V_{RMS}}{\frac{1}{2\pi F C}} = 2\pi F \times V_{RMS} \times C_{total} \quad (28)$$

$$I_{RMS} = 2\pi F \times V_{RMS} \times C_{total} \quad (29)$$

Where: $C_{total} = C_{L2} + \left(\frac{C_{PCB_Stray}}{2}\right) + C_{probe}$

The Drive Level can then be calculated by the following formula:

$$D_L = \frac{(\pi \times F \times C_{total})^2 \times V_{pp}^2 \times R_{Load}}{2} \quad (30)$$

If the drive level exceeds the maximum level specified by the crystal manufacturer, the total load capacitance may need to be adjusted to reduce R_{Load} , or an external series dampening resistor (R_d) needs to be added between the amplifier output and the crystal + CL1 net.

It is recommended to keep the load capacitance within the crystal manufacturer's recommendation. However with lower load capacitors, the OSC2 swing can be too close to ground. This could trigger the CLKIN detection

circuit that disables the oscillator and stops the oscillations. To avoid the CLKIN detection circuit disabling the oscillator, the load capacitance needs to increase resulting in lower drive levels as well, or a dampening resistor (R_d) needs to be added between the amplifier output and the crystal + CL1 net. This allows lower drive levels to be achieved without increasing the load capacitance beyond the recommended value.

11 Calculate the External Dampening Resistor

The dampening resistor R_d placed between the OSC1 pin of TCAN455x and the crystal along with the capacitor CL1 will help attenuate the V_{pp} level. The dampening series resistance R_d will limit the current and lower the voltage amplitude of the oscillation waveform by forming a voltage divider with the CL1 capacitor further reducing the power dissipated across the crystal and keeping the voltage on the OSC2 pin above the clock input detection threshold needed to prevent the Amplifier and Bias Control block from being disabled. The reactance of the CL1 capacitor can be calculated by following formula:

$$X_c = \frac{1}{(2\pi f C_{L1})} \quad (31)$$

In a typical application using FR-4 PCB material contributing 2-3 pF of stray parasitic capacitance, and a crystal with an 8 pF load capacitance specification, this resistance R_d is typically in the range of 50 to 100 ohms and CL1 as low as 1 pF or 2.2 pF should be sufficient to ensure that OSC2 pin swings above the clock input detection threshold.

This dampening series resistance will be added to the load resistance seen by the oscillator and reduce the negative resistance margin. Recalculate the negative resistance margin with this additional series resistance to determine if there is still enough safety margin and that the magnitude of the negative resistance is still 3 to 5 times greater than the load resistance + R_s with the following formula:

$$R_{neg} = \frac{g_m}{\omega^2 \times (2 \times C_{Load})^2} - R_d \quad (32)$$

Ensure that this does not exceed the negative resistance margin available. If the margin is too small, then the dampening series resistor may need to be reduced to a value that satisfies both the safety margin and drive level requirements. If this cannot be done, then larger load capacitors, a crystal with a lower motional resistance, and or a higher drive level specification must be used.

12 Recalculate Critical Transconductance and Gain Margin

If a series dampening resistor is used, the critical transconductance $g_{m_{crit}}$ and gain margin needs to be recalculated to ensure there is still enough gain margin to start and maintain oscillation.

$$g_{m_{crit_with_Rd}} = 4 \times (R_{load} + R_d) \times \omega^2 \times (C_0 + C_L)^2 \quad (33)$$

$$Gain_{margin_with_Rd} = \frac{g_m}{g_{m_{crit_with_Rd}}} \quad (34)$$

13 Verify and Check for Margin

Re-check the frequency, Drive Level and negative resistance if any components have been modified in the process and repeat until all requirements have been satisfied.

Calculate the temperature derating coefficient's impact on the circuit, including component tolerances of all resistors and capacitors in the circuit. Recalculate the values with the min/max and derated values.

Test the development board over the desired temperature and voltage range to verify there is no undesired behavior such as an excessive frequency shift, or the crystal fails to start or stops oscillating during operation. The parasitic capacitance is not typically stable across temperature and the total C_{Load} will tend to vary slightly with temperature.

If issues are detected, adjust the capacitance and series dampening resistance and re-evaluate the frequency, negative resistance, Drive Level, and voltage level parameters as necessary.

14 Summary

As described, the dual crystal oscillator and single-ended input clock structure of the TCAN455x poses additional design requirements with regards to the component selection used in this circuit. It is common to see a crystal oscillator circuit that contains only a crystal and two external load capacitors but does not contain a series damping resistor. Omitting the series dampening resistor R_d may or may not be acceptable and increases the risk of causing the clock to stop, fail to start, or overdrive the crystal with excessive power reducing its lifetime due to mechanical stress and increasing the oscillation V_{pp} amplitude to unacceptable levels.

Relying solely on external load capacitors large enough to keep the oscillation V_{pp} amplitude away from the single ended clock input detection threshold is possible, but this could result in a small frequency shift if the total load capacitance seen by the crystal exceeds its typical specification

Therefore, it is recommended to add a series damping resistor into the design to limit the oscillation V_{pp} amplitude without requiring excessive load capacitance. By adding this extra series resistor and taking the time to determine the proper value for all components in the circuit, many problems can be avoided resulting in a reliable and stable circuit design.

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