Application Note

Migrating From HDMI2.0 to HDMI2.1

David Liu

ABSTRACT

This document provides an overview of the migration from HDMI2.0 to HDMI2.1 specification. It also gives an introduction to TDP1204 and TMDS1204, Texas Instruments latest HDMI2.1 hydrid redriver.

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Trademarks

1 Introduction

HDMI2.0 was introduced in 2013. It features maximum bandwidth up to 18 Gbps that can support resolutions up to 4K@60Hz. But as display technology continues to advance, a new standard is needed. HDMI2.1, introduced in 2017, pushed the maximum bandwidth from 18 Gbps to 48 Gbps, while maintain backward compatibility with the existing HDMI specification. Below are some of the HDMI2.1 key features.

2 HDMI2.1 Key Features

2.1 Bandwidth

Most HDMI displays currently support the HDMI 2.0 standard, which has a bandwidth up to 18 Gbps. The 18 Gbps bandwidth can support an uncompressed 4k signal at 60 frames per second at up to eight-bit color. HDMI 2.1, with its 48 Gbps bandwith, adds support for an uncompressed 8k signal at 60 frames per second in 12-bit color. Using display stream compression (DSC), HDMI 2.1 can even push to 10K signal at 120 frames per second in 12- bit color.

Along with the increased bandwidth, it also introduces a new electrical mode of operation called Fixed Rate Link (FRL). With FRL, the existing TMDS data lane 0 to 2 are re-defined as FRL data lane 0 to 2. The TMDS clock lane are re-defined as FRL data lane 3. HDMI2.1 supports the following FRL rate and lane control.

- 3 Gbps on 3 lanes
- 6 Gbps on 3 lanes
- 6 Gbps on 4 lanes
- 8 Gbps on 4 lanes
- 10 Gbps on 4 lanes
- 12 Gbps on 4 lanes

Note when in the FRL 3 lanes operating mode, the FRL data lane 3 is not being used.

2.2 Dynamic HDR

Dynamic HDR can vary how each scene looks to better suit a particular scene. For example, a dark scene with bright highlights would take advantage of HDR differently than a bright scene with dark areas. If these two scenes were in the same movie, the static HDR would treat these the same,. Dynamic HDR would automatically adjust and let each scene looks at its best.

2.3 Auto Low-Latency Mode

A HDMI sink includes processing to smooth out motion and improve picture quality, but this process also introduces latency. HDMI2.1 specification introduces a new Auto Low Latency Mode (ALLM) feature. The ALLM allows a HDMI source to enable or disable a HDMI sink low-latency mode automatically without requiring an end user to navigate to the sink's menus and manually setting the optimal latency.

2.4 Variable Refresh Rate

Refresh rate is how many times a video panel refreshes per second. This is measured in hertz, and it is closely tied to the frame rate. When the HDMI source and sink are out of sync, you get an effect called “frame tearing”. It is caused by the HDMI sink trying to show more than one frame simultaneously when the source is not ready. Variable Refresh Rate (VRR) enables the source to display the image at the moment it is rendered for more fluid and better detailed video play, and for reducing or eliminating lag, stutter and "frame tearing".

2.5 Quick Frame Transport

Quick Frame Transport is another feature that works in conjunction with ALLM to deliver a more responsive video viewing experience. The feature prioritizes video frames in a bid to keep latency as low as possible.

If you want to take advantage of this feature, make sure any intermediary devices, like a surround sound receiver, are also compatible. This ensures all of your devices work together to deliver a smooth, responsive experience.

2.6 Quick Media Switching

In the past, when playing video contents that have different refresh rate, there was a short blackout as the HDMI sink needs to re-sync its refresh rate when different video content is switching. The Quick Media Switching (QMS) eliminates the blackout caused by refresh rate changes and allows the end user to watch content with differing refresh rates back-to-back without the blackout.

2.7 Enhanced Audio Return Channel

Audio Return Channel (ARC) allows you to send audio over HDMI to your audio receiver without an additional optical audio cable. Enhanced Audio Return Channel(eARC) takes advantage of the additional bandwidth that is available in HDMI 2.1 specification. The eARC is able to carry uncompressed 5.1, 7.1, and high bit rate or object based audio at up to 192 kHz in 24-bit resolution.

3 TDP1204 and TMDS1204

With the introduction of the HDMI2.1 specification, the maximum data rate per lane has been increased to 12 Gbps. The signal condition or the quality of the lane becomes paramount in order to deliver a smooth and rich video and audio experience for the consumer. With any multi-gigabit signal, the signal integrity starts to degrade from transmission line insertion loss, crosstalk, inter-symbol interference, noise, and reflections as the data rate increases.

To compensate these signal integrity degradations, Texas Instruments introduces two redrivers for HDMI2.1, TDP1204 and TMDS1204. Both TDP1204 and TMDS1204 are HDMI 2.1 redrivers supporting data rates up to 12 Gbps per lan. They are backwards compatible for HDMI 1.4b and HDMI 2.0b. The high-speed differential inputs and outputs can either be AC-coupled or DC-coupled, which qualifies the TDP1204 and TMDS1204 to be used as a DP++ (AC-coupled) to HDMI level shifter or HDMI (DC-coupled) to HDMI redriver. The TDP1204 can support both 3 and 4 lane HDMI 2.1 FRL at 3, 6, 8, 10, and 12-Gbps.

Both TDP1204 and TMDS1204 are hybrid redrivers, which means they can operate either as linear or limited redriver. Both source and sink applications can be supported with this hybrid redriver approach.

When configured as a limited redriver, the TDP1204 and TMDS1204 differential output voltage levels are independent of the graphics process unit (GPU) output levels, ensuring HDMI specification compliant levels at the HDMI receptacle. The limited redriver mode is recommended for HDMI source applications.

When configured as a linear redriver, the TDP1204 and TMDS1204 differential output levels are a linear function of the GPU output levels, enabling the redriver to be transparent to the link training and operate as a channel shortener. Linear redriver mode is recommended for HDMI sink applications.

Table 3-1 highlights the major features difference between the TDP1204 and TMDS1204. It is up to the system design requirement when choosing between TDP1204 and TMDS1204.

Table 3-1. TDP1204 and TMDS1204 Feature Comparison

Features	TDP1204	TMDS1204
Fan-out buffer to separate HDMI1.4/2.0 clock and HDMI2.1 data lane 3	No	Yes
SIGDET_OUT signal detect output	No	Yes
DDC level shifter (5 V to 1.2 V/1.8 V/3.3 V)	Yes	No
DC gain adjustment from the pin strap mode	No	Yes

3.1 TMDS1204 Fan-Out Buffer

In some applications a HDMI sink requires the clock and data must be on separate paths. The TMDS1204 implements a fan-out buffer feature to support such applications. When the fan-out buffer feature is enabled, the TMDS1204 will output the HDMI clock on RCLKOUTp/n when operating in HDMI 1.4 or HDMI 2.0. The OUT_CLKp/n will be disabled. When operating in HDMI 2.1 FRL mode, the TMDS1204 will output FRL data lane 3 on OUT_CLKp/n. RCLKOUTp/n will be disabled.

3.2 TMDS 1204 SIGDET_OUT

The TMDS1204 provides an input signal detect function as part of the power management feature. When standby is enabled and swap is disabled, the TMDS1204 looks for a signal on either IN_CLK (if HDMI 1.4 or 2.0) or IN_D2 (if HDMI 2.1). When standby is enabled and swap is enabled, the TMDS1204 looks for a signal on either IN_CLK (if HDMI 2.1) or IN_D2 (if HDMI 1.4 or 2.0). The TMDS1204 is fully functional when a signal is detected. If no signal is detected, then the device re-enters standby state waiting for a signal again. In the standby state, all of the TMDS outputs are in high-Z status.

When standby state is enabled, the TMDS1204 will assert the SIGDET_OUT pin low when the signal is detected on IN_CLK or IN_D2. Otherwise SIGDET_OUT pin is de-asserted when entering power down or standby state.

3.3 TMDS1204 DC Gain Adjustment

The TMDS1204 equalizer is used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. The TMDS1204 provides three sets of CTLE curves with each curve having 16 AC gain settings and 3 DC gain settings. For the DC gain, the TMDS1204 provides a globally lane control feature through the DCGAIN pin in pin strapping mode.

3.4 TDP1204 DDC Buffer

The TDP1204 has a DDC buffer for HDMI capacitance isolation and for shifting 5-V levels present on the HDMI connector to as low as 1.2-V levels on the GPU source side. The HV_DDC_SDA and HV_DDC_SCL pins support 5-V levels while the LV_DDC_SDA and LV_DDC_SCL pins can support 1.2-V, 1.8-V, and 3.3-V levels.

Note that the TMDS1204 does not provide the DDC buffer function. If level shifting is required, then an external DDC level shifter must be implemented.

4 Summary

This application note provides a quick overview of the difference between HDMI2.0 and HDMI2.1. It also highlights the key difference between TDP1204 and TMDS1204. For more detail information, see the HDMI2.1 specification and the TDP1204 and the TMDS1204 data sheets (listed in Section 5).

5 References

- *TDP1204 12-Gbps, DC/AC-Coupled to HDMI™ 2.1 Level Shifter Hybrid Redriver Data Sheet*
- *TMDS1204 12-Gbps, DC or AC-Coupled to TMDS® and FRL HDMI™ Hybrid Redriver Data Sheet*

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