

TMDS_CLOCK/FRL_Data Detection Design in HDMI® Sink Applications TMDS1204



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ABSTRACT

Texas Instruments [TMDS Clock Detection Solution in HDMI® Sink Applications TS3USB3031, SN65LVDS4, SN65LVDS17](#), application note presented a method for High-Definition Multimedia Interface (HDMI®) sink applications such as digital TVs, monitors, and other display equipment to wake up from standby or sleep mode by detecting Transition-Minimized Differential Signaling (TMDS) clock in HDMI applications. But with the latest HDMI2.1 Fixed Rate Link, with the TMDS clock lane being re-purposed as FRL data lane, a new detection method is needed.

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1 Waking Up an HDMI Sink Device

HDMI is a de facto interface standard in consumer electronics and the most successful and easiest video and audio connector in the industry. Most digital TVs, monitors, and video display equipment have one or more HDMI ports. Video source equipment such as set-top boxes, gaming consoles, Blu-ray Disk™ players, notebooks, and mobile video sources support HDMI as well. HDMI supports a supplemental specification, Consumer Electronics Control (CEC), to control the HDMI source and sink in HDMI-connected equipment. CEC provides the same ‘language’ between the HDMI equipment allowing users to easily control them. Figure 1-1 shows the high-level HDMI 1.4/2.0 interconnection, including a CEC line.

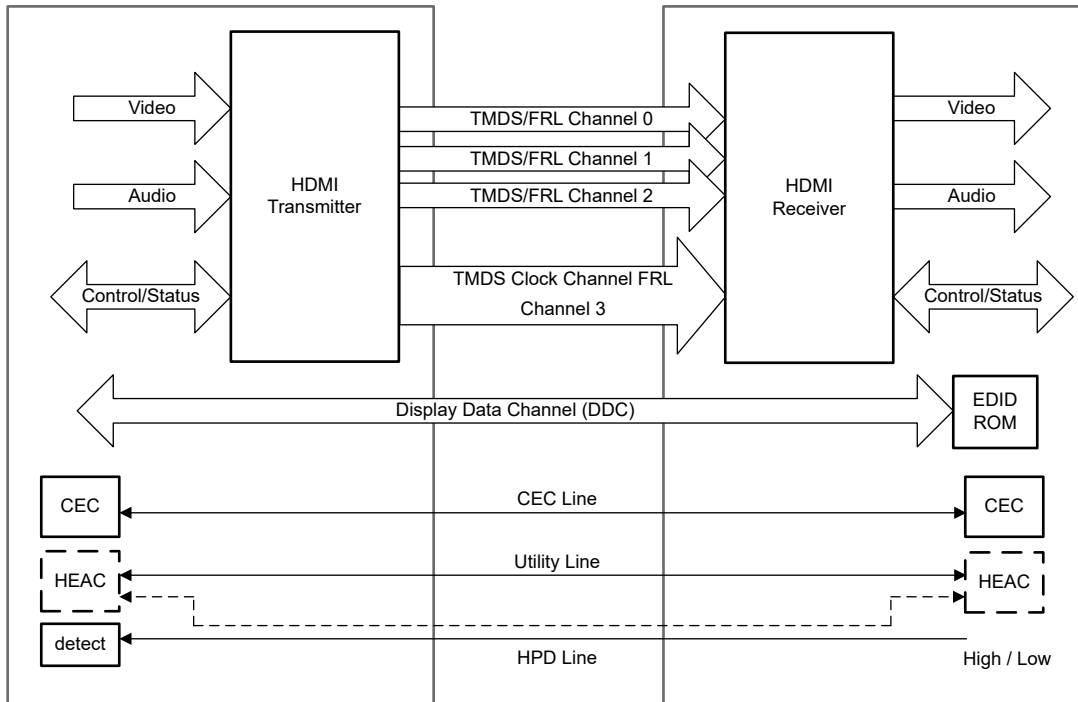


Figure 1-1. HDMI High-Level Block Diagram

CEC is one of the 19 HDMI connector pins and CEC has an electrical and protocol specification. A number of different messages and operation code (opcode) are used for the best user experience so that users can use only one remote controller to control both HDMI source and HDMI sink devices. For instance, if an HDMI source and sink are in standby mode and the user wants to wake up both of them, the following power-on function code can be used to switch on the HDMI devices by pressing the power button on the remote controller. This can wake up both the HDMI source and sink devices. More advanced user-controlled CEC messages are available, refer to the CEC specification in HDMI 2.0, or older version specifications.

1.1 Reasons for Wake Up Failure

Although CEC is provided for the control of the HDMI devices, its implementation and operation is not that simple. It is common that HDMI sink users experience the HDMI source is not controllable through a single remote controller as expected, and vice versa. This is because many HDMI sources and sinks do not support CEC, including a few very well-known HDMI source devices and thus there is no simple way to control both the HDMI source and sink devices at once. There are also a number of HDMI devices supporting CEC, but require complicated steps to enable the feature in the equipment. Not as common are some devices that implement vendor-specific codes preventing HDMI source and sink devices from communicating.

2 Communicating Without CEC

The [TMDS Clock Detection Solution in HDMI® Sink Applications TS3USB3031, SN65LVDS4, SN65LVDS17](#), application note provides examples for making the HDMI1.4/2.0 sink device detect Transition Minimized Differential Signaling (TMDS) clock or signal from an HDMI1.4/2.0 source device so that the HDMI sink can wake up from its standby state by turning on the HDMI source with a single remote controller. The HDMI transmitter source detects receiver terminations in HDMI sink. If the HDMI receiver enables the termination resistors, then the transmitter can determine the 3.3-V terminated level and that the receiver is connected and functioning.

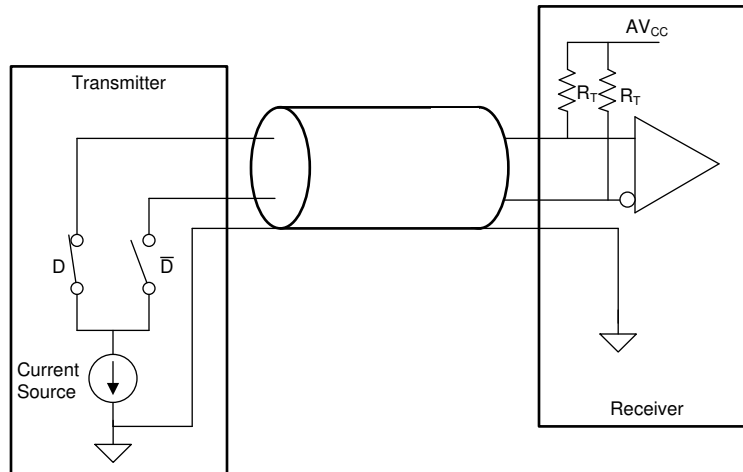


Figure 2-1. TMDS/FRL Differential Pair Conceptual Schematic

HDMI2.1 introduces a new electrical mode of operation called Fixed Rate Link (FRL). With FRL, the existing TMDS data lane 0 to 2 are re-defined as FRL data lane 0 to 2. The TMDS clock lane are re-purposed as FRL data lane 3. HDMI2.1 supports the following FRL rate and lane control.

- 3Gbps on 3 lanes
- 6Gbps on 3 lanes
- 6Gbps on 4 lanes
- 8Gbps on 4 lanes
- 10Gbps on 4 lanes
- 12Gbps on 4 lanes

Note, when in the FRL 3 lanes operating mode, the FRL data lane 3 is not being used.

With the TMDS clock lane being re-purposed as FRL data lane 3, the clock detection methodology being presented in [TMDS Clock Detection Solution in HDMI® Sink Applications TS3USB3031, SN65LVDS4, SN65LVDS17](#) application note is no longer applicable and a new detection methodology is needed for HDMI2.1.

3 HDMI1.4/2.0/2.1 Detection Methodology

TI's TMDS1204 is a HDMI2.1 Hybrid Redriver capable of supporting data rates up to 12Gbps. TMDS1204 is backwards compatible for HDMI 1.4b and HDMI 2.0b. The TMDS1204 is a hybrid redriver supporting both source and sink applications. A hybrid redriver can operate either in a linear or limited redriver function.

The TMDS1204 has a SIGDET_OUT open drain output. When TMDS1204 Standby mode is enabled and Swap function is disabled, the TMDS1204 looks for a signal on either IN_CLK (if HDMI 1.4 or 2.0) or IN_D2 (if HDMI 2.1). When the Standby mode is enabled and the Swap function is enabled, the TMDS1204 looks for a signal on either IN_CLK (if HDMI 2.1) or IN_D2 (if HDMI 1.4 or 2.0).

When standby state is enabled, the TMDS1204 can assert the SIGDET_OUT pin low whenever the TMDS1204 exits the standby state and can de-assert SIGDET_OUT pin when entering power down or standby state.

The SIGDET_OUT pin can then be used to drive an MCU. Once the wake-up signal is detected, then the MCU wakes up the video processor and the video processor can enable RTerm in HDMI Rx for normal operation.

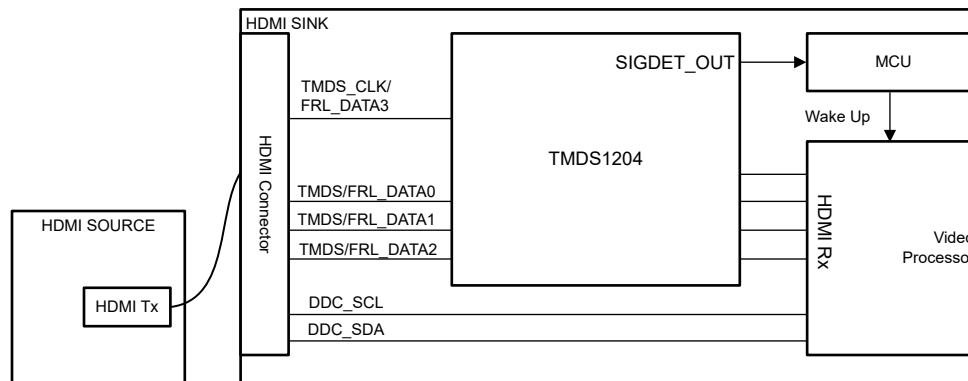


Figure 3-1. TMDS1204 Implementation Example Block Diagram

Please note, this detection scheme does not limit to HDMI2.1, the detection scheme also be used for HDMI1.4 and 2.0.

4 Summary

With the usage of TMDS1204 SIGDET_OUT pin, this presents a simpler clock and signal detection circuitry implementation design for HDMI1.4, 2.0, and 2.1. The HDMI/FRL source can determine HDMI/FRL sink receiver termination and transmit clock and signal when the user activates the source from the standby mode, and eventually the HDMI/FRL sink can detect TMDS clock or FRL signal running and wake up the system without any control.

5 References

- Texas Instruments, [TMDS Clock Detection Solution in HDMI® Sink Applications TS3USB3031, SN65LVDS4, SN65LVDS17](#), application note.

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