

# ***High Speed Clock Distribution Design Techniques for CDC 509/516/2509/2510/2516***

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*APPLICATION REPORT: SLMA003A*

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September 1998*



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## Abstract

The memory bandwidth of high performance microprocessors is increasing at a rapid rate and the future memory bandwidth requirements are expected to keep increasing. The bandwidth requirements of RAM will be satisfied in the near term by using Synchronous DRAM. The need to drive multiple DRAM chips at high speeds with low skew necessitates the use of clock distribution devices with Phase Locked Loop (PLL) technology.

To meet the designer's need for high-performance clock system components, Texas Instruments has developed PLL Clock Drivers that push the clock speeds up to 125 MHz. The focus of this application note will be on Clock Distribution chips specifically designed for use with Synchronous DRAMs. The clock driver series designed for buffered SDRAM applications includes CDC509, CDC516, CDC2509, CDC2510 and CDC2516. Some of the advanced features offered by these chips include:

- Phase-Lock Loop Clock Distribution for Synchronous DRAM applications
- Distributes one clock to multiple outputs in a banked mode
- External Feedback (FBIN) pin is used to Synchronize the Outputs to the Clock Input
- No External RC Network Required
- Operates at 3.3-V Vcc
- Packaged in Plastic Thin Shrink Small-Outline Package
- Series or parallel termination options



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## Introduction

The memory bandwidth of high performance microprocessors is increasing at a rapid rate and the future memory bandwidth requirements are expected to keep increasing. The bandwidth requirements of RAM will be satisfied in the near term by using Synchronous DRAM. The need to drive multiple DRAM chips at high speeds with low skew necessitates the use of clock distribution devices with Phase Locked Loop (PLL) technology.

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The designer has the option of using either CDC2xxx or CDC5xx series of clock drivers. The CDC2509 provide the same functions as the CDC509, but also include series-damping resistors to improve signal integrity without increasing component count, see Figure 1. The CDC516 is a scaled version of the CDC509, with the CDC516 having sixteen outputs instead of nine, see Figure 2. Though these chips were designed for SDRAM applications, the designer should not limit the scope to which these chips can be used.

## Clock Terminology

**Peak-to-Peak-Jitter (Period Jitter)**, is defined as the upper and lower bounds of a distribution of a large number of samples of cycle-to-cycle period measurements from ideal. In reference to a PLL, the period jitter is the worst case period deviation from ideal that would ever occur on the output of the PLL.

**Output Skew -  $t_{sk(o)}$** , is the difference between two concurrent propagation delay times that originate from a single input, or multiple inputs switching simultaneously and terminating at different outputs.

**Board Skew -  $t_{sk(pcb)}$** , is introduced into the clock system by unequal trace lengths and loads. It is independent of the skew generated by the clock driver. It is important to keep line lengths equal to minimize board skew.

**Electrical Length**, is the distance a signal or clock travels in a specified length of time in a specified media.

**Early Clock**, is a clock generated by a phase locked loop whose phase is leading that of the input to the PLL. The output clock is generated before the input clock arrives.

**Late Clock**, is a clock generated by a phase locked loop whose phase is lagging that of the input to the PLL. The output clock is generated after the input clock arrives.

**Static Phase Error -  $t_{ph(in-fb)}$** , is the static phase offset of the reference input clock and the feedback input to the PLL.

**Period Jitter (Cycle-to-Cycle)**, is the difference in the period of successive cycles of a continuous clock pulse.

**Accumulated Phase Error**, is the static phase error plus (or minus) the cycle to cycle jitter across n cycles.

## Basic Operation

A clock distribution chip consists of a Phase Locked Loop (PLL) system that is buffered to one or more outputs. The output clocks are controlled in banks with “1G” and “2G” enabling each bank as shown in Figure 1 below.

The PLL is a closed loop system designed so that there is nominally zero phase error between CLK and FBIN. Phase compensation is achieved by adjusting the propagation delay in the feedback line. The feedback line is a microstrip or stripline trace that connects the FBOUT to the FBIN. The propagation delay is a function of the velocity of propagation and the microstrip or stripline trace length.

Figure 1. CDC509/2509 Functional Block Diagram

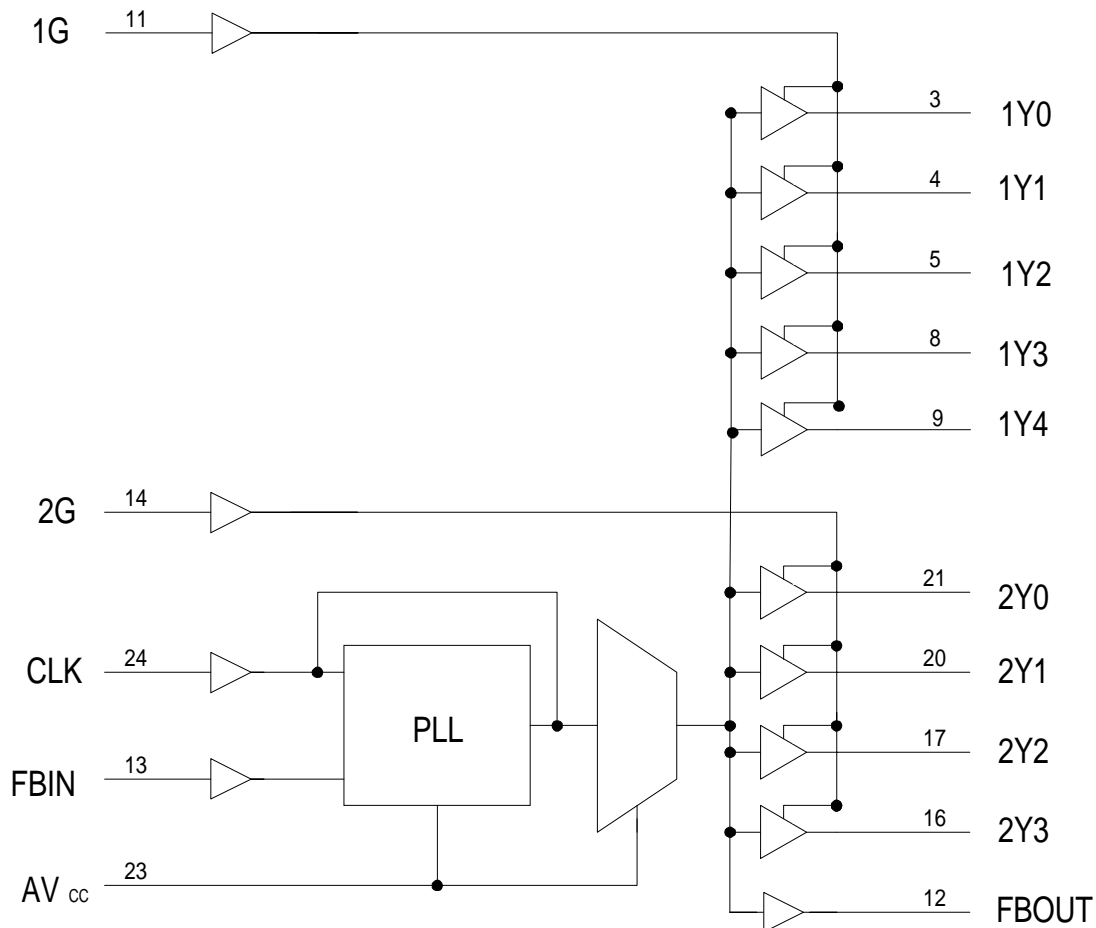
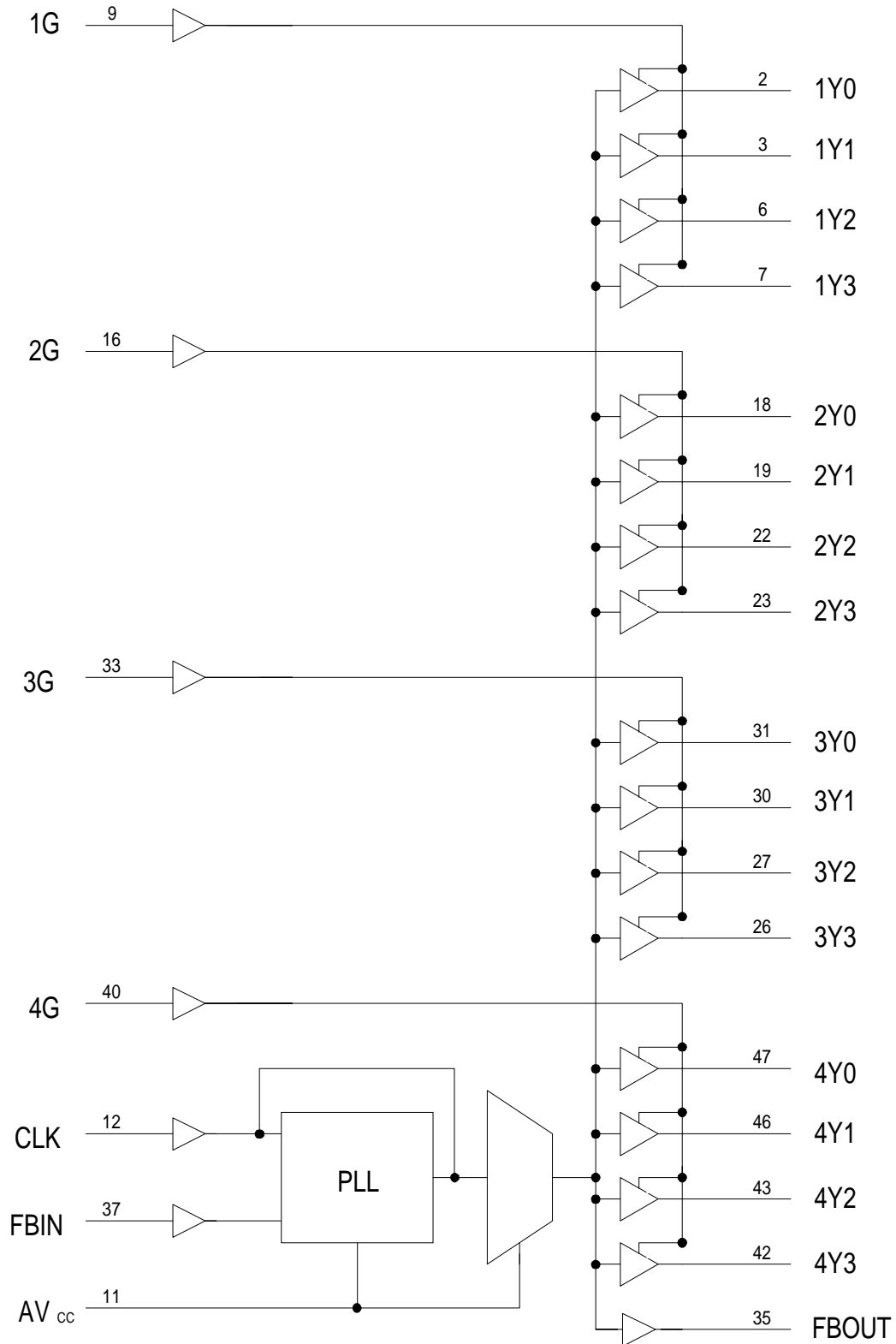


Figure 2. CDC516 Functional Block Diagram



## Operating Modes

The CDC2509 has many modes of operation which aid the designer in trouble shooting, reducing power consumption and minimizing EMI. On the CDC2509 banked operation is achieved by using 1G and 2G to enable or disable banks 1Y and 2Y respectively. If a bank is disabled (1G or 2G is logic low) then the output clock is pulled to a low state as shown in Figure 3. A summary of all normal modes of operation is given in Table 1. The enable/disable feature provides a method of disabling all or part of the clock output without the need for PLL restoration. Thus, the designer can maintain signal integrity and still can use on/off operation as a measure for reducing power consumption and radiated emissions.

Additionally, the designer can disable the PLL by taking AVCC to ground. This places the chip in a bypass test mode. In this mode, the input clock is buffered directly to the output. Therefore, the output clock will be only be delayed by the output buffer. By disabling and enabling the PLL, the designer can compare the characteristics of the PLL. This will aid the designer in evaluating jitter characteristics and phase differences created by the PLL.

Figure 3. CDC509/2509 Device Configurations

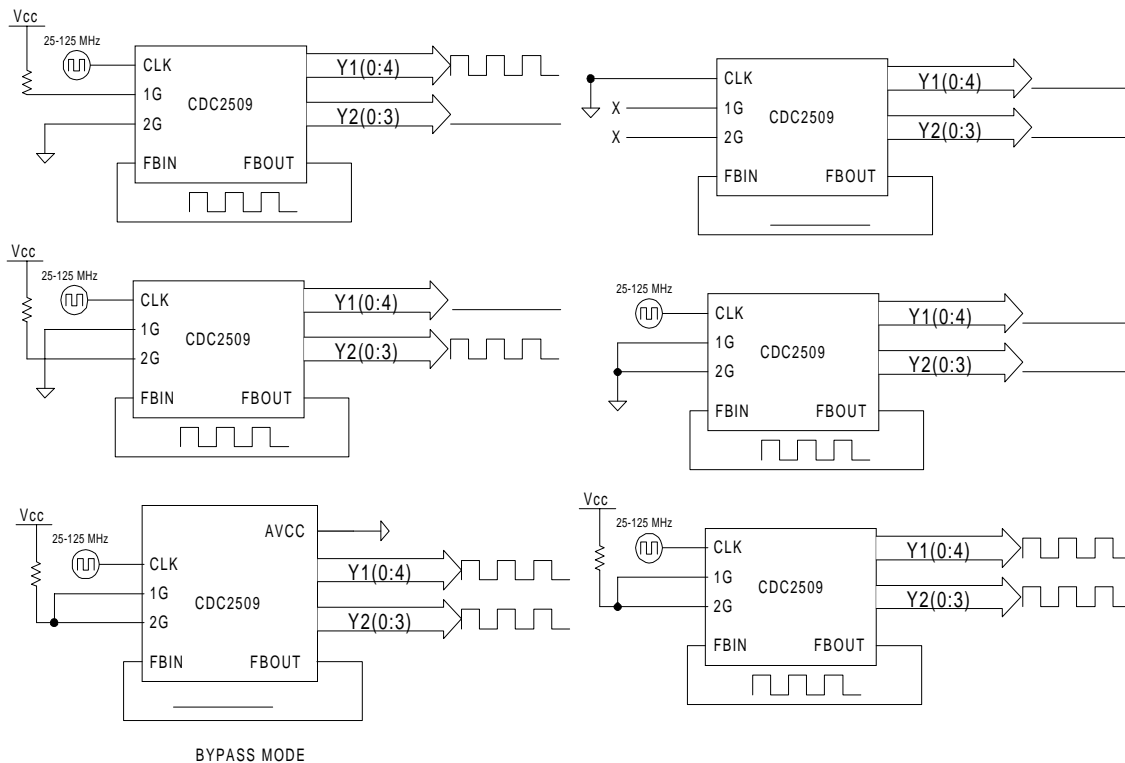


Table 1. Mode Summary

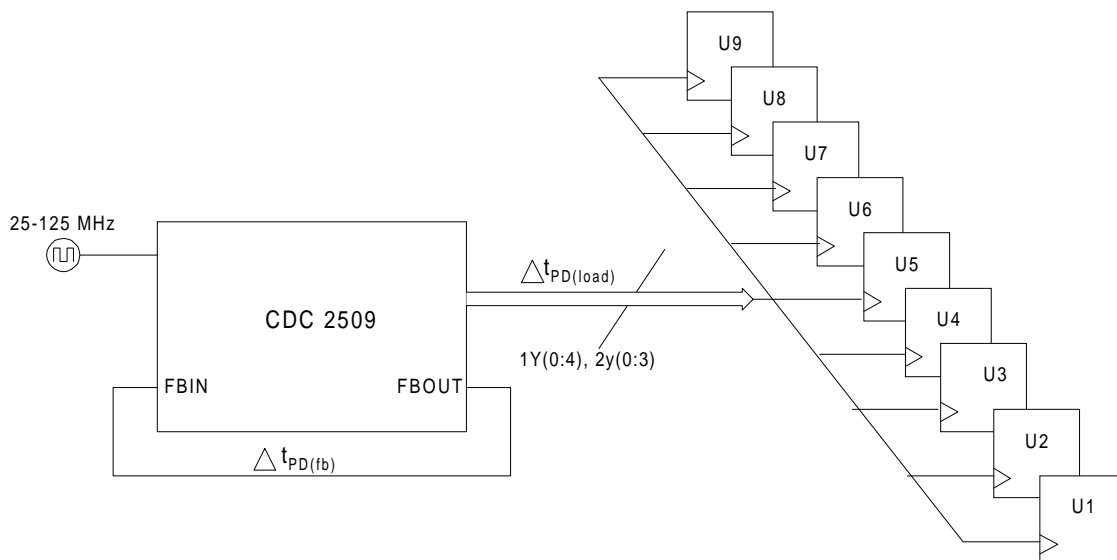
INPUTS			OUTPUTS		
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

## Zero Delay Buffer

A typical SDRAM application configured as a zero delay buffer is shown in Figure 4. The PLL of the CDC2509 generates an early clock that results in the clock edge arriving at the loads at the same time that the clock arrives at the clock buffer input. This is achieved by matching the propagation delay of the output to load ( $t_{PD(Load)}$ ) with the propagation delay of the feedback line ( $t_{PD(FB)}$ ). This effectively compensates for the propagation delay through the output PC board traces.

To ensure that each load is clocked at the same time, the designer should route output clock traces with matched lengths. Additionally, clock signal quality can be ensured by matching and controlling trace impedance and loading. Typically, each output is capable of driving five loads or a total capacitance of 30pF.

Figure 4. PC DRAM Configuration





## Power Supply Considerations

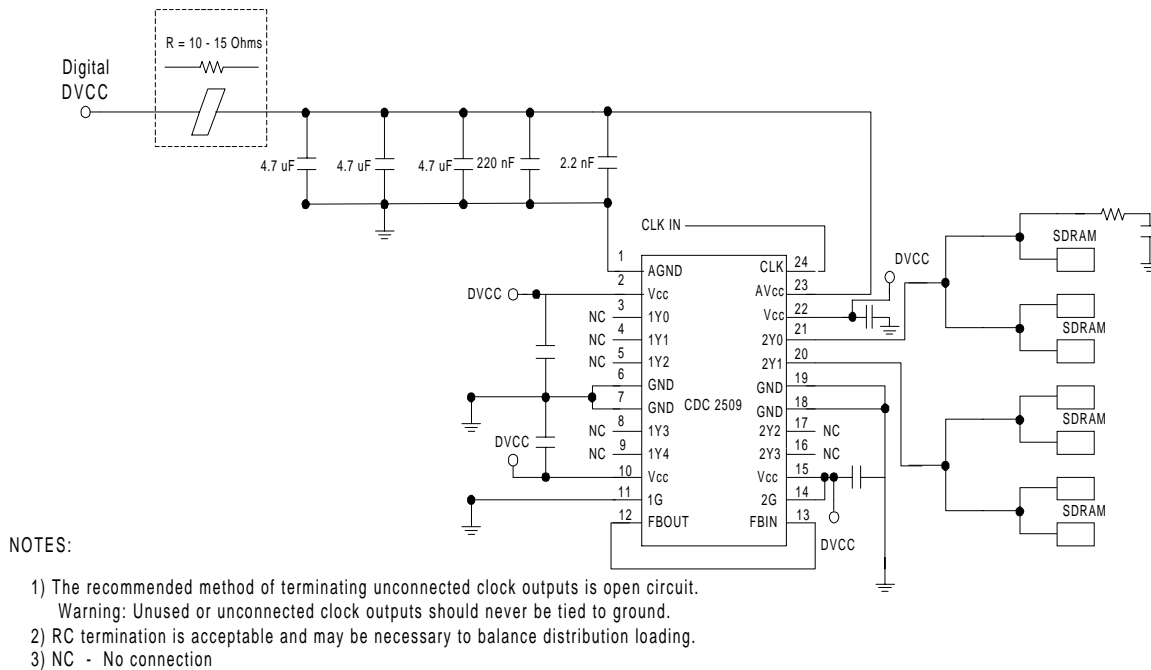
The CDC509, CDC516, CDC2509, CDC2510 and CDC2516 family of clock drivers uses a precision integrated analog PLL that is sensitive to noise on the analog power and ground pins. Noise on the analog supply line can significantly increase the output jitter and the total system skew margin. For best performance results, a filter network as shown in Figure 5 should be utilized.

The filter may be designed using an inductor, ferrite bead or a resistor as a noise mismatch component. The designer should choose the approach that meets the application jitter tolerance and cost compromise. For best results, all components should be placed as close as possible to the pins of the device. To maximize RF decoupling, the use of surface mount components is recommended. Choose capacitors with low parasitic inductance and keep lead lengths as short as possible.

## Output Termination

To avoid poor clock transmission quality, it is necessary to use effective line termination techniques. The correct method of terminating an output clock is dependent on the specific application. If multiple loads are to be driven off the same clock output then an RC termination may be necessary to balance output loading. If the output clock is not used, then the output can be left either unterminated or RC terminated as shown in Figure 5. The unterminated approach does not affect performance and is recommended because of lower power consumption and a lower component count.

Figure 5. Typical Application Circuit







## Board Layout Considerations for Signal Integrity and EMI

The following are general guidelines for proper clock buffer layout and usage. These suggestions may help the designer reduce radiated and conducted emissions and improve signal quality. This list is not entirely inclusive and it is up to the designer to research those techniques that will be most beneficial to the design.

- Match consistent impedance of signal lines by using either a power or a ground plane to form a (micro)strip line.
- Do not route traces closer to the edge of the PCB board than 3 times the height above the image plane (or 3 x layer thickness).
- Face the power plane with its return ground plane and have no signal trace layers in between.
- Maintain impedance control for all clock traces. Calculate impedance for both microstrip and stripline. Minimize impedance mismatches by reducing the number vias and connectors. If an impedance mismatch is necessary, keep the mismatch as close to the clock source as possible.
- Be aware of differences in propagation delays of signal traces routed through microstrips versus those routed through striplines. Microstrip allows for fastest transition of signal edges while permitting greater amounts of RF energy to be radiated. Stripline provides more shielding but transition times are slower.
- Calculate capacitive loading of all components and properly compensate with a series resistor and/or end termination.
- Decouple clock components (VCC) with capacitors having a self-resonant frequency (that frequency above which the capacitor looks resistive) higher than the clock harmonics requiring suppression. Place capacitors near the clock chip and avoid long trace lengths.
- Minimize or eliminate use of vias to route clock traces. Vias add inductance to the trace. Vias could change the trace impedance causing reflections of EMI emissions.
- Do not locate clock signals near I/O areas.
- Keep trace impedance as balanced as possible and keep traces as short as possible to minimize reflections, ringing, and creation of RF common mode currents.



- ❑ Route clock traces on one routing plane only. This layer must be adjacent to a solid (image) plane at all times. If possible, route all clock traces using stripline.
- ❑ If possible, create localized ground and VCC planes on the top layer of the PCB. The localized ground plane can reside beneath the chip while the VCC plane can surround the chip. Tie the ground and VCC planes to their respective main plane. These localized planes will provide a path for RF currents to return to the ground plane via the localized planes to its respective reference plane at many points.

## Typical Characteristics Curves CDC509/CDC516

Figure 6. Phase Error vs. Clock Frequency

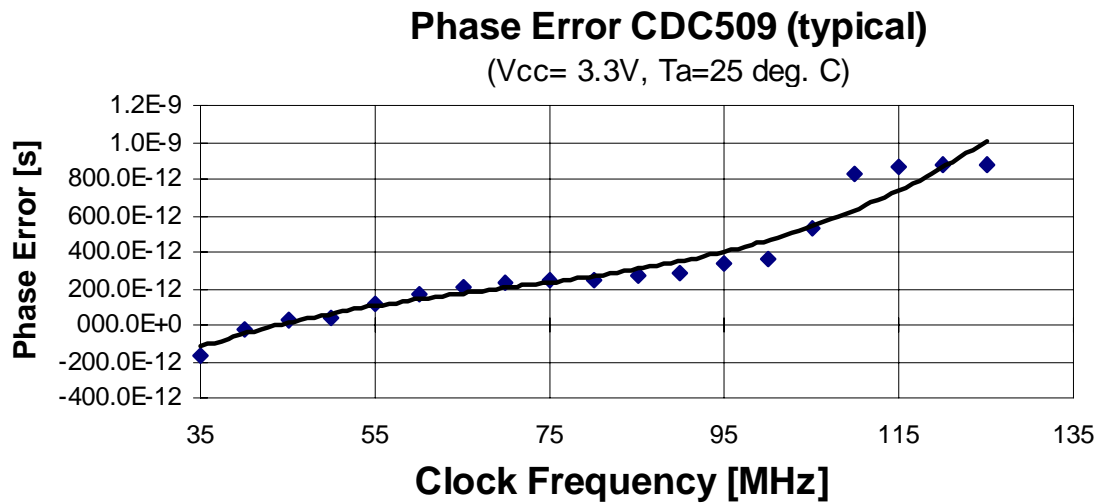


Figure 7. Duty Cycle vs. Clock Frequency

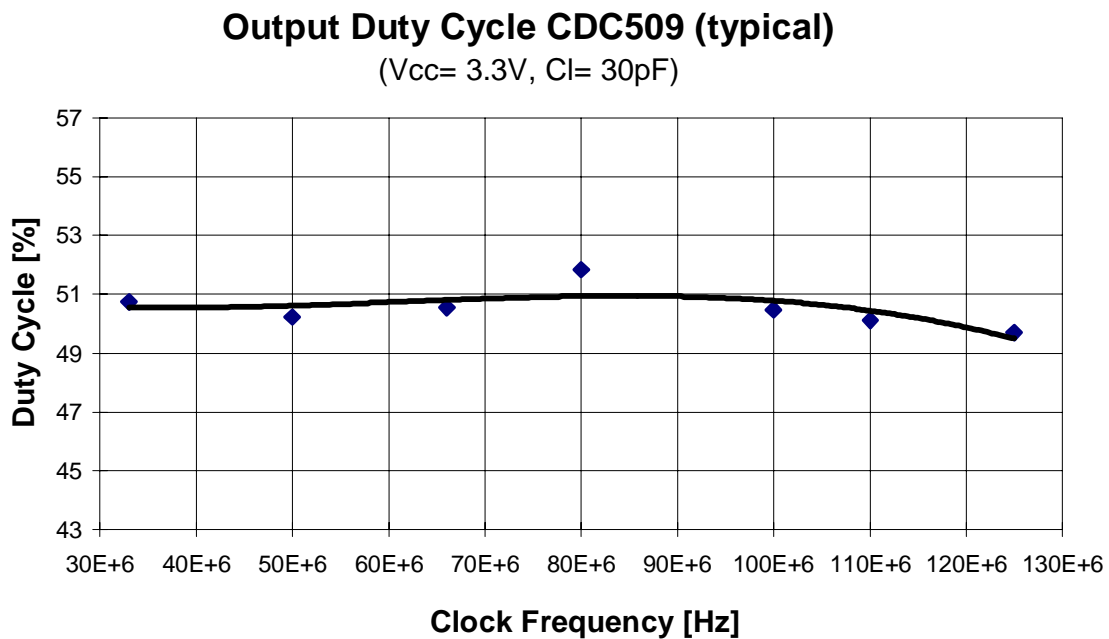


Figure 8. Analog ICC vs. Clock Frequency

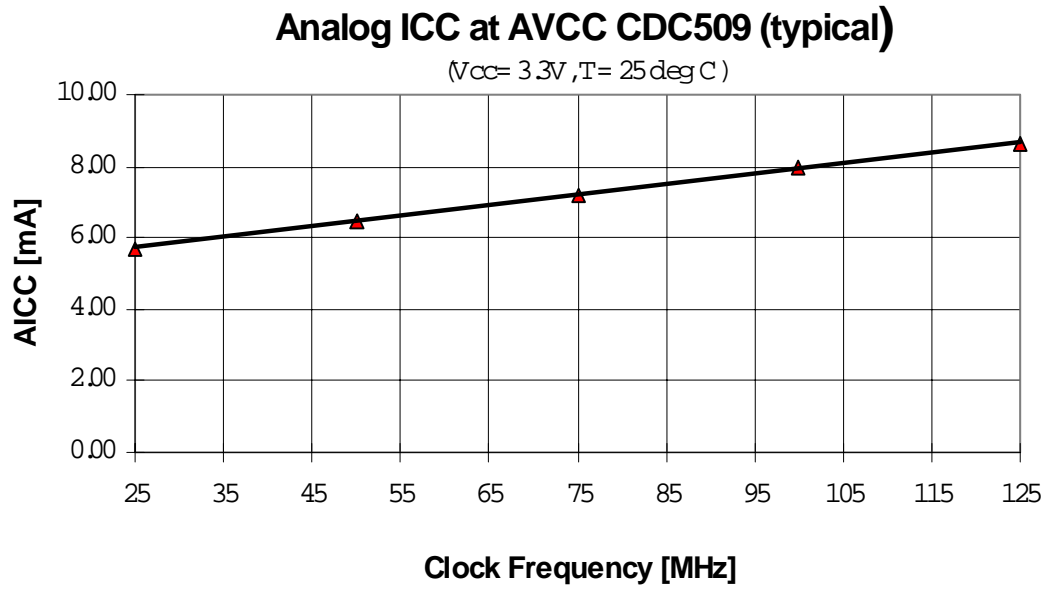


Figure 9. Phase Error vs. Clock Frequency

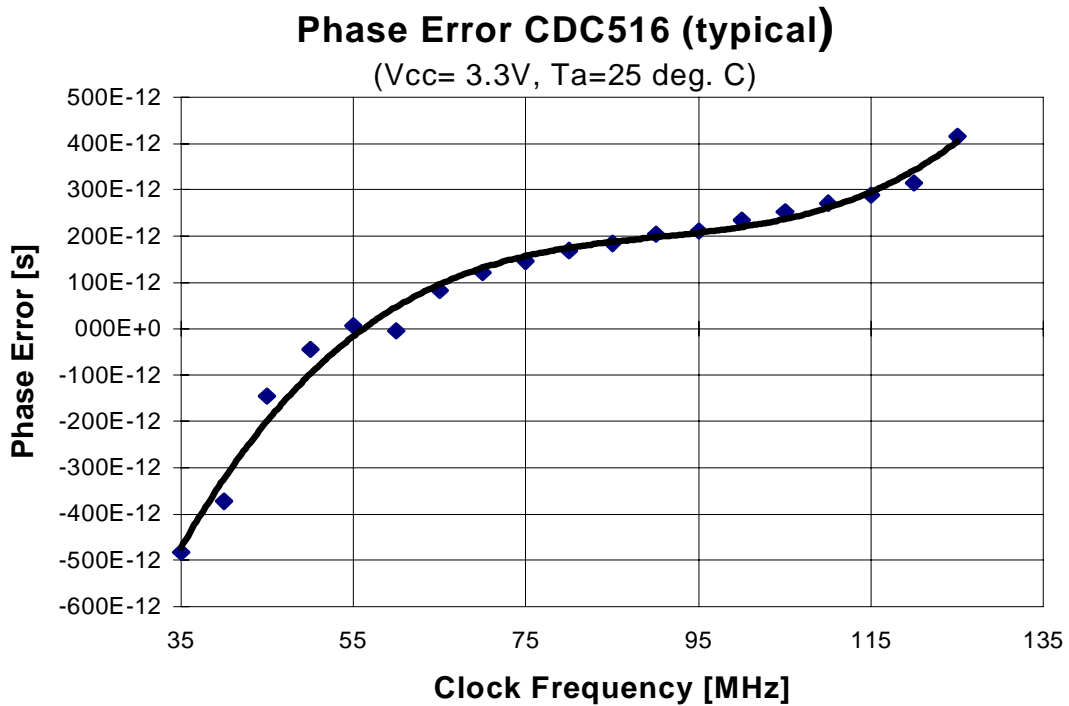


Figure 10. Duty Cycle vs. Clock Frequency

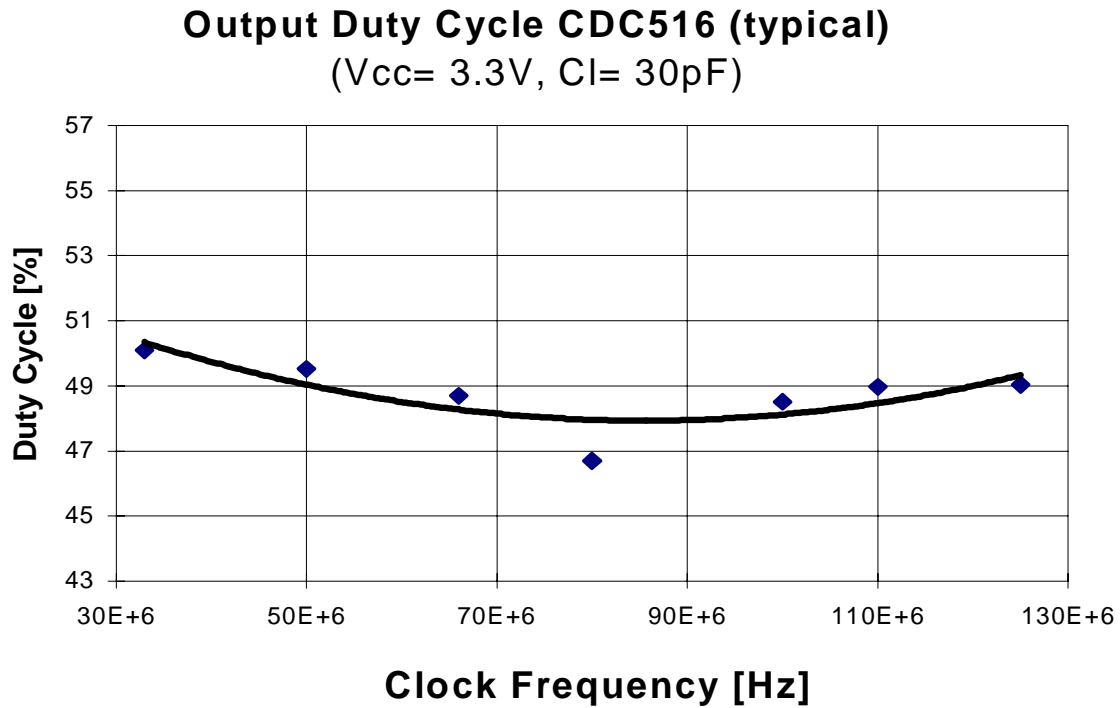


Figure 11. Analog ICC vs. Clock Frequency

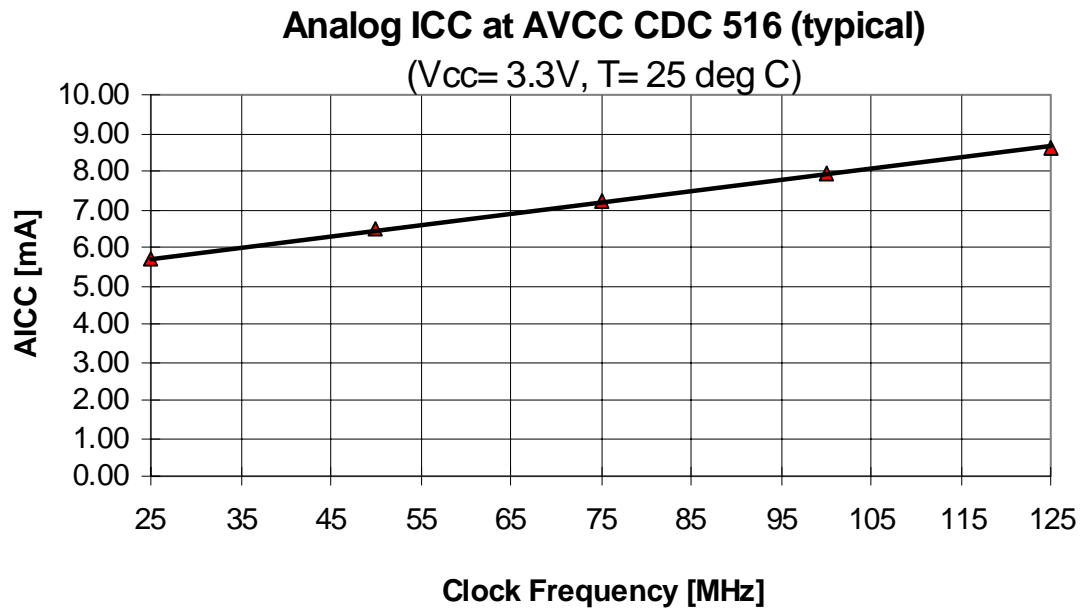


Figure 12. Dynamic ICC vs. Clock Frequency

