

## **DC Parameters: Input Offset Voltage ( $V_{IO}$ )**

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### **ABSTRACT**

The input offset voltage,  $V_{IO}$ , is a common dc parameter in operational amplifier (op amp) specifications. This report aims to familiarize the engineer by discussing the basics and modern aspects of  $V_{IO}$  by providing a definition and a detailed explanation of causes of  $V_{IO}$  for BJT, BiFET, and CMOS devices. Discussion centers around measurement techniques, data sheet specifications, and the effect of  $V_{IO}$  on circuit design and the trim methods to correct it.

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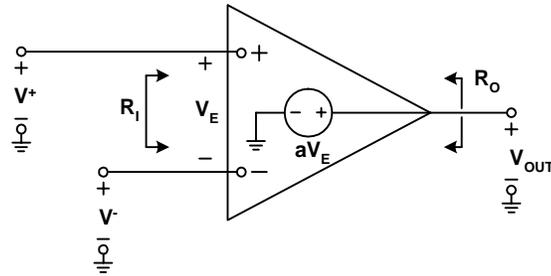
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## 1 Introduction

Op amps find extensive use in a wide variety of circuits, and their appropriate specification for a particular application requires knowledge of relevant data-sheet parameters. Data sheet specifications are divided into two general categories: dc parameters and ac parameters. The dc parameters represent internal errors that occur as a result of mismatches between devices and components inside the op amp. These errors are always present from the time the power is turned on (i.e., before, during and after any input signal is applied), and they determine how precisely the output matches the ideal op-amp model. Thus the precision of the op amp is determined by the magnitude of the dc errors.

The objective of this report is to provide the information necessary for the designer to understand each parameter; what it is, what causes it, and how it is measured, trimmed and specified.

Figure 1 presents an ideal op amp together with a table of ideal parameters. The general assumptions listed in the table simplify design analysis and provide a good, first order approximation that is reasonable when the op amp limits are not being pushed. Most applications, however, utilize the op amp to the fullest extent for one or more parameters and require more detailed analysis. It is then that the nonideal, or real, op amp of Figure 2 must be used. See *Understanding Basic Analog—Ideal Op Amps*, (SLAA068) for more information on the ideal op amp.



PARAMETER	VALUE
Gain ( $a$ )	$\infty$
Input resistance ( $R_i$ )	$\infty$
Output resistance ( $R_o$ )	0
CMRR	$\infty$
$K_{SVR}$	$\infty$
$V_E$	0

Figure 1. Ideal Op-Amp Model and Model Parameters

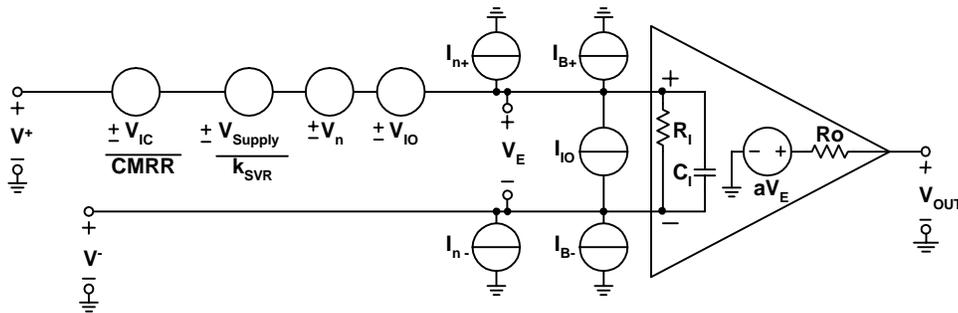
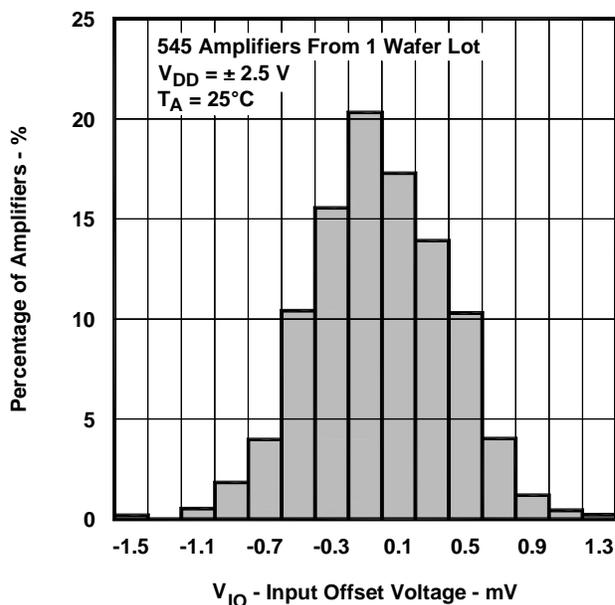


Figure 2. Nonideal Op-Amp Model

## 2 Input Offset Voltage Defined

The input offset voltage is defined as the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output. Ideally the output of the op amp should be at zero volts when the inputs are grounded. In reality the input terminals are at slightly different dc potentials.  $V_{IO}$  is symbolically represented by a voltage source that is in series with either the positive or negative input terminal (it is mathematically equivalent either way). It can be either negative or positive in polarity, varying from device to device (die to die) of the same wafer lot. Figure 3 shows the distribution of  $V_{IO}$  measured in one wafer lot of the TLV2721 op amp as an example of the variance that  $V_{IO}$  may have.



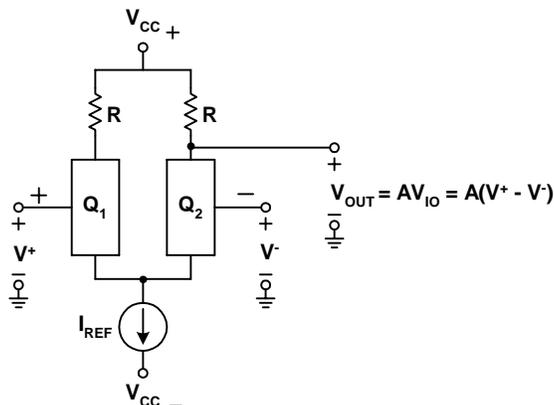
**Figure 3. Distribution of  $V_{IO}$  for the TLV2721**

$V_{IO}$  is considered to be a dc error and is present from the moment that power is applied until it is turned off, with or without an input signal. It occurs during the biasing of the op amp and its effect can only be reduced, not eliminated.

### 3 Cause of $V_{IO}$

The cause of input offset voltage is well known—it is due to the inherent mismatch of the input transistors and components during fabrication of the silicon die, and stresses placed on the die during the packaging process (minor contribution). These effects collectively produce a mismatch of the bias currents that flow through the input circuit, and primarily the input devices, resulting in a voltage differential at the input terminals of the op amp.  $V_{IO}$  has been reduced with modern manufacturing processes through increased matching and improved package materials and assembly.

The input stage of most op amps consists of a differential-pair amplifier. A simplified version is shown in Figure 4, where  $Q_1$  (+ or noninverting input terminal) and  $Q_2$  (– or inverting input terminal) can be BJT, FET or MOS transistors. The input terminals of the op amp are the bases (BJT) or gates (FET, MOS) of these transistors. The current source biases the transistors, and ideally each leg of the circuit is balanced so that one half of the current flows through each transistor ( $I_{Q1} = I_{Q2} = I_{REF}/2$ ) and the inverting and noninverting inputs are at the same potential. Mismatches in  $R$ ,  $Q_1$ , and  $Q_2$  unbalance this current. The base (gate) voltages of the transistors then become unequal, creating the small differential voltage,  $V_{IO}$ .



**Figure 4. Simplified Differential-Pair Amplifier. Q1 and Q2 Are BJT, FET or MOS.**

When the op amp is open loop, this small differential voltage is multiplied by the large internal gain of the op amp. At the very least, the output dynamic range will be greatly reduced. Normally, however, the output of the op amp is driven to one of the power supply rails, saturating the device. When the op amp is operated closed loop the differential voltage is multiplied by the noninverting closed loop gain of the op amp, which is set by the circuit designer.

#### 4 $V_{IO}$ and Temperature Drift in the Major Device Types

There are three major manufacturing processes in which most op amps can be grouped: bipolar, BiFET, and CMOS. The magnitude of  $V_{IO}$  varies, but each process has a range associated with it. Table 1 shows the range and drift associated with each process type and lists the typical, max and full range  $V_{IO}$  for various op amps of each type. A brief description of each process and the mechanism of  $V_{IO}$  and drift for that particular process are described below. See Gray and Meyer [2], and Dostal [3] for more detail concerning  $V_{IO}$  and drift for the processes described in this section.

**Table 1. Range of Input Offset Voltage and Drift Per Device Process**

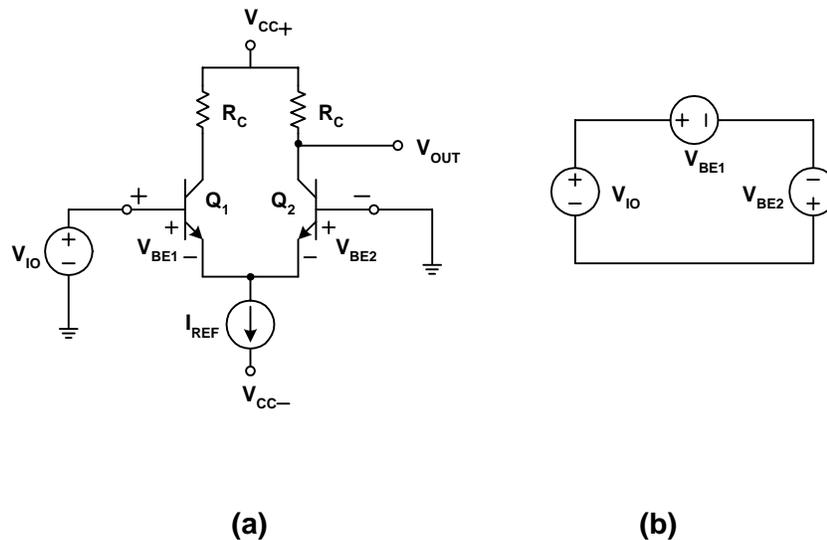
PROCESS AND DEVICE TYPE	$V_{IO}^{max}$ at 25°C (μV)	$\Delta V_{IO}/\Delta T^\dagger$ (μV/°C)	$V_{IO}$ Full Range (μV)	Long term Drift <sup>†</sup> (μV/month)
Bipolar LM324 TLE2021 THS4001	150 – 10000 7000 500 8000	1 – 10  2 10	240 – 15000 9000 750 10000	0.005
BiFET LF353 TLE2071 TL051	800 – 15000 10000 4000 3500	1 - 30 10 3.2 8	3000 - 20000 13000 6000 4500	0.04
CMOS TLC071 TLV2471 TLC2201	200 – 10000 1000 2200 200	<1 – 10 1.2 0.4 0.5	300 - 13000 1500 2400 300	0.005

†Typical specifications

Note: Devices listed are commercial, ranges valid for all temperature ranges

## 4.1 Bipolar

Bipolar op amps consist solely of bipolar junction transistors (BJTs). These devices typically have the lowest  $V_{IO}$  and low temperature drift. A wide range of performance specifications are available, ranging from low performance, widely used relics such as the LM324, to the more contemporary op amps such as the TLE2021 and the high speed THS4001.



**Figure 5. Bipolar Transistor Differential-Pair Circuit. (a) Basic Circuit and (b) General Circuit Used to Calculate  $V_{IO}$**

Substituting bipolar NPN transistors for  $Q_1$  and  $Q_2$  in the circuit of Figure 4, and setting  $R = R_C$  provides the basic NPN bipolar differential input circuit shown in Figure 5a. Small resistors may also be placed at the emitter of the devices to improve linearity and speed at the cost of increased noise and decreased open loop gain. This is normally done as it increases stability, but the effect is not discussed here.

In the bipolar process  $V_{IO}$  is created primarily by differences in the base width, emitter area, and doping levels of the base and collector of transistors  $Q_1$  and  $Q_2$  (see reference 2). These errors create differences in the bias currents flowing in the legs of the differential pair. The overall result is a difference in the  $V_{BE}$  values of  $Q_1$  and  $Q_2$ , which causes the differential voltage  $V_{IO}$  to appear across the op amp inputs.

When the inputs are grounded, a loop is formed as shown in Figure 5b. Kirchoff's voltage law (KVL) is then used to obtain equation (1), rewritten in the form of equation (2).  $V_{BE}$  is defined in equation (3), where the term  $kT/q$  is known as the thermal voltage ( $V_T$ ),  $I_C$  is the collector current, and  $I_S$  is the reverse saturation current. Then equation (3) is substituted into equation (2) and manipulated into the form in equation (4):

$$-V_{IO} + V_{BE1} - V_{BE2} = 0 \quad (1)$$

$$V_{IO} = V_{BE1} - V_{BE2} \quad (2)$$

$$V_{BE} = \left( \frac{kT}{q} \right) \ln \left( \frac{I_C}{I_S} \right) \quad (3)$$

$$V_{IO} = \left( \frac{kT}{q} \right) \ln \left( \frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}} \right) \quad (4)$$

The errors introduced in equation (4) by the  $I_C$  terms are due to the mismatch in the  $R_C$  resistors. The  $I_S$ -term errors are due primarily to mismatches in the area of the emitter and the width and doping of the base (see Gray and Meyer [2]). The value of  $V_T$ , or  $kT/q$ , is material dependent (e.g., 26 mV for silicon) and is inherent in all transistors. This term has the largest impact on  $V_{IO}$  and its drift with temperature. As  $T$  changes  $V_{IO}$  changes, and the change is predictable.

The offset drift over time is low for bipolar input stages, and typically ranges from a few  $\mu\text{V}/\text{month}$  down to a few  $\text{nV}/\text{month}$ . This parameter is dependent upon the heat and mechanical stress induced on the op amp by the fabrication of the circuit board and the application circuit.

The overall maximum  $V_{IO}$  can be calculated for a bipolar op amp using equation (5), again ignoring any second-order effects. Remember, this value can be positive or negative. The first term is the base  $V_{IO}$  at room temperature. The second term is calculated by multiplying the value for drift from the data sheet by the temperature change,  $\Delta T$ , in  $^{\circ}\text{C}$  or  $\text{K}$ . The final term is the drift over time; the drift per month is a device parameter and is multiplied by the number of months the part is intended to be in use.

$$V_{IO} = V_{IO}(25^{\circ}\text{C}) + \left( \frac{V_{IO}}{T} \right) \cdot \Delta T + \left( \frac{\Delta V_{IO}}{\text{month}} \right) \cdot \text{months} \quad (5)$$

## 4.2 BiFET

BiFET op amps consist of a JFET input stage and BJTs in the gain and output stages. These devices typically have the highest  $V_{IO}$  and temperature drift of the 3 process types. This is attributed to the transconductance of the JFET, which is lower than that of the BJT (see Gray and Meyer [2]). DC precision is sacrificed in BiFET op amps so they are generally used when a high input impedance or ac performance is needed. Once again, a wide range of performance specifications are available, ranging from the low precision LF353 to the contemporary TL081 and the high precision (for a JFET) TL051.

The BiFET differential input circuit is the same as the bipolar circuit shown in Figure 5, with JFET transistors substituted for  $Q_1$  and  $Q_2$ . The collector load resistor  $R_C$  now becomes the drain load resistor  $R_D$ . Again, Kirchoff's voltage law is used to derive equation (6).  $V_{GS}$  is defined in equation (7), assuming the JFET is a square-law device, and substituted into equation (6) to get equation (8).

$$V_{IO} = V_{GS1} - V_{GS2} \quad (6)$$

$$V_{GS} = V_P \left[ 1 - \left( \frac{I_D}{I_{DSS}} \right)^{1/2} \right] \quad (7)$$

$$V_{GS} = (V_{P1} - V_{P2}) - V_{P1} \left( \frac{I_{D1}}{I_{DSS1}} \right)^{1/2} + V_{P2} \left( \frac{I_{D2}}{I_{DSS2}} \right)^{1/2} \quad (8)$$

The JFET is much more sensitive to changes in bias current from mismatches in the channels of  $Q_1$  and  $Q_2$ ,  $R_D$  and  $I_{REF}$ , resulting in a higher overall  $V_{IO}$  than the bipolar differential input stage.  $V_{IO}$  for the BiFET process is primarily created by mismatching of the pinch-off voltages ( $V_P$ ) of the devices as represented in the first term (in parenthesis) of equation (8). The channel doping level and thickness are the components of  $V_P$  that create this error. The second and third terms also have some error introduced by  $V_P$ , as well as error introduced by  $I_D$  through the mismatching of  $R_D$  and  $I_{DSS}$  caused by the channel geometry and doping levels of the input transistors. The overall result is a difference in the  $V_{GS}$  voltages of  $Q_1$  and  $Q_2$ , causing  $V_{IO}$  to appear across the op-amp inputs.

The offset drift over time is similar in magnitude to that of the bipolar process. It is interesting to note that plastic packaging induces stresses on the die that prevent low  $V_{IO}$  and drift. Ceramic or metal packages must be used for the high precision BiFET devices. These materials conduct heat much better than the plastic, keeping the thermal gradients on the die more uniform and reducing the heat-related stress. Overall  $V_{IO}$  is calculated as for the bipolar using equation (5).

## 4.3 CMOS

CMOS op amps consist of complimentary MOS transistors (NMOS and PMOS together) throughout the device. Two other types of CMOS devices are available – BiCMOS and BiMOS. CMOS devices typically have a low  $V_{IO}$  and the lowest drift of the processes. These amplifiers make excellent low voltage, single-supply, rail-to-rail op amps. Some examples consist of the general-purpose LinCMOS TLC272, the low voltage rail-to-rail input/output TLV2474, and the TLC2201.

The CMOS differential input circuit is the same as that of the bipolar in Figure 4, with MOS transistors substituted for  $Q_1$  and  $Q_2$ . The loop equation derived is identical to equation (6). The MOSFET definition for  $V_{GS}$  in equation (9) is substituted into equation (6) and manipulated into the form of equation (10). Here  $V_{IO}$  is primarily due to differences in the threshold voltage,  $V_T$  (not to be confused with the thermal voltage,  $V_T$ , of bipolar devices), caused by variations in the width, length, thickness and doping levels of the channels in the transistors (see Gray and Meyer [2]). The differences cause variations in the threshold voltage,  $V_T$ , of the devices; thus,  $V_T$  mismatching is the primary contributor to  $V_{IO}$  in the MOSFET.

$$V_{GS} = V_T + \left( \frac{2I_D}{k'} \cdot \frac{L}{W} \right)^{1/2} \quad (9)$$

$$V_{IO} = (V_{T1} - V_{T2}) + \sqrt{\left( \frac{2I_{D1}}{\mu C_{OX}} \cdot \frac{L_1}{W_1} \right)} - \sqrt{\left( \frac{2I_{D2}}{\mu C_{OX}} \cdot \frac{L_2}{W_2} \right)} \quad (10)$$

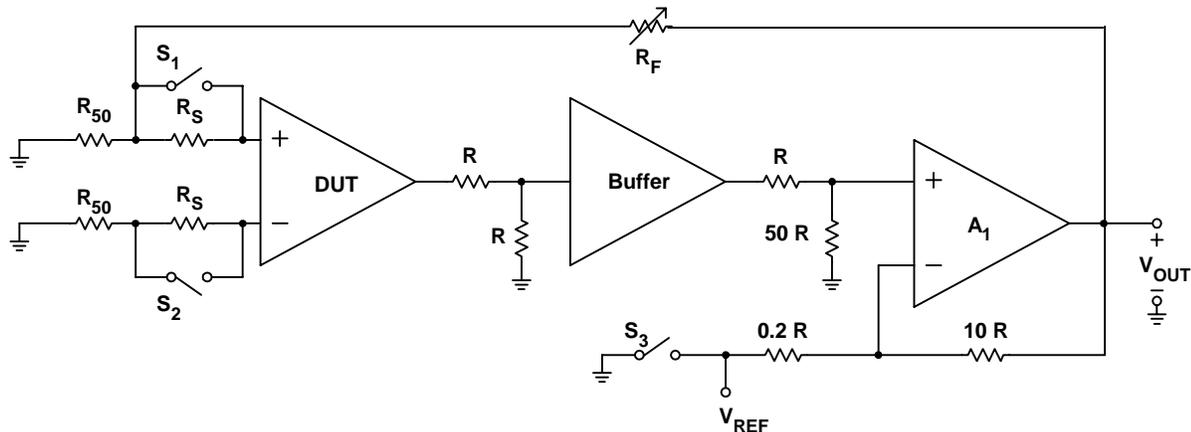
Typically, the offset drift over time is of the order of nanovolts per month. The overall maximum  $V_{IO}$  is calculated the same as for a bipolar using equation (5).

## 5 Manufacturer Measurement, Trim, and Specification of $V_{IO}$

The salient dc parameters for each device are printed in its data sheet. To understand fully the specifications on the data sheet, it is necessary to understand the methods used by the manufacturer to measure, reduce, or trim,  $V_{IO}$ . This section briefly explains how the measurement and trim process is performed. It then explains and provides examples of the specifications for various devices.

### 5.1 Measurement

Most of the parameters are measured using a servo loop. Figure 6 shows a simplified circuit. This test loop is used for the major dc parameter measurements.  $V_{IO}$  is measured with switches S1 and S2 closed, essentially providing a very low source impedance to ensure that input bias current offsets are negligible during the measurement. The inverting input of op-amp A1 controls the output of the device under test (DUT) through the feedback loop containing  $R_F$  and the 50- $\Omega$  resistor. When S3 is closed A1 drives the output voltage of the DUT to zero by applying the necessary voltage to the positive terminal. Thus, the voltage across the 50- $\Omega$  resistor is equal to  $V_{IO}$  and the output of A1 is  $-(R_F/50)V_{IO}$ . Resistor  $R_F$  is adjusted depending on the expected offset voltage of the DUT so that the output of A1 is not saturated, yet is easily discerned.



**Figure 6. Simplified Servo-Loop Test Circuit**

## 5.2 Trim

Most op amps have some form of offset trim that is performed during the manufacturing process. The op amps with bipolar and JFET inputs use a Zener diode trim technique to reduce the offset voltages. This method places a network of Zener diodes with series resistance in parallel with the biasing collector-drain resistor. The Zener diodes are then blown as required to increase the parallel resistance, lowering the overall biasing resistance in the desired leg of the circuit.

Op amps with CMOS inputs use a fuse-link trim network because a CMOS diode structure is not available. This method places a fuse in series with resistors, rather than the Zener diode. When the fuse is removed, the parallel resistance is decreased, and the biasing resistance is increased in the desired leg of the circuit.

Laser trim is another alternative that is often used to lower  $V_{IO}$ . A resistor network is often created and then portions eliminated to increase or decrease the resistance and balance the currents in each leg of the differential pair. This is a more precise technique and is reserved for precision parts.

Devices in multiple packages (duals and quads) often have less trim capability. This is because the space is reduced on the silicon die for adding trim networks. Multiple op amps on a package use up all available space, particularly the quads. One or more op amps on a quad package may, therefore, have a higher offset rating than the single- or dual-packaged devices, although good design and layout of the IC often prevents this.

## 5.3 Specifications

The very name input offset voltage indicates that it has been referred to the op-amp input. This is done with all of the error sources because the actual output created by any error source depends on the closed loop gain ( $A_{CL}$ ) of the circuit, as seen from the error source. Thus  $V_{IO}$  must be multiplied by  $A_{CL}$  for the noninverting circuit to be referenced to the output.

**Table 2. Example of  $V_{IO}$  Specifications Taken From TLE2021 Data Sheet (SLOS191)**

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLE2021C			TLE2021AC			TLE2021BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C		120	500		80	200		40	100	$\mu V$
			Full range						500			200	$\mu V$
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu V/^\circ C$
	Input offset voltage long-term drift		25°C		0.006			0.006			0.006		$\mu V/mo.$

Note: Characteristics at free air temperature and  $V_{CC} = \pm 15 V$

Table 2 shows the  $V_{IO}$  portion of the TLE2021 data sheet (SLOS191). Each  $V_{IO}$  specification has a column on the data sheet for the minimum, typical, and maximum values to be listed. There are four major  $V_{IO}$  specifications that may be provided for an op amp:  $V_{IO}$  at 25°C,  $V_{IO}$  full range,  $\alpha_{V_{IO}}$  (drift) over some specified temperature range, and  $V_{IO}$  drift over time. Each device further falls under a specified operating temperature range that has a designated letter indicator. Commercial (C) parts are specified over 0°C to 70°C, industrial (I) from -40°C to 85°C, and military (M) from -55°C to +125°C. The table shows data only for the commercial-grade device. The older devices sometimes have different grades available. These are marked with letters such as A, B, or no letter. These grades indicate the accuracy of the part: the better the quality (grade), the lower the dc errors. Check with each manufacturer for their particular grades.

The first entry is for  $V_{IO}$  under static temperature conditions, where the maximum and typical values are listed for a temperature of 25°C. This specification is listed on virtually all op-amp data sheets and is expressed in millivolts (mV) or microvolts ( $\mu V$ ). Typical values are meaningless in design because, as was shown by the variance of  $V_{IO}$  in Figure 3, it is the maximum values that the designer needs to know. Basing the design on typical numbers is destined to lead to trouble because eventually a batch of ICs will arrive that contains devices near the maximum rating. While not truly this random, it is possible that natural variations or future changes in the process used to create a device result in a  $V_{IO}$  that is much different from the typical value. Typical values are not assured, but the maximum data-sheet values are. Every device is tested at the factory to ensure that it does not exceed the maximum specified value before it is shipped to the customer.

On the data sheet,  $V_{IO}$  full range is usually provided, but normally only has a maximum rating and thus is assured. Devices are tested prior to shipment to ensure they do not exceed this range. This specification lists the worst possible  $V_{IO}$  that can be encountered over a specified temperature range. Occasionally the full range is specified for a temperature range less than the maximum operating temperature range, so strict attention must be paid to the conditions.

The drift of a device with temperature is indicated by  $\alpha_{V_{IO}}$ . This is an average that is calculated using the ends of the specified temperature range as shown in equation (11). For example,  $V_{IO}$  for a commercial part is measured at 0°C (TA1) and 70°C (TA2) and the results are calculated and expressed as the number of microvolts of increase in  $V_{IO}$  per degree Celsius of temperature change ( $\mu V/^\circ C$ ). Drift is not always given as a typical value on data sheets. The exception is for

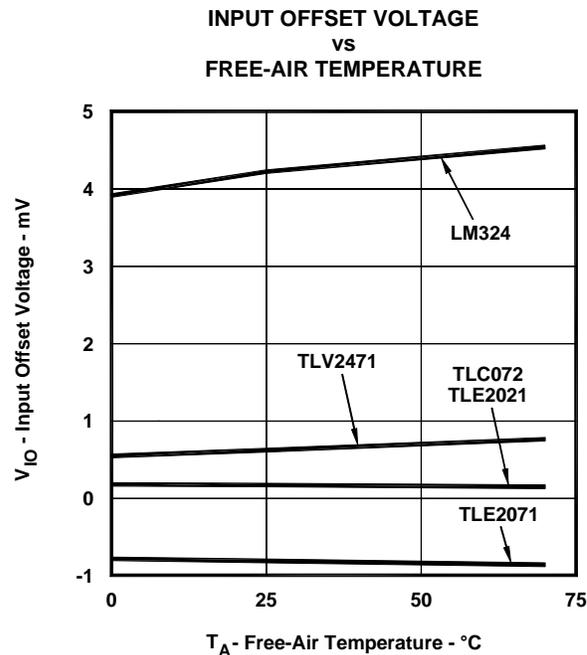
chopper-stabilized op amps, which are used when low  $V_{IO}$  and drift are critical—in this case, the maximum value for  $\alpha_{VIO}$  is listed. The specification is fully tested and assured when the maximum or minimum values are listed. Typical specifications are not assured.

$$\alpha_{VIO} = \frac{V_{IO}(T_{A1}) - V_{IO}(T_{A2})}{T_{A1} - T_{A2}} \quad (11)$$

When only typical values are listed,  $\alpha_{VIO}$  has been tested initially and the devices are monitored for quality, but the value is not assured. When  $\alpha_{VIO}$  is not specified, or only a typical value is provided, use the full range data if possible. If this is not available or does not cover the desired range, measurements must be taken or an amplifier found that specifies the desired data. It is never a good idea to assume and there is usually a good reason why the data is not specified.

The temperature drift,  $\alpha_{VIO}$ , is measured with the assumption that the temperature dependence of  $V_{IO}$  is linear. This representation is fairly accurate for small mismatches in the device input transistors, which is normally the case for manufacturing technology today. Second-order effects have only a slight impact on the linearity over most of the temperature range that is specified in the measurement conditions.

Figure 7 shows  $V_{IO}$  measured at 0, 25 and 70°C for several device types that are standard commercial grade, which means they are standard parts that have a temperature range of 0 to 70°C. The slope of each line indicates the magnitude of  $\alpha_{VIO}$ , or drift, for that part. The steeper the line, the greater the  $\alpha_{VIO}$ .

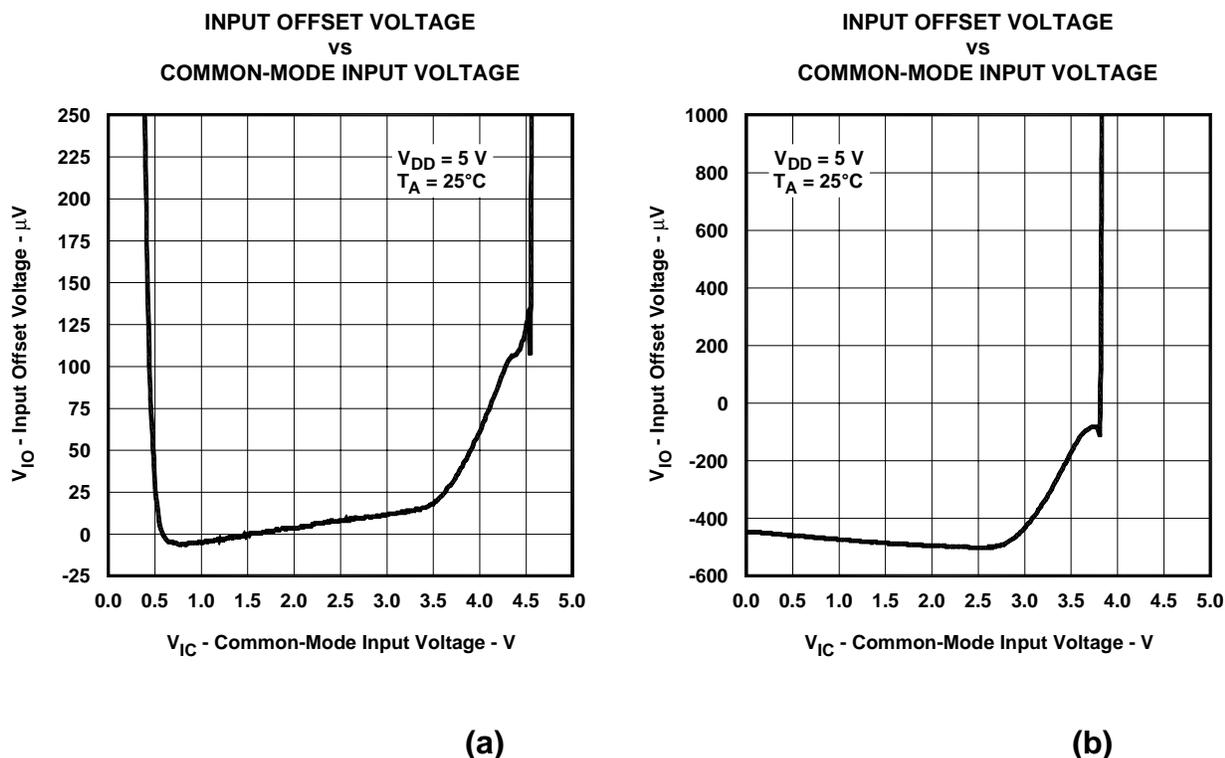


**Figure 7. Graph of  $V_{IO}$  Drift Over 0–70°C**

The LM324 represents the legacy bipolar op amp that has a  $V_{IO}$  that is over an order of magnitude greater than that of the newer TLE2021, and the most severe  $\alpha_{VIO}$  of the parts tested. The TLE2071 is a top performance BiFET op amp having a very low  $V_{IO}$  (for JFET input op amps) that is only slightly larger than the CMOS rail-to-rail TLV2471 op amp. These parts have similar typical specifications for  $V_{IO}$ , but the TLE2071 has a maximum specification almost double that of the TLV2471, and has the highest possible  $\alpha_{VIO}$  specified, though the drift shown in Figure 7 is respectable. The TLC072 represents the standard CMOS op amps, and the  $V_{IO}$  and  $\alpha_{VIO}$  measured were almost identical to the TLE2021 bipolar op amp. The difference between them is in tens of microvolts, indistinguishable at the scale provided. The  $V_{IO}$  specifications of the TLC072 are almost double that of the TLE2021. These measurements serve to illustrate the point that  $V_{IO}$  and  $\alpha_{VIO}$  will vary from device to device, even within the same family, and so the maximum specifications should be used when possible.

The changes in  $V_{IO}$  from heat stress of the part. (Heat stress affects the packaging through expansion and contraction which applies mechanical stress to the silicon die.) It is measured over a period of time, normally from 1 to 3 weeks, at an elevated temperature of 150°C to simulate aging of the device. When this specification is listed, conditions and assumptions are provided. Again, the typical specifications are not assured. Because of feasibility, the maximums are not tested for this parameter on every device, but they are assured by the design. The typical parameter may be useful for reliability calculations to provide an indication of the useful life of the part. This parameter is specified in microvolts per month ( $\mu\text{V}/\text{month}$ )

The only other information provided for  $V_{IO}$  is in the form of data graphs. These graphs depict a typical device—the assured specifications are in the tables of the data sheet. Figure 8 is an example of the relationship between  $V_{IO}$  and the input common mode voltage ( $V_{IC}$ ). Since  $V_{IO}$  is normally tested at one value of  $V_{IC}$  (0 V), such graphs are useful in correlating information that is not specified in the data sheet. They provide the designer with an understanding of the behavior of the device over a wide range of values.



**Figure 8.  $V_{IO}$  vs  $V_{IC}$  for (a) TLC071 and (b) TLC081 Op Amps**

When the limits of  $V_{IC}$  are approached,  $V_{IO}$  quickly goes off scale. As a general rule, when the common-mode input voltage increases,  $V_{IO}$  increases. The TLC081 is similar to the TLC071 op amp, but has  $V_{IO}$  adjusted so that it includes power ground, and  $V_{IO}$  is stable down to that point. This is very useful for in circuits where the inputs must include the ground rail, for example, with some sensors. This graph is useful to determine the impact of  $V_{IO}$  for a given input range, but it is covered under the full-range value as described earlier in this section.

The relationship between  $V_{IO}$  and  $V_{IC}$  is different when dealing with CMOS rail-to-rail input op amps. Figure 9(a) shows a graph of  $V_{IO}$  versus  $V_{IC}$  for the TLV247x. A stair-step transition is created by the input stages of the op amp, where a PMOS differential pair and an NMOS differential pair are placed in parallel.  $V_{IO}$  is high at low  $V_{IC}$  because the NMOS transistors are active and the PMOS transistors are off, and it drops sharply as the NPN/PMOS transistors turn on.  $V_{IO}$  is stable during the mid-range, when the offset voltages of the parallel differential pairs are in equilibrium. As  $V_{IC}$  nears the upper power supply rail, the NMOS transistors turn off and only the  $V_{IO}$  of the PMOS transistors is present. Figure 9(b) shows the graph of  $V_{IO}$  versus  $V_{IC}$  for the TLV2731 and is typical for a CMOS op amp that does not have rail-to-rail inputs. Such changes introduce distortion, and the circuit must be analyzed to determine if it is acceptable for the application.

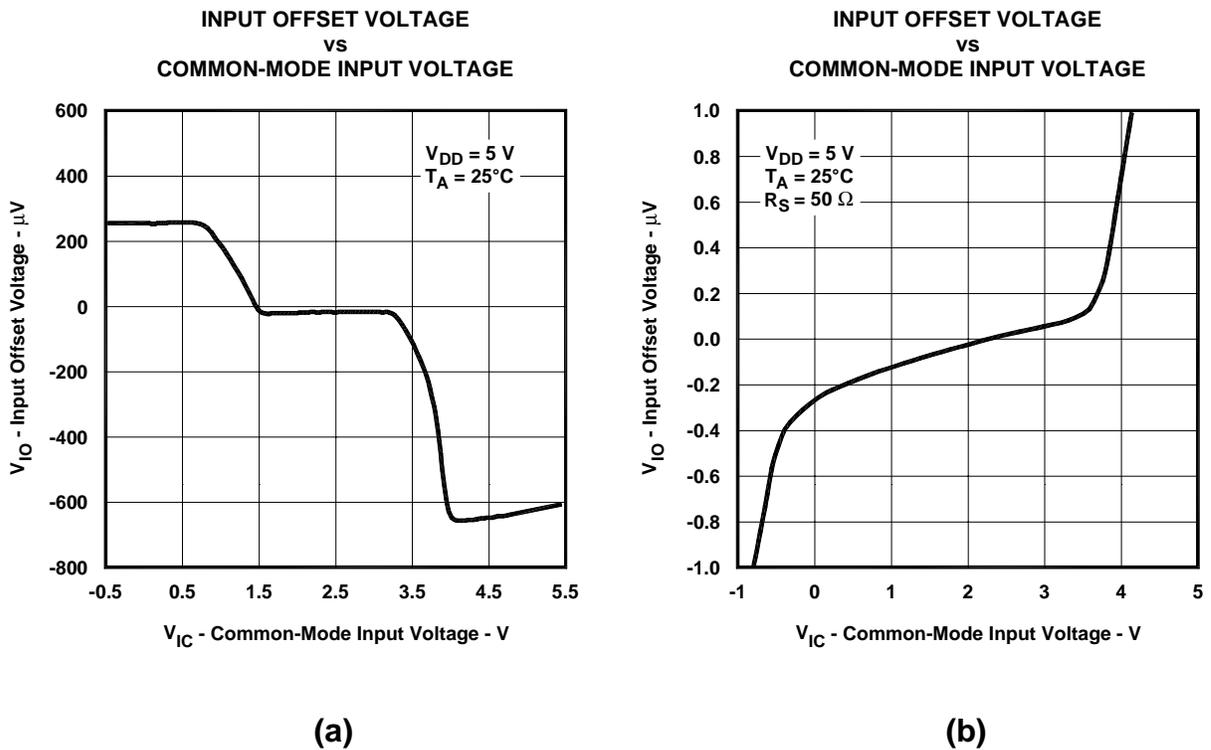


Figure 9.  $V_{IO}$  Changes With Common Mode Input Voltage ( $V_{IC}$ ) for (a) the TLV247x and (b) the TLV2731

## 6 Impact of $V_{IO}$ on Circuit Design and Methods of Correction

Figure 10 shows an inverting op amp circuit with  $V_{IO}$  included. Superposition is used to find the closed loop gain of the circuit ( $A_{CL}$ ) in equation (12) (see Understanding Basic Analog—Circuit Equations, SLOA025,[5]).

$$V_O = V_I \left( \frac{-R_F}{R_G} \right) \pm V_{IO} \left( 1 + \frac{R_F}{R_G} \right) \quad (12)$$

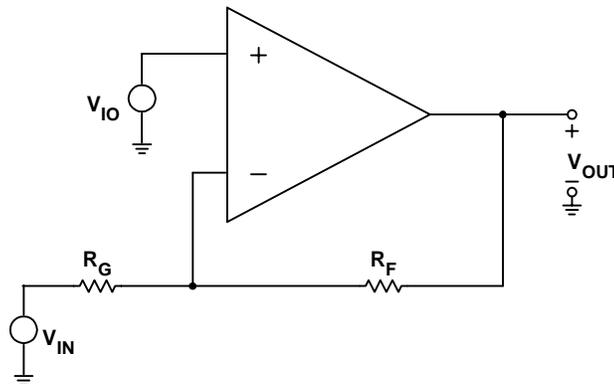


Figure 10. Inverting Op-Amp Circuit With  $V_{IO}$  Included

$V_{IO}$  is always multiplied by the noninverting gain of the op amp and added to (or subtracted from) the signal gain of the circuit, which is  $-(R_F/R_G)$  in this example. In large-gain dc-coupled circuits,  $V_{IO}$  may be significant and may need to be reduced through offset adjustment techniques, although an op amp with very low offset may not require adjustment. Normally, adjustment of  $V_{IO}$  is used only when the dc accuracy is necessary in order to reduce distortion.

Adding the effects of temperature and time to equation (12) gives equation (13). This allows a fairly accurate calculation of the worst-case change in the output due to  $V_{IO}$ , neglecting the effect of the resistors; however, the resistor values also change with temperature and will affect the gain of  $V_{IO}$ . Equation (13) does not include the errors from the other dc and ac sources as shown in Figure 2 for the nonideal op amp—the focus is strictly on  $V_{IO}$ —and they must be included in final calculations.

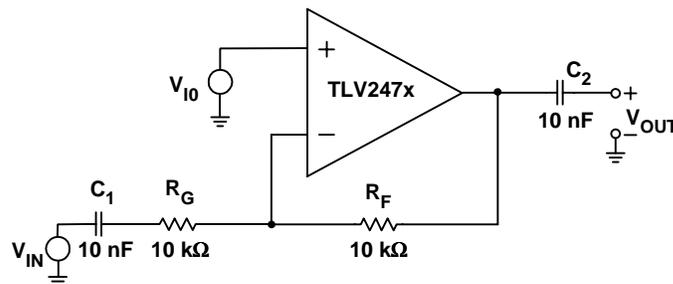
$$V_O = V_I \left( \frac{-R_F}{R_G} \right) + V_{IO} \left( 1 + \frac{R_F}{R_G} \right) + \Delta V_{IO} \left( \frac{\Delta T}{T} \right) + \Delta V_{IO} \left( \frac{\Delta t}{t} \right) \quad (13)$$

The first step is to determine the maximum allowable dc error in the system. An error budget analysis must be performed to determine all the dc error sources in the system, and the maximum contribution the design allows for each section. If the op amp or other device fails to meet the specification for  $V_{IO}$ , compensation then attempts to remove or reduce the offset.

Methods for reducing the effects of  $V_{IO}$  include circuit modifications such as ac-coupling and dc feedback. In some applications, the solution is to use devices that have some form of internal or external calibration, such as chopper stabilization, an autozero loop, or offset trim. These methods are briefly described in the following sections. Applications that utilize a computer to correct for dc offset are not covered in this report.

## 6.1 AC Coupling

$V_{IO}$  affects the signal conditioning ability of an op amp circuit in both ac-coupled and dc-coupled circuits. Figure 11 shows an ac-coupled inverting op amp. The capacitor  $C_1$  ac-couples the input from the previous stage, and  $C_2$  ac-couples the output to the load. Thus,  $C_1$  prevents any dc current from flowing through  $R_F$  and  $R_G$  (with the exception of bias currents) and  $C_2$  prevents any dc current from flowing into the load.  $V_{IO}$  appears across the inputs and, because there is no dc-current flow, the gain is unity, and the amplifier output is at the same potential as the inverting input. This is the case even if the output is not dc-coupled ( $C_2$  is not present) because  $V_{IO}$  does not appear across  $R_G$ . The capacitors also serve to establish some filtering in the circuit, the values being chosen to set some desired 3-dB point.



**Figure 11. AC Coupled Inverting Amplifier**

When  $C_1$  is removed from the circuit the amplifier is dc-coupled to the signal source. This is the case with DACs and many transducers such as temperature sensors and strain gauges. Transducers output voltages, currents, or resistances, and the latter require conversion to a voltage. Such applications require dc conversions and  $V_{IO}$  and the drift play a big part in the accuracy. With  $C_1$  removed, the  $V_{IO}$  of the op amp is multiplied by the noninverting gain  $(1+R_F/R_G)$  of the circuit, and is added to any dc offset of the source multiplied by the signal gain  $(-R_F/R_G)$ . The worst case is when the two offsets add together. If the gain of the circuit is large, either the dynamic range is greatly reduced or the output is saturated. If  $C_2$  is also removed, the situation gets worse, for the load now has a dc-offset applied.

Audio power amplifiers use ac-coupling at the input to prevent any dc-voltage component of the input signal from adding to the dc level of the audio circuit (which is normally set to the mid-rail of the power supply for maximum dynamic range). For single-ended loads such as headphones, the output is ac-coupled to prevent any dc voltage from being dropped across the speakers which might possibly damage the speakers.

$V_{IO}$  reduces the dynamic range of an ADC, as well. The loss of dynamic range affects the resolution of ADC circuits because maximum dynamic range is required for maximum resolution. Table 3 shows the resolution of a least-significant bit for various input-voltage ranges. Usually an op amp can be chosen that has a  $V_{IO}$  low enough to meet the desired resolution. It is easy to find an op amp that meets the  $V_{IO}$  specification for an 8 or ten bit converter, but becomes increasingly difficult as the resolution increases. High speed, low voltage acquisition circuits may require ac-coupling at the op amp input to remove offset contribution from previous stages. An alternative is ac-coupling the op-amp output prior to the ADC input to remove the dc component, particularly if the  $V_{IO}$  is higher than desired [reference 6]. This is particularly true of the high-speed op amps, which often have a high  $V_{IO}$ . The number of bits of error introduced by a given  $V_{IO}$  is given by the number of bits, equal to  $A_{CL}V_{IO}/\text{LSB}$ , where  $A_{CL}$  is the closed loop gain and LSB is  $V_{(\text{fullscale})}/2^N$  is the least-significant bit of the ADC (see TLC2654 data sheet, SLOS020 [7]).

**Table 3. Converter Resolution**

NUMBER OF BITS	NUMBER OF CODES	LSB VALUE		
		2.7 V	5 V	10 V
8	256	10.55 mV	19.53 mV	39.06 mV
10	1024	2.64 mV	4.88 mV	9.76 mV
12	4096	659.18 $\mu\text{V}$	1.22 mV	2.44 mV
14	16,384	164.79 $\mu\text{V}$	305.18 $\mu\text{V}$	610.35 $\mu\text{V}$
16	65,536	41.20 $\mu\text{V}$	76.29 $\mu\text{V}$	152.59 $\mu\text{V}$
18	262,144	10.30 $\mu\text{V}$	19.07 $\mu\text{V}$	38.15 $\mu\text{V}$
20	1,048,576	2.57 $\mu\text{V}$	4.77 $\mu\text{V}$	9.54 $\mu\text{V}$

High-speed amplifier circuits often use ac-coupling of the inputs and outputs to minimize the magnitude of  $V_{IO}$ , particularly in circuits that have a high gain. When ac-coupling is not possible or is not feasible for some reason, then dc feedback or op amps with calibration can be employed to reduce  $V_{IO}$ .

## 6.2 DC Feedback

Another method for removing  $V_{IO}$  is to use some form of a dc feedback loop. This can be done in many ways, but the general form of the circuit is shown in Figure 12. Such a loop is used to limit the  $V_{IO}$  of a section of a circuit, usually just before some critical input where the offset must be removed. It reduces the offset voltage to that of the error amplifier only, which can be a DAC, op amp, or some other more elaborate circuit. The dc measurement must be made when there is no input, as represented by the switches. Such offset correction takes a long time to make—usually milliseconds—compared with the speed of the system, and they are made during some noncritical time, such as during start-up.

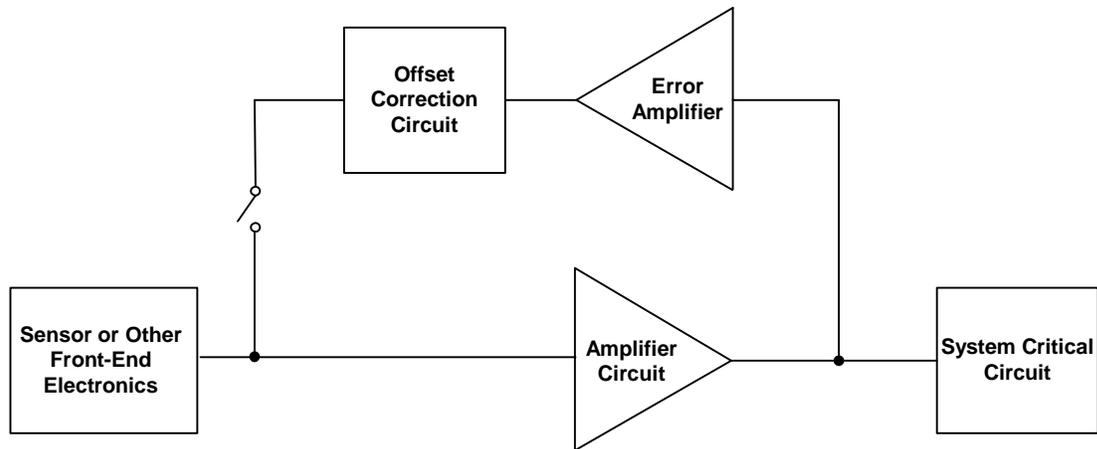


Figure 12. General Form of DC Feedback Loop

## 6.3 Internal Calibration

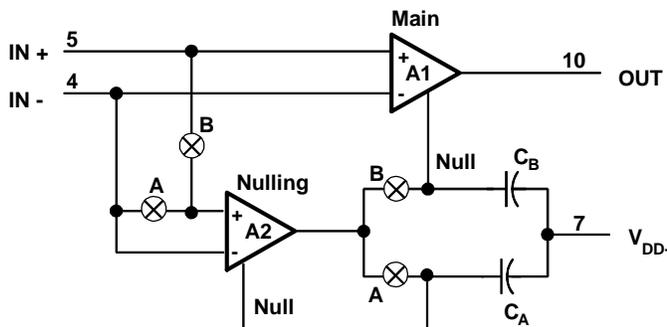
Some devices offer internal dc feedback loops. These features are called autocalibration, Self-Cal™, or autozero and are contained in precision devices such as data converters, codecs, processors, and chopper-stabilized and self-calibrating op amps.

Data converters often have internal biases that create an offset voltage, as well as offsets from the internal circuits that must be removed prior to the output stage of the device. Examples are the DDC101, a 20-bit ADC that performs error correction every integration cycle, and the DAC1220 that has internal calibration with registers for storing actual values or writing user-defined values. Communications devices such as codecs and voice-band audio processors (VBAP™) use autozero circuits at device start-up to reduce the dc error in the transmission paths prior to encoding. Processors for charge-coupled devices (CCDs), such as the VSP2080, have pins for externally controlling the internal calibration with a digital signal.

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Self-Cal and VPAP are trademarks of Texas Instruments Incorporated.

Chopper stabilizers are op amps specifically designed to correct for  $V_{IO}$  and drift and are used when a high degree of accuracy is required at low frequencies. The chopper incorporates internal feedback to eliminate  $V_{IO}$ . The TLC2654 has a 24- $\mu\text{V}$  maximum  $V_{IO}$  over the operating temperature range, with a maximum drift of 50 nV/ $^{\circ}\text{C}$ . This is done through continuous nulling and has the benefit of compensating for variations in  $V_{IO}$  with temperature, time, common-mode voltage and power-supply voltage. Figure 13 is a simplified block diagram of a chopper-stabilized amplifier. These devices consist of a main amplifier, nulling amplifier, and oscillator-controlled logic, and they operate in two phases: a nulling phase and an amplification phase. They require external capacitors for operation.



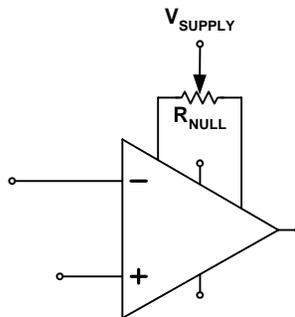
Note: Pin numbers shown are for the D (14 pin), J, and N packages.

**Figure 13. Simplified Block Diagram of the TLC2654 Chopper-Stabilized Amplifier**

During the nulling phase, switches A are closed and B are open, shorting the input of the nulling amplifier (A2). The offset voltage of A2 is stored on capacitor  $C_A$  and is fed back to the input of A2 through the null line. This effectively cancels the  $V_{IO}$  of A2. Next, the A switches are open and the B are closed, connecting the input signal to the inputs of both A1 and A2 during the amplification phase. The offset voltage of A1 is then stored on capacitor  $C_B$ . The voltage on  $C_A$  and  $C_B$  then serve as the null potentials for the next cycle of the system (see TLC2654 data sheet, SLOS020 [7]).

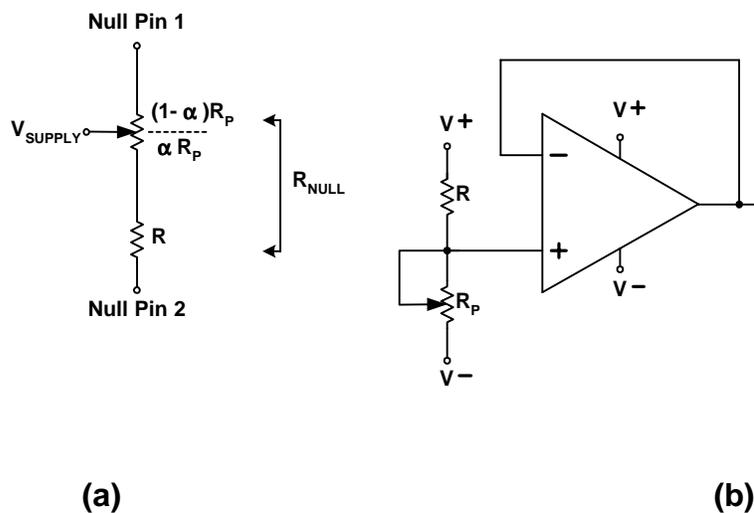
Self-Cal is a technique that allows a CMOS op amp digitally to trim  $V_{IO}$  using converters and a successive approximation register (SAR). Figure 14 shows a single channel of the TLC4502 CMOS rail-to-rail op amp (see TLC4502 data sheet, SLOS221 [8]). During start-up, switch A is open and B is closed, shorting the inputs of the amplifier together and connecting the output to the ADC. The  $V_{IO}$  of the amplifier appears at the output and is converted to a digital signal, then stored on the SAR. The DAC output current is fed into the null line of the amplifier, reducing the  $V_{IO}$ . This system provides a maximum  $V_{IO}$  of 50  $\mu\text{V}$  over the full temperature range and a maximum temperature drift of 1  $\mu\text{V}/^{\circ}\text{C}$ .





**Figure 15. Typical Null Configuration of an Amplifier**

Potentiometers have a very high temperature coefficient that sometimes can be minimized by adding a low-temperature-coefficient resistor ( $R$ ) in series with the potentiometer. Figure 16a shows such a circuit. The nulling potentiometer resistance,  $R_P$ , of Figure 16 is divided into two parts,  $(1-\alpha)$  and  $\alpha$ , to represent the wiper position in equation (14). Equation (14) can also be used when  $R$  is not included in the circuit. This circuit is often used to generate reference voltages or to sum a cancellation current into a summing node to compensate for  $V_{IO}$  as shown in Figure 16b.



**Figure 16.  $V_{IO}$  Adjustment With (a) Potentiometer and (b) Low Temperature Coefficient Resistor**

$$V_{ref} = V_{SS} \frac{\alpha R_P + R}{(1-\alpha)R_P + \alpha R_P + R} \quad (14)$$

More detail concerning methods and effects of external  $V_{IO}$  adjustment can be found in Understanding Basic Analog—Passive Devices, SLOA027 [9] and Nulling Input Offset Voltage of Operational Amplifiers, SLOA045 [10].

## 7 Summary

The dc parameters represent internal errors that occur as the result of mismatches between devices and components inside the op amp. The precision of the op amp is determined by the magnitude of these errors. One of the primary dc errors is the input offset voltage ( $V_{IO}$ ) and is defined as the voltage that must be applied between the two input terminals of an op amp to obtain zero volts at the output.  $V_{IO}$  is symbolically represented by a voltage source that is in series with either the positive or negative input terminal, and that can have either negative or positive polarity, varying from device to device.

$V_{IO}$  is caused by the mismatch of the input transistors and components, primarily in the input stage of the op amp. Such errors are introduced during fabrication of the silicon die and stresses placed on the die during the packaging process (minor contribution). These effects collectively produce a mismatch of the bias currents that flow through the input circuit, resulting in a voltage differential at the input terminals of the op amp.

There are three general manufacturing processes into which most op amps can be grouped: bipolar, BiFET, and CMOS. Bipolar devices typically have the lowest  $V_{IO}$  of the three, and have a low temperature drift. BiFET devices have the worst  $V_{IO}$  and temperature drift. CMOS devices have a  $V_{IO}$  that is close to that of bipolar devices and, of the three types, they have the least drift.

All devices are tested prior to shipment to the customer. DC parameters are measured using a servo-loop, and are normally trimmed during this measurement process. Devices in multiple packages often have less trim capability because of limited space available on the die. When this occurs,  $V_{IO}$  varies between the single, dual and quad packages. The op amps with bipolar and JFET inputs use a Zener-diode trim technique to reduce the offset voltages. Op amps with CMOS inputs use a fuse-link trim network, because a CMOS diode structure is not available. Laser trim is another alternative that is often used to lower  $V_{IO}$ .

$V_{IO}$  is referred to the op amp input in specification sheets. This is done with all the error sources because the actual output created by any error source depends on the closed loop gain,  $A_{CL}$ , of the circuit as seen from the error source.  $V_{IO}$  is multiplied by  $A_{CL}$  for the noninverting circuit to be referenced to the output. There are four major  $V_{IO}$  specifications that may be provided for an op amp:  $V_{IO}$  at 25°C,  $V_{IO}$  full range,  $\alpha V_{IO}$  (drift) over some specified temperature range, and  $V_{IO}$  drift over time. The specification is fully tested and assured when the maximum or minimum values are listed. Typical specifications are not assured. Data graphs only show typical specification information.

An error budget analysis helps determine all the dc error sources in the system and the maximum contribution the design allows for each section. When the op amp or other device fails to meet the specification for  $V_{IO}$ , compensation then attempts to remove or reduce the offset. Methods of reducing the effects of  $V_{IO}$  include ac-coupling and dc feedback. In some applications the solution is to use devices that have some form of internal or external calibration such as chopper stabilization, an autozero loop, or offset trim.

Audio amplifiers, and communications circuits and converters often use ac-coupling to remove  $V_{IO}$ . DC feedback is often used in measurement systems that require precision. Many devices such as instrumentation amplifiers, data converters, codecs, processors, and CMOS chopper amplifiers and Self-Cal amplifiers correct the offsets internally. Other devices, particularly instrumentation amplifiers and op amps in single packages, have external pins where  $V_{IO}$  can be externally reduced. Most of these techniques minimize  $V_{IO}$  only, and at only one temperature. The chopper amplifiers provide continuous correction, even over a temperature range, so they have very low drift. There are drawbacks to each method of  $V_{IO}$  correction that must be considered for each design.

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10. *Nulling Input Offset Voltage of Operational Amplifiers*, Application Report, Texas Instruments (SLOA045)

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