PowerPAD™ Layout Guidelines

Yang Boon Quek *HPL Audio Power Amplifiers*

ABSTRACT

This application report focuses on helping printed-circuit board designers to understand and better use board layout and stencil information for Texas Instruments PowerPAD™ devices.

1 Introduction

Board layout and stencil information for most Texas Instruments (TI) PowerPAD™ devices is provided in their data sheets. This document focuses on helping printed-circuit board (PCB) designers understand and better use this information for optimal designs.

The PowerPAD package is a thermally enhanced, standard-size IC package designed to eliminate the use of bulky heat sinks and slugs. This package can be easily mounted using standard PCB assembly techniques and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the lead frame die pad (or thermal pad) is exposed on the bottom of the IC (see Figure 1). This provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package.

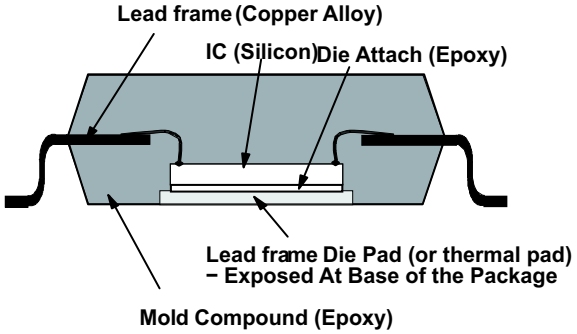


Figure 1. Section View of a PowerPAD Package

PowerPAD is a trademark of Texas Instruments.

2 Board Layout

Figure 2 shows an example of the recommended board layout for a PCB package.

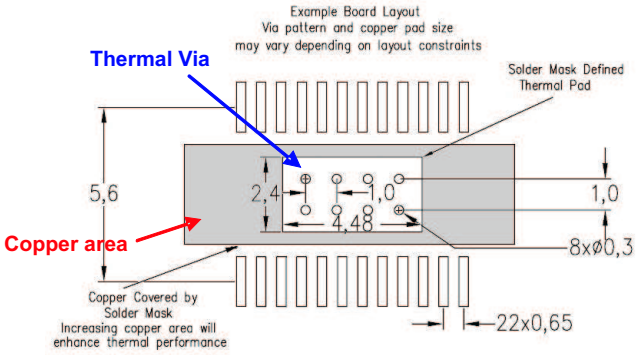


Figure 2. Board Layout for a PCB Package

2.1 Solder Mask Defined Thermal Pad

The solder mask defined thermal pad is the exposed copper area not covered by solder mask. It must be soldered directly to the thermal pad on the bottom of the IC. An example of the recommended dimensions is shown in Figure 2.

2.2 Copper Areas

Copper areas on and in the PCB act as heat sinks for the PowerPAD device. Top copper areas should be covered with solder mask leaving only the solder mask defined thermal pad exposed. The top copper areas should be made as large as possible.

Inner or bottom-layer copper planes can also be connected to the thermal pad by using vias and should be made as large as possible. The thermal pad is usually tied to ground, and designers should ensure electrical correctness when connecting the copper planes to the thermal pad.

Designers may leave the bottom copper plane exposed. However, studies have shown that this has minimal impact on thermal performance.

2.3 Thermal Vias

TI recommends placing thermal vias in the solder mask defined thermal pad to effectively transfer heat from the top copper layer of the PCB to the inner or bottom copper layers.

The thermal vias should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole. Place a ring of exposed copper (0,05 mm wide) around the vias at the bottom copper plane.

Do not cover the vias with solder mask which causes excessive voiding.

Do not use a thermal relief web or spoke connection which impedes the conduction path into the inner copper layer(s).

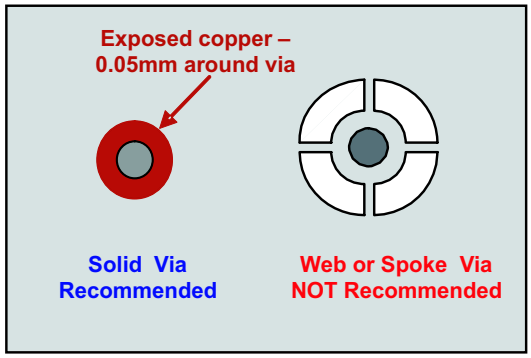


Figure 3. Via Connection at the bottom copper plane

TI provides the recommended layout of the thermal vias in most data sheets. The recommended via diameter is 0,3 mm or less, and the recommended via spacing is 1 mm (see Figure 2 and Figure 4).

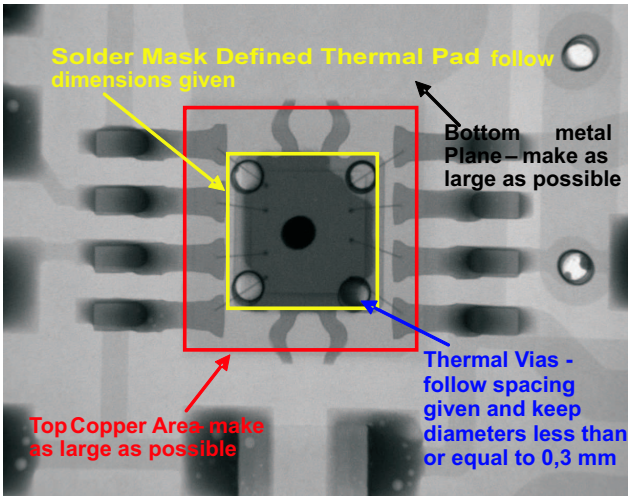


Figure 4. X-Ray – DGN Device

Vias may be plugged to prevent solder loss and protrusions. This often produces the best thermal performances but is not necessary or recommended because of the increased cost of PCB boards and because solder tends to wet the upper surface first before filling the vias.

Vias can also be used in the copper area outside the solder mask defined thermal pad to help transfer heat to the bottom or inner planes (see Figure 5).

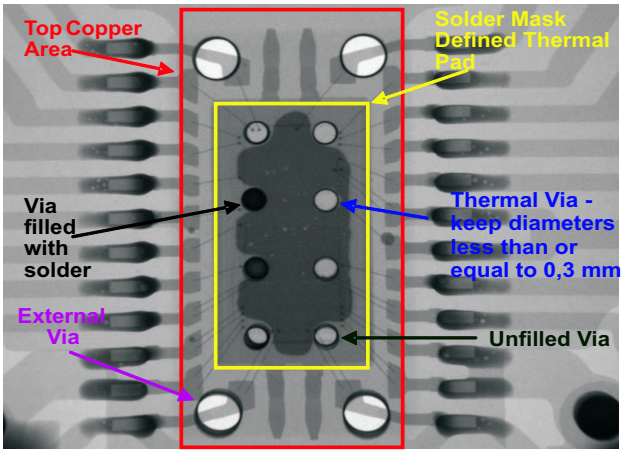


Figure 5. X-Ray – PCB Device With Internal and External Vias

If thin PCB boards or vias larger than 0,3 mm are used, designers may use only external vias to prevent solder loss and protrusions (see Figure 6). Designers should note that this might reduce thermal performance significantly and should be evaluated on their PCBs.

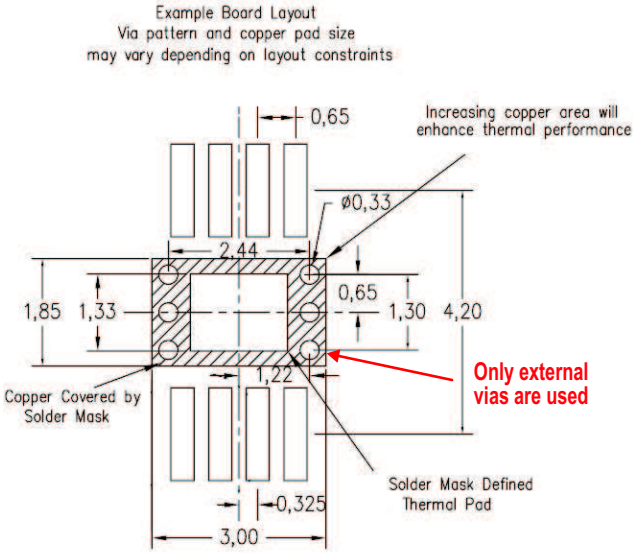


Figure 6. Example of Using Only External Vias

2.4 Solder Loss and Protrusions

Solder loss and protrusions result when excessive solder flowed through internal vias during reflow. These usually happen when incorrect internal vias sizes and stencil openings are used.

Solder loss results in voiding and severely affects thermal conductivity. Designers are encouraged to x-ray their reflowed boards to verify that at least 50% of thermal pad area is soldered (less than 50% voiding) when using 0,127-mm-thick stencils.

Protrusions might cause misalignment in stencil on the reverse side of PCB (see Figure 7).

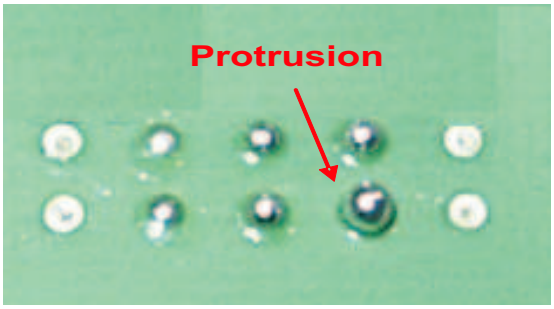
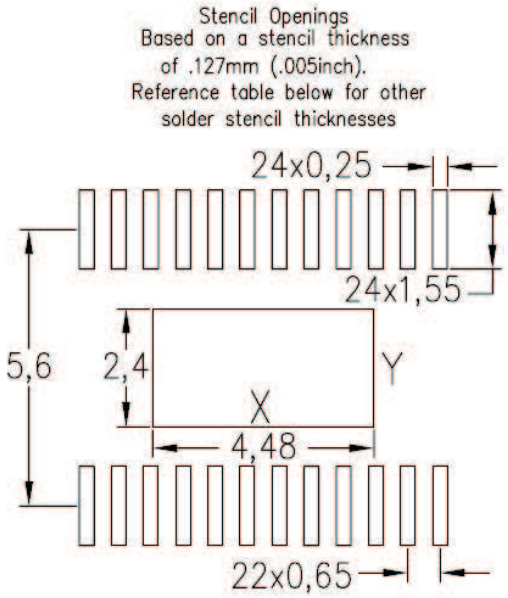


Figure 7. Protrusion at the Other Side of Board

2.5 Stencil

Figure 8 shows an example of the recommended stencil openings and thickness. Follow the stencil openings and thickness recommendations to ensure that the right amount of solder paste is used.



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.75	2.65
0.127mm	4.48	2.4
0.152mm	4.25	2.25
0.178mm	4	2.1

Figure 8. Recommended Stencil Openings for PCB Package

For PowerPAD devices, do not use cross hatching in the stencil thermal pad opening. This significantly reduces the amount of solder paste applied and increases voiding (see Figure 9).

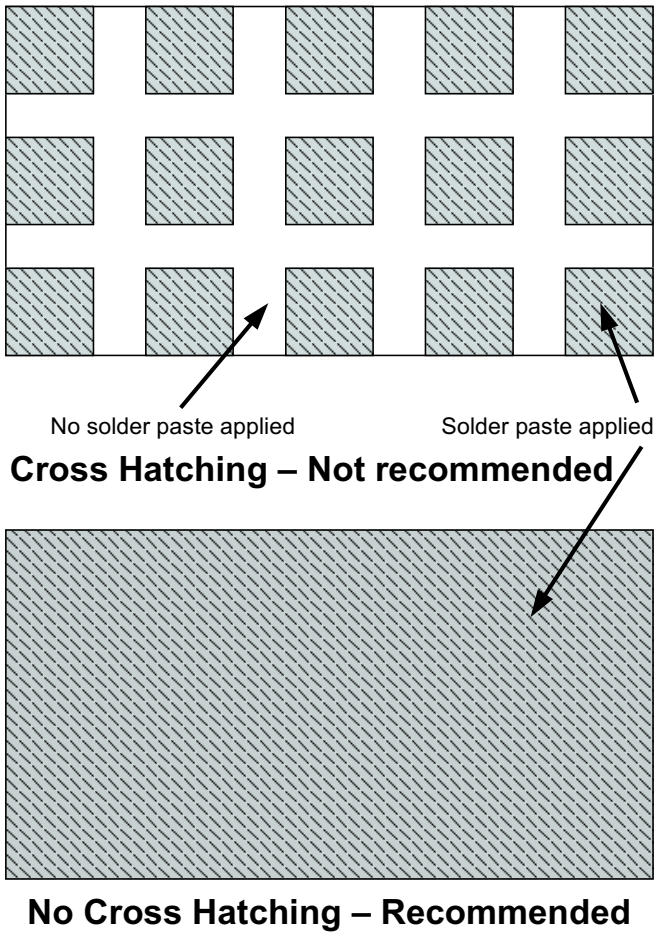


Figure 9. Stencil Thermal Pad Opening

2.6 Recommended Solder Paste

TI recommends using type 3 or finer solder paste when mounting a PowerPAD.

2.7 Additional Information

For detailed information on the PowerPAD package including thermal modeling considerations and repair procedures, see the *PowerPAD Thermally Enhanced Package* application report (SLMA002)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265