Application Report
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Implementation of ISO14443A Anti Collision Sequence in the TI TRF796x

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ABSTRACT

This application note discusses the anti-collision sequence of the ISO14443A standard implemented in the MSP430F2370 (a 16-bit ultra-low power microcontroller from the TI MSP430 family) used with Texas Instruments' TRF796x, a fully integrated 13.56 MHz radio frequency identification (RFID) analog front end and data framing reader system.

This document is designed for use by customers who are experienced with RFID and firmware development and want to develop their own application using the TRF796x. This reference guide should be used in conjunction with the ISO14443A standard which specifies the standard protocol, commands and other parameters required for communication between the transponder and the reader.

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1 Anti-Collision Sequence for ISO14443A

The commands used by the PCD during anti-collision are:

- **REQA** – The REQA commands are sent by the PCD initially to probe the field for PICCs of Type A
- **ANTICOLLISION and SELECT** – Both commands consist of:
  - Select code, SEL (SEL specifies the cascade level)
  - Number of valid bits, NVB
  - 0 to 40 data bits of UID according to the value of NVB (search criterion)

Note: If NVB specifies 40 data bits of UID (NVB = '70'), the command is called a SELECT command. As long as NVB does not specify 40 valid bits, the command is called ANTICOLLISION command.

On reception of a REQA command, the tag (PICC) then responds with an answer to request A (ATQA) block. The reader now recognizes that at least one card in the read range and begins anti collision sequence by sending an ANTICOLLISION command. Only the PICCs whose UIDs match the search criterion respond to this command with the rest of their UIDs.

If there is no collision, the reader reads the data bytes (UID) in the FIFO. The reader then sends the complete UID with NVB = '70' as a SELECT command. The card with the detected UID responds with a select acknowledge (SAK) command. The ISO14443A standard permits UIDs of different lengths – 4 bytes, 7 bytes and 10 bytes. Therefore if the selected card has 7 or 10 bytes UID, it will notify the reader by setting the cascade bit in the SAK command. Thus the reader starts another round of anti collision to detect the second part of the UID. If the UID is 10 bytes long, the anti-collision sequence will have to be run a third time. The SELECT command differentiates between the 3 cascade levels.

If there is a collision, the reader makes note of the bit collision position and therefore reads only those bytes/bits in the FIFO that are valid. This data is now set as the new search criterion. The length of the valid data is NVB. The reader sends out another anti collision command with the new search criterion and length. The PICC whose UID matches that of the search criterion will respond. This is repeated until there are no collisions.

2 Pseudo-Code for ISO14443A Tag Detection

2.1 Setting Up of Registers

The default configuration after power-up supports ISO15693, single sub-carrier, high data rate, 1-outof- 4 operation. To enter another protocol (ISO14443A in this case), the ISO control register (0x01) has to be written to with the appropriate data byte. For example, to choose an ISO14443A, 106 Kbps protocol, the ISO control register is written with 0x08. All the low level options register (0x02 to 0x0B) are automatically set according to the new protocol.

Next the RF field and receivers should be turned on. This can be done by setting bit B5 in the chip status control (0x00) register. Now the reader is ready to transmit commands to the tag.

2.2 Send REQA Command

There is an option in the ISO control register that determines if the received message (from the tag) contains CRC or not. According to the ISO14443A standards, the ATQA message (which the tag sends in response to the REQA command) does not have any CRC appended to it. Therefore, turn bit B7 in the ISO control register to enable reception without CRC.

Note: The general procedure to start transmission is described below. **This is applicable to all commands that need to be transmitted to the tag.**

The data/command that is to be transmitted is written in to the FIFO, a 12 byte buffer. Transmission starts when the first data byte is written into FIFO. The reader adds SOF, EOF and CRC to the request packet before transmitting.

1. Start condition
2. Send reset command 0x0F (command mode – 0x8F)
3. Send transmission command (0x90 - without CRC or 0x91 – with CRC)
4. Continuous write to register 0x1D (0x3D)
5. Data for register 0x1D (upper and middle nibble of the number of bytes to be transmitted)
6. Data for register 0x1E (lower nibble of the number of bytes to be transmitted)
7. Data byte(s) for FIFO
8. Stop condition

Note that the FIFO can be written to (and read from) in continuous mode only.

For details on the start and stop conditions, refer to the timing diagrams for SPI/Parallel mode.

As mentioned earlier, the SOF, CRC and EOF will be added automatically by the reader. Only the REQA command byte ‘26’ has to be written to the FIFO for transmission.

Pseudo-Code:

buf is an array that holds all the command/data bytes that are to be sent to the reader.

size is the number of bytes to be transmitted. In this case, size = 1.

```
buf[0] = 0x8f;                    /* Reset FIFO command */
buf[1] = 0x90;                    /* send with CRC */
buf[2] = 0x3d;                    /* write continuous from register 1D */
buf[3] = (char) (size >> 8);      /* Data for register 1D */
buf[4] = (char) (size << 4);      /* Data for register 1E */
buf[5] = 0x26;                    /* ISO14443A REQA command byte*/
```

1. Write buf[0] to buf[5] to TRF796x via SPI or parallel mode (refer to the Parallel/SPI timing diagrams in the TRF7960-61 data sheet, SLOU186).
2. Wait for End of TX interrupt.
3. Wait for next interrupt (use a timer for timeout). This can be due to any of the following:
   a. End of RX
   b. Collision

Check the IRQ status register to determine the cause of the interrupt (for more details, refer to the section on Interrupts).

If interrupt is due to End of RX, this means that the response (from the tag) is received in the FIFO without any error/collision. Read the FIFO to obtain the data (ATQA) received from the tag. Start the anti collision procedure.

If interrupt is due to collision, start the anti collision procedure.

2.3 Anti-Collision Sequence

According to the ISO14443A, the ANTICOLLISION command format is as shown below.

Table 1. ANTICOLLISION Command Format

SEL (1 byte)	NVB (1 byte)		UID (0 to 40 bits)
'93' – Cascade level 1	Byte count (upper 4 bits)	Bit count (lower 4 bits)	Search criterion
'95' – Cascade level 2			
'97' – Cascade level 3			

The anti-collision sequence always starts with cascade level 1.

The upper 4 bits of the NVB is called the "byte count" which specifies the number of valid data bytes transmitted by the PCD (including SEL and NVB). Therefore, the minimum value of "byte count" is 2 and maximum value is 7.

The lower 4 bits of the NVB is called the "bit count" which specifies the number of valid data bits (including SEL and NVB) modulo 8.

Initial value of the NVB is 0x20.

The UID field contains parts of the UID (initial value = 0) which is used as a search criterion.

Pseudo-Code:

buf is an array that holds all the command/data bytes that are to be sent to the reader.

NVB is the number of valid bytes and bits.

select is the cascade level.

searchlength is the length of the UID search criterion.

```
buf[0] = 0x8f;                                  /* Reset FIFO */
buf[1] = 0x90 or 0x91;                          /* Transmit with no CRC for ANTICOLLISION command or
                                                   transmit with CRC for SELECT command*/
buf[2] = 0x3d;                                  /* Write continuous to register 0x1D */
buf[3] = 0x00;                                  /* Data for register 0x1D */
buf[4] = NVB & 0xf0;                            /* Data for register 1E */
if ((NVB & 0x07) != 0x00)                       /* Number of complete bytes – Data for reg. 0x1E */
    buf[4] |= ((NVB & 0x07) << 1) + 1;          /* Number of broken bits with Broken byte flag set in reg. 0x1E */
buf[5] = select;                                /* Can be 0x93, 0x95 or 0x97 */
buf[6] = NVB;                                   /* Number of valid bits */
buf[7] to buf[7+searchlength] = UID search criterion
```

1. Write buf[0] to buf[7+searchlength] to TRF796x via SPI or Parallel mode (Refer to the Parallel/SPI timing diagrams in the TRF7960-61 data sheet, SLOU186).
2. Wait for End of TX interrupt.
3. Wait for next interrupt (use a timer for timeout). This can be due to any of the following:
   a. End of RX
   b. Collision

Check the IRQ status register to determine the cause of the interrupt (for more details, refer to Section 3 on Interrupts).

If interrupt is due to collision, read the valid data bytes and bits from the FIFO (refer to Section 3 on Interrupts for more details). This forms the new search criterion. Repeat from step 1 with new NVB and UID until complete UID is obtained.

If interrupt is due to End of RX, this means that the response (from the tag) is received in the FIFO without any error/collision. Read the FIFO to obtain the UID received from the tag.

Combine the known bytes and the received bytes to form the complete UID.

1. Reset bit B7 (B7 = 0) of the ISO control register to enable reception with CRC.
2. Send a SELECT command with the appropriate cascade level, NVB = 0x70 and complete UID.
3. Wait for End of TX interrupt.
4. Wait for End of RX interrupt.

   Read the data (received from the tag) in the FIFO. Examine the SAK field in the tag response. If the cascade bit is set, UID is not complete. Therefore, increase the cascade level and initiate a new anti collision sequence.

Note: Due to the recursive nature of the anti-collision algorithm, there is a risk of stack overflow. It is highly recommended that the user implement stack overflow check in the firmware.

The anti collision loop of the ISO14443A protocol is described in more detail in the flowchart below.

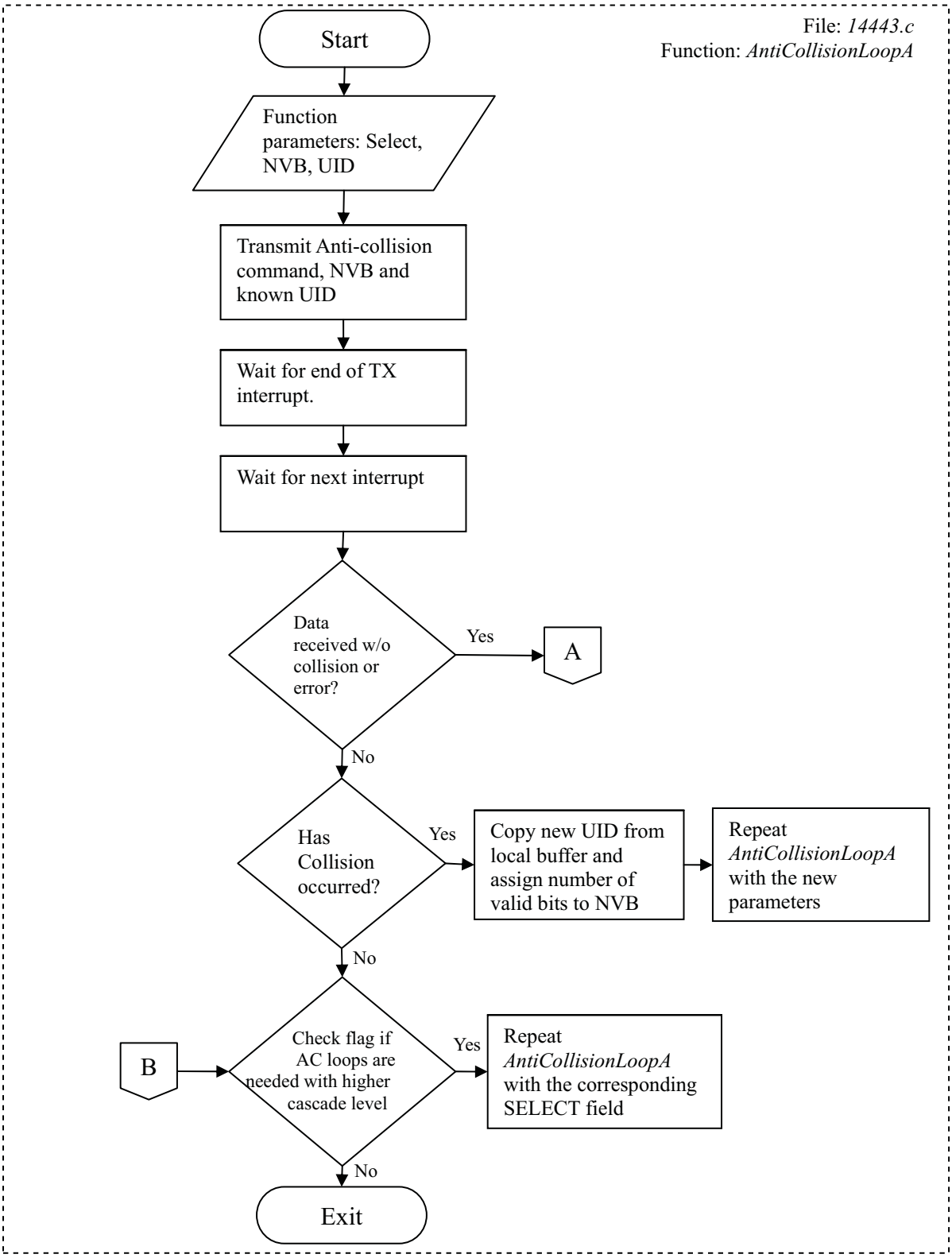

Figure 1. AntiCollisionLoopA (1)

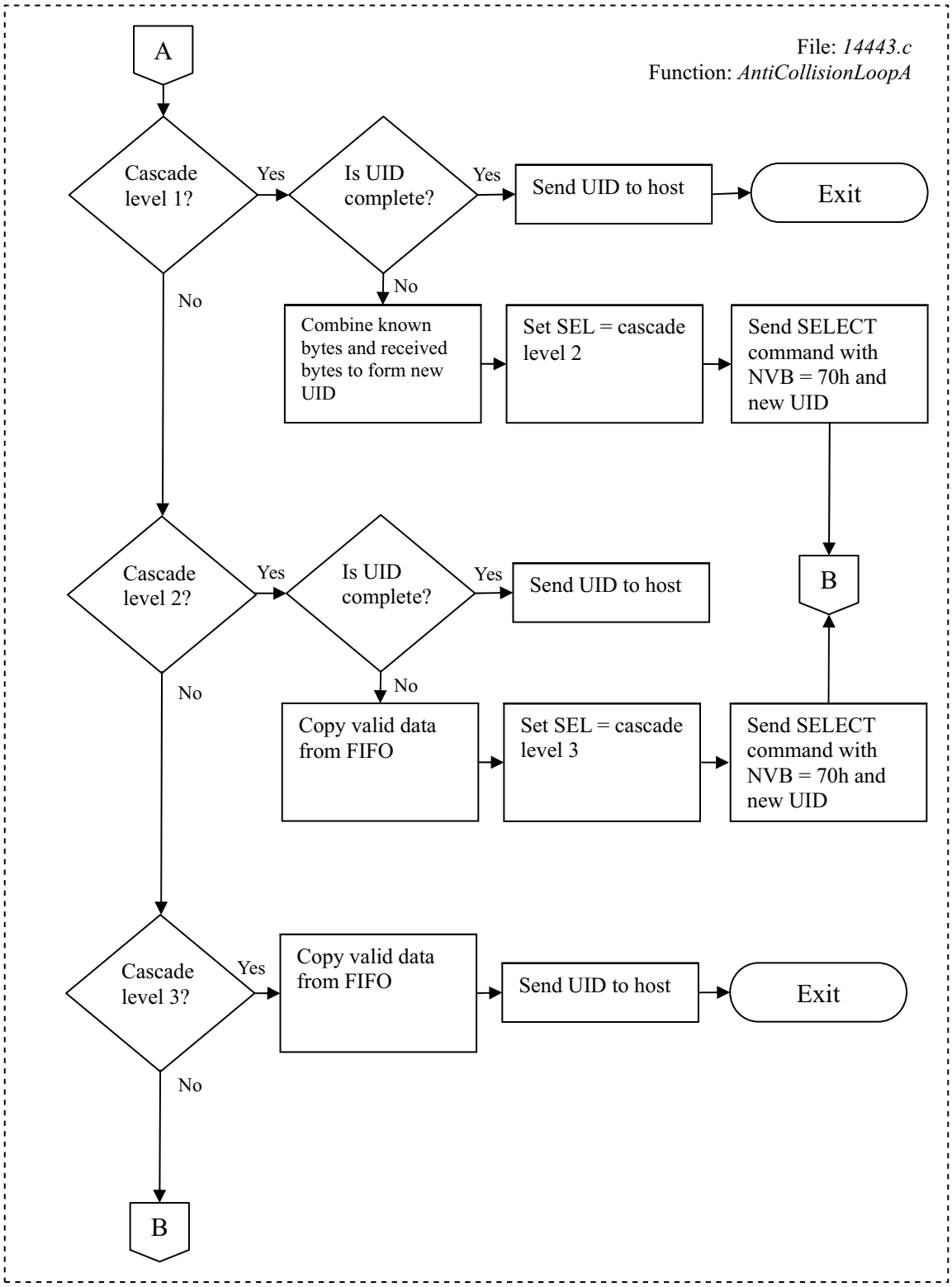

Figure 2. AntiCollisionLoopA (2)

3 Interrupt Handler Routine

The reader which is a slave device has an IRQ pin to prompt/flag the MCU for attention in cases when the reader detects a response from the PICC/VICC. The interrupt handler routine described below determines how the IRQ should be handled.

The TRF796x IRQ status register (Table 3) is read to determine the cause of the IRQ. The following conditions (Table 2) are checked and appropriate actions taken:

Table 2. Interrupt Conditions

NO.	CONDITION	ACTION
1	Transmission complete	Reset FIFO
2	Collision occurred	1. Read collision position register (TRF796x).(1)(2) 2. Determine the number of valid bytes and bits. 3. Read the valid received bytes and bits in FIFO and write to local buffer. 4. Reset FIFO.
3	RX flag set (at End of RX)	1. Read FIFO status register (TRF796x) to determine the number of unread bytes and bits in FIFO. 2. Read the data in FIFO and write to local buffer. 3. Reset FIFO.
4	RX active and 9 bytes in FIFO	1. Read 9 bytes from FIFO. 2. Check if IRQ pin is still high. If yes, go to condition No. 3.
5	CRC error	Set error flag.
6	Byte framing error	Set error flag.
7	No-response time-out	
8	Any other	1. Reset FIFO. 2. Clear interrupt flag.

(1) Though registers 0Dh and 0Eh give the collision position, only register 0Eh is read because the anti-collision command in ISO 14443A is maximum only 7 bytes long. Hence 8 bits are enough to determine the position.

(2) The upper nibble of the collision position register (0Eh) has the byte position and the lower nibble has the bit position within the byte. For example, if the collision position register holds the value 0x40, it means that the collision happened in the 4th byte on bit 0.

Table 3. IRQ Status Register

BIT	BIT NAME	FUNCTION	COMMENTS
B7	Irq_tx	IRQ set due to end of TX	Signals the TX is in progress. The flag is set at the start of TX, but the interrupt request is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX, but the interrupt request is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO is 1/3 > FIFO > 2/3	Signals FIFO high or low (less than 4 or more than 8).
B4	Irq_err1	CRC error	Reception CRC
B3	Irq_err2	Parity error	
B2	Irq_err3	Byte framing or EOF error	
B1	Irq_col	Collision error	For ISO14443A and ISO15693 single sub-carrier
B0	Irq_noresp	No response interrupt	Signal to MCU that next slot command can be sent.

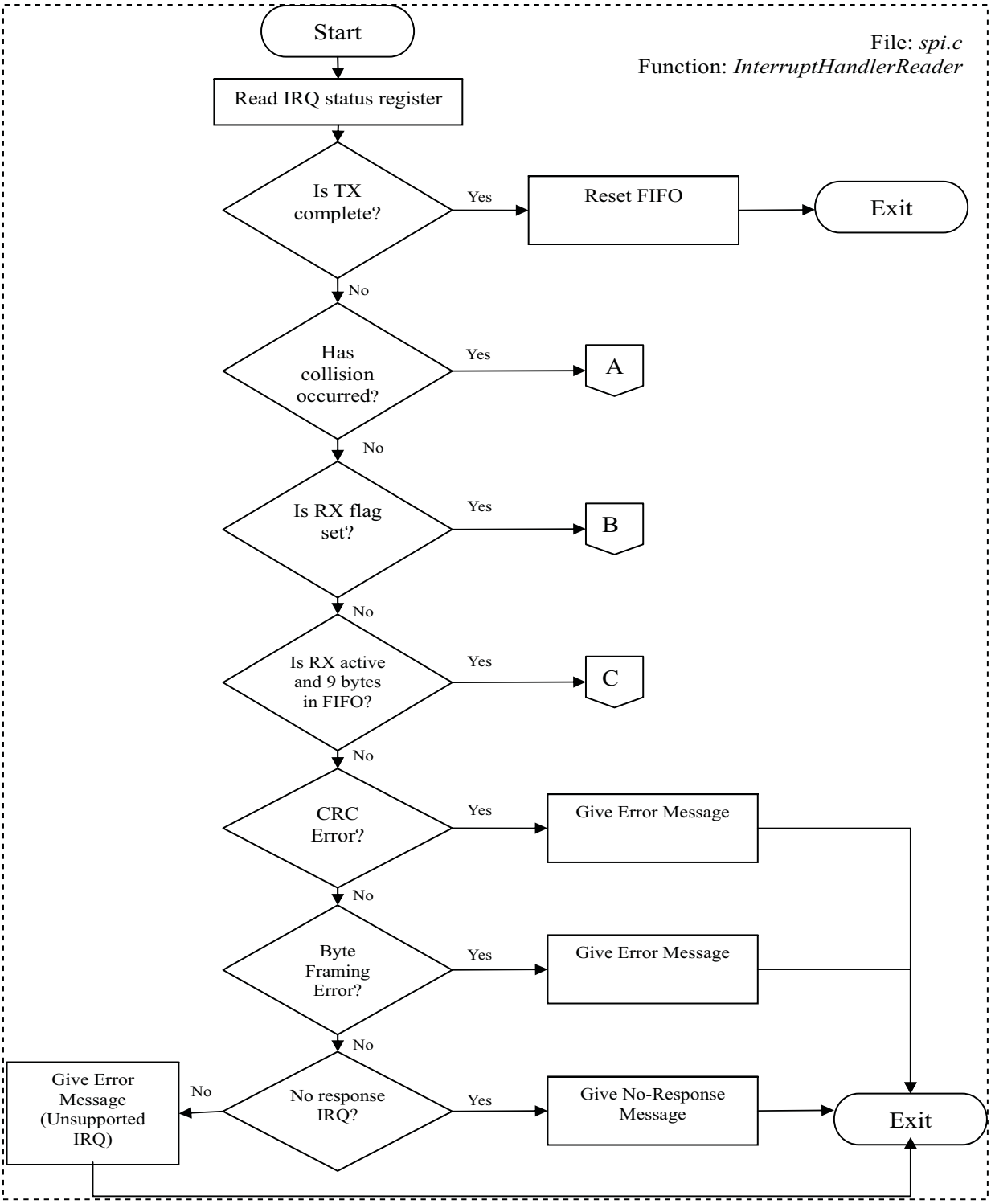

Figure 3. Interrupt Handler Routine (1)

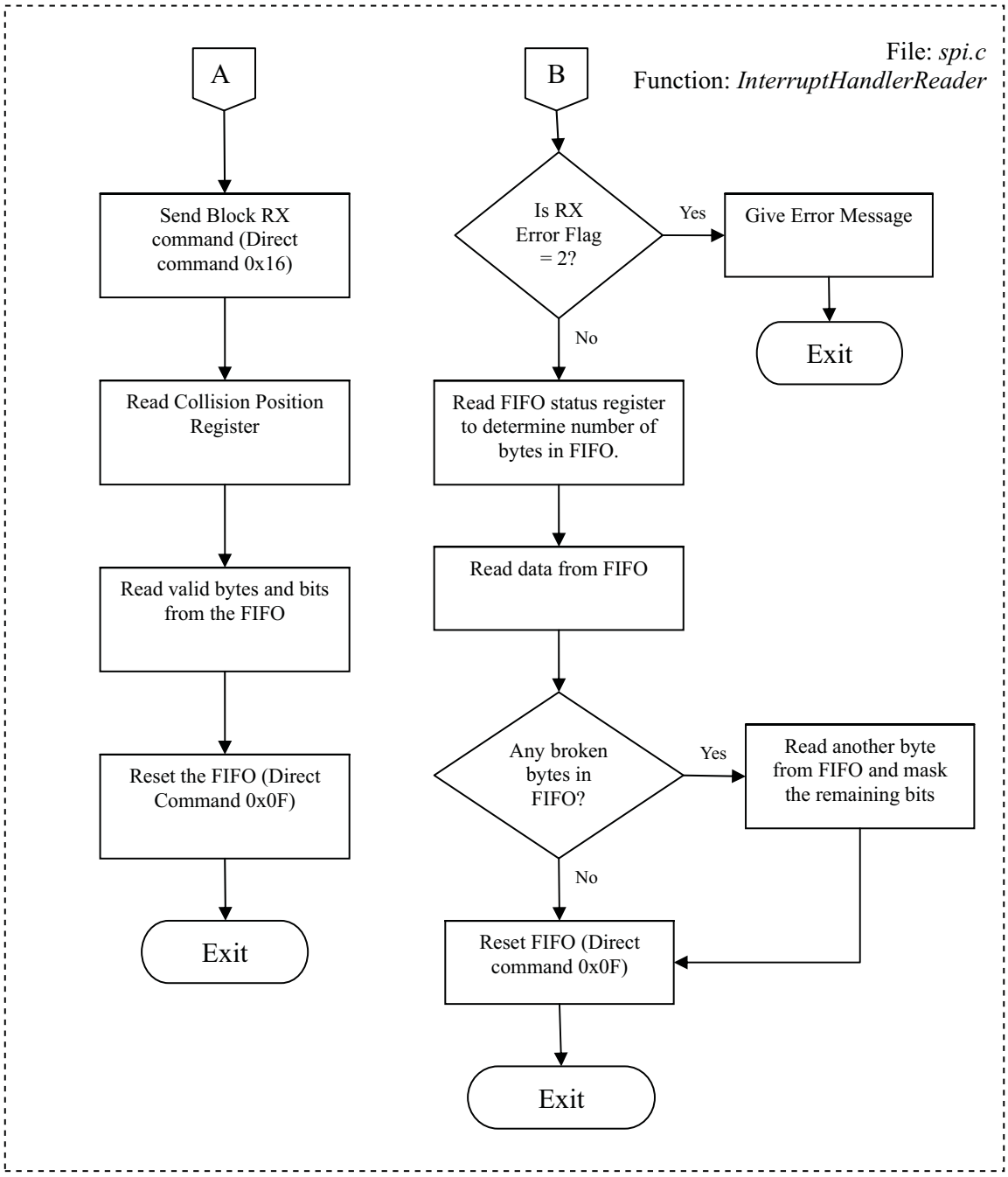

Figure 4. Interrupt Handler Routine (2)

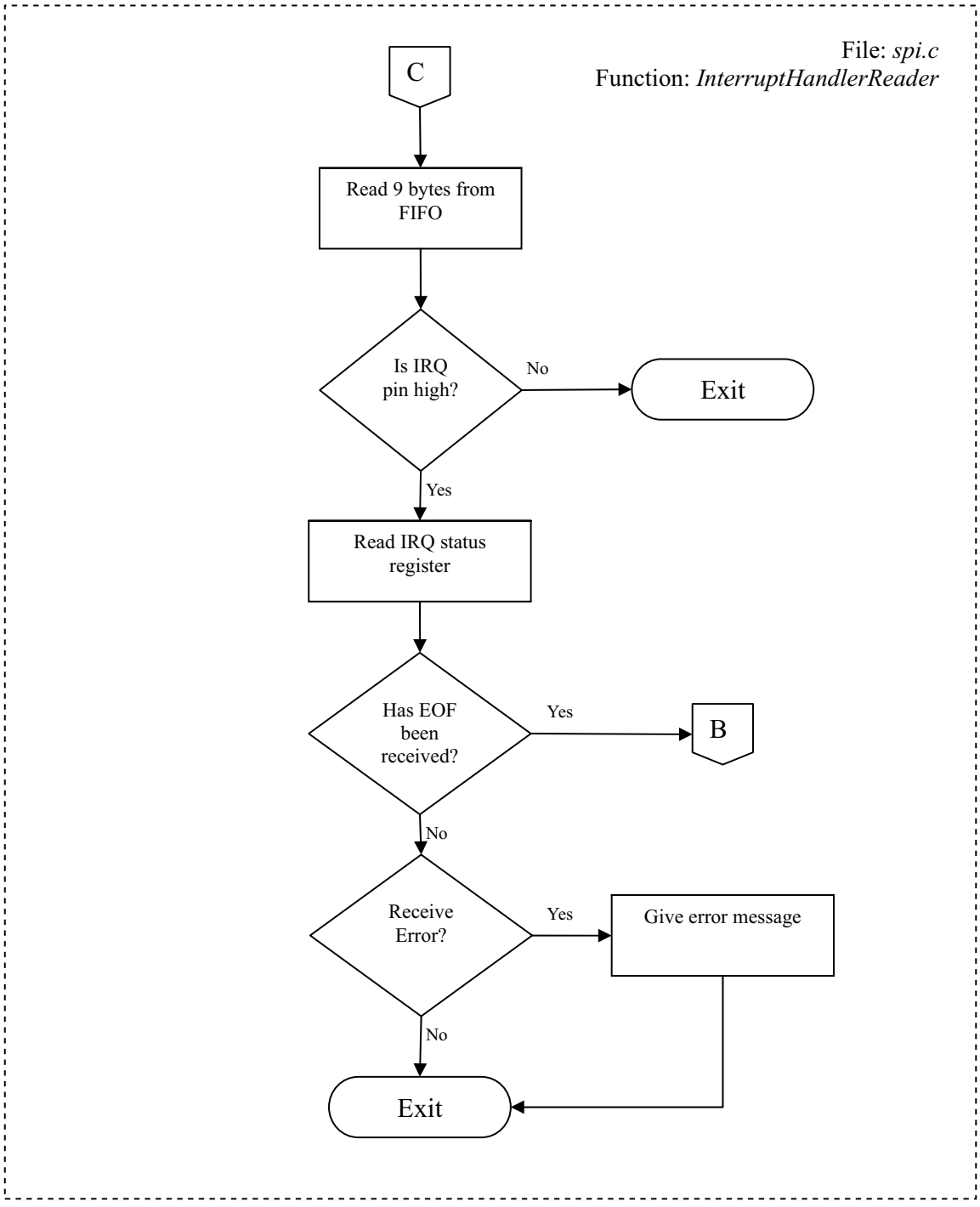

Figure 5. Interrupt Handler Routine (3)

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