

TRF79xxA HF-RFID Reader Layout Design Guide

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ABSTRACT

This application note describes suggested guidelines for use in the laying out the TRF79xxA family of HF RFID readers. As each customer’s implementation will be different, it is the customer’s responsibility to ensure that all the proper methodologies and techniques are followed to ensure optimal performance.

1 Design Guide

Figure 1 shows a sample layout as described in this guide.

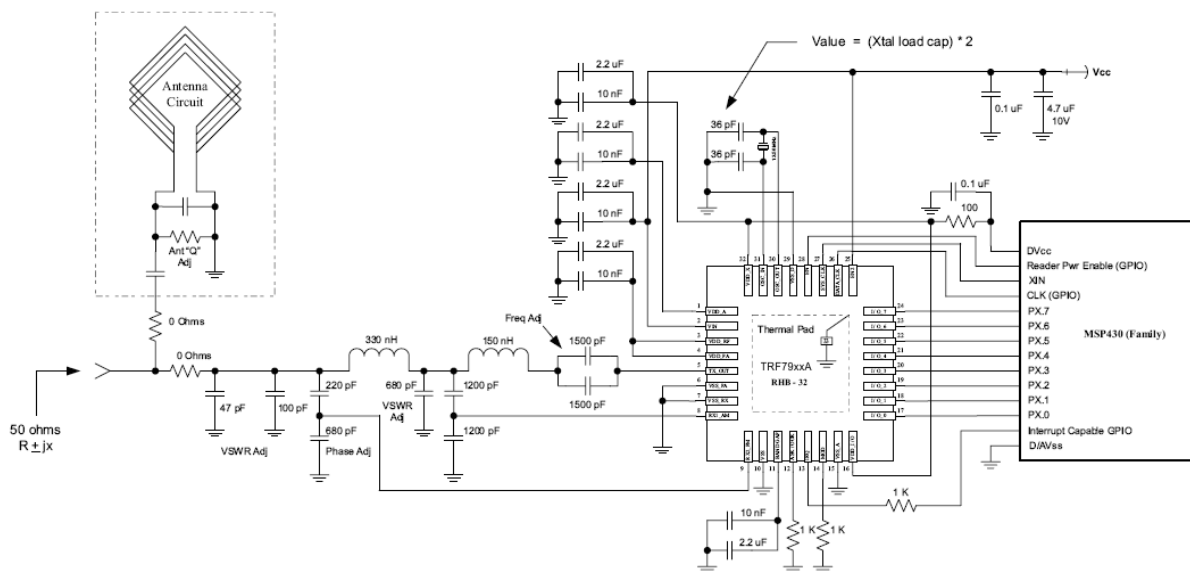
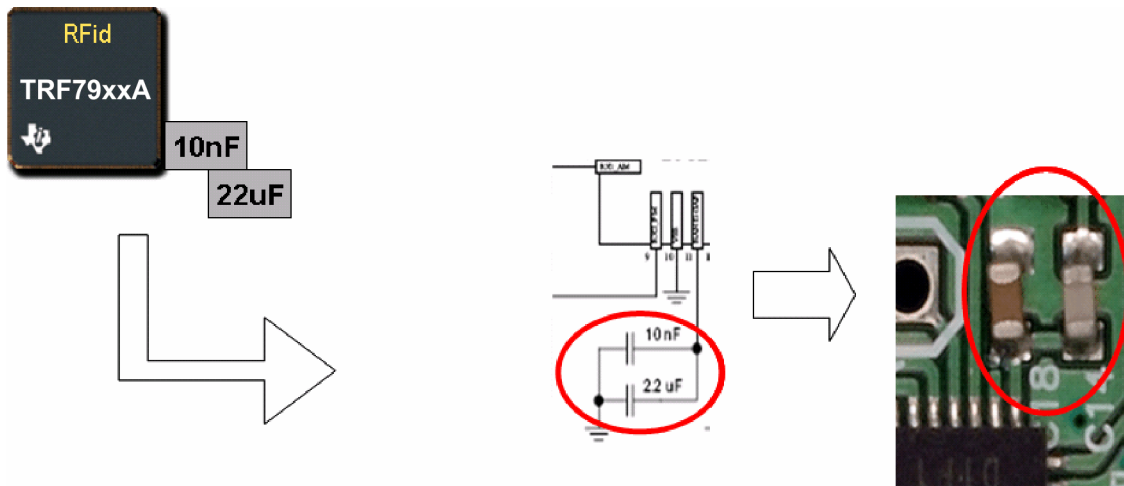


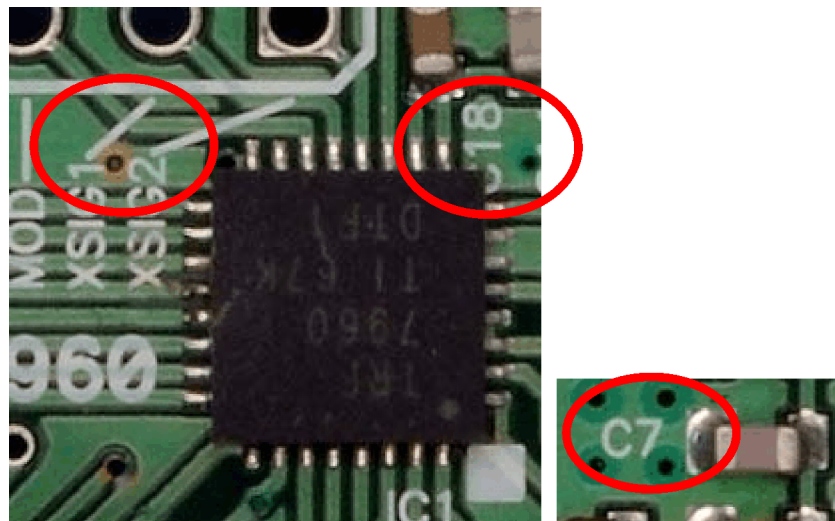
Figure 1. Sample Layout

1. Keep all decoupling capacitors as close to the IC as possible with the high-frequency decoupling capacitor (10 nF) closer than the low-frequency decoupling capacitor (2.2 μ F).

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2. Place ground vias as close as possible to the ground side of the capacitors and the reader IC pins to minimize any possible ground loops.

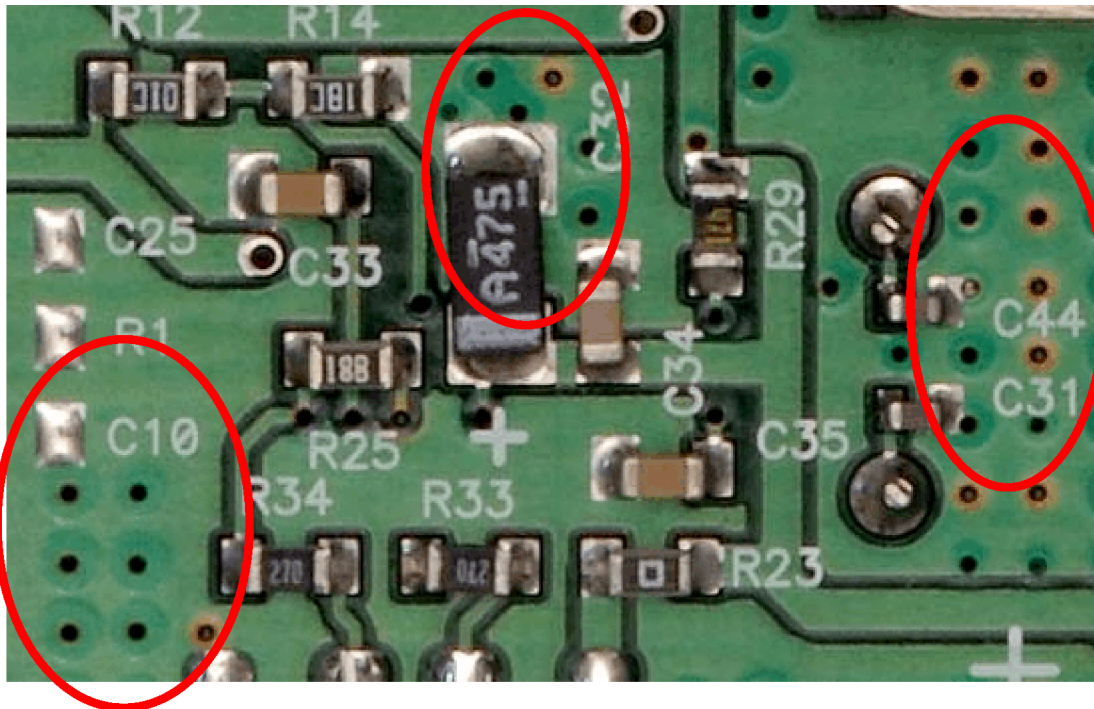


3. Place the two inductors at 90° orientations with respect to each other (that is, if the first inductor is laid out in a horizontal orientation, the next inductor should be placed in a vertical orientation). This arrangement minimizes coupling between the two inductors.



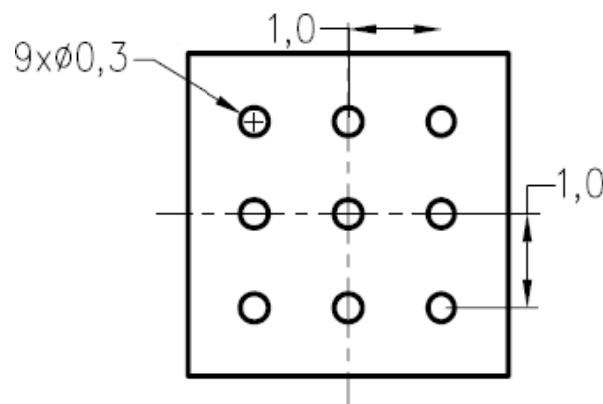
NOTE: TI does not recommend using any inductor sizes below 0603, because the output power can be compromised. If smaller inductors are absolutely necessary, it is up to the customer to confirm output performance.

4. If the crystal is changed from an HC49 to another crystal type, the designer should pay close attention to the internal load capacitance and adjust the two external shunt capacitors accordingly. Follow the recommendations of the crystal manufacturer for those values.
5. There should be a common ground plane for the digital and analog sections. The multiple ground sections or *islands* should have vias that tie the different sections of the planes together.

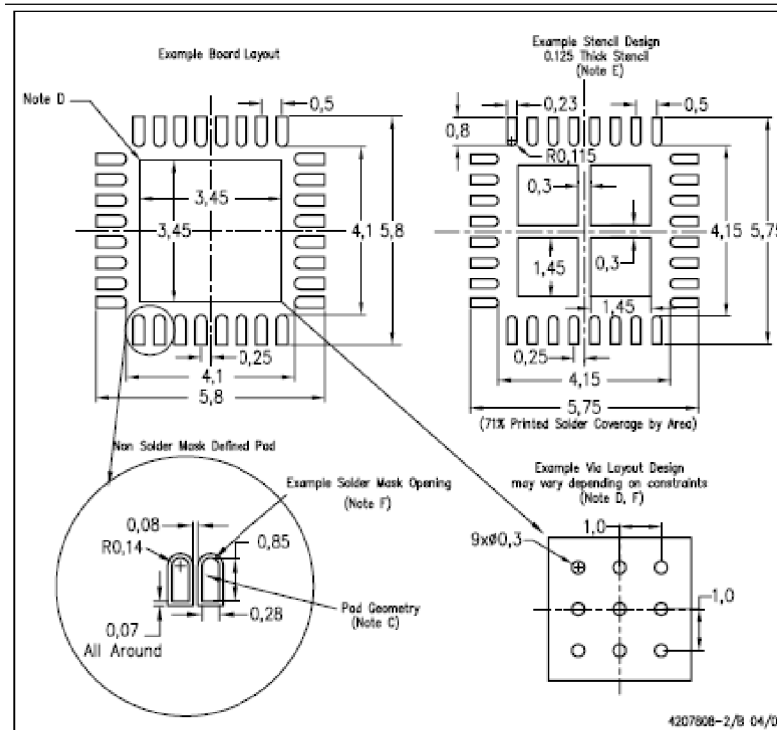


6. Ensure that the exposed thermal pad at the center of the reader IC is properly laid out as specified in the device-specific data sheet (see [Section 2](#)). This helps to dissipate heat away from the IC. The following figures show the suggested layout guidelines for the IC (PCB layout, stencil, and vias).

Example Via Layout Design
may vary depending on constraints

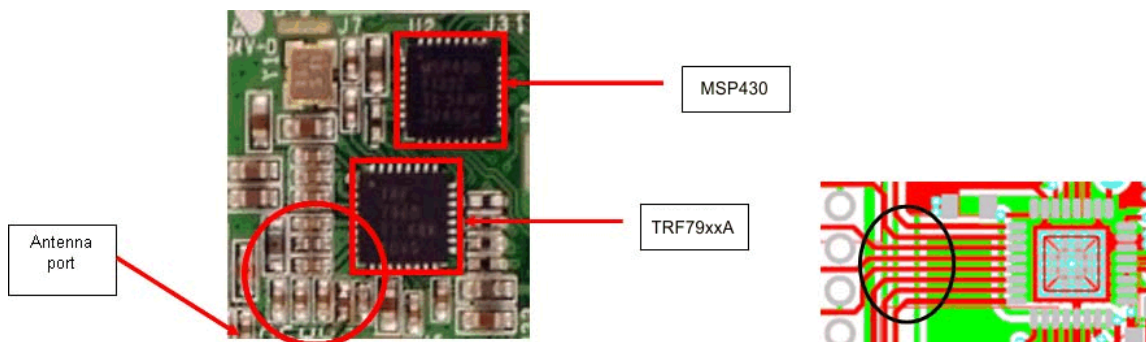


NOTE: The external thermal pad is electrically isolated on the IC. Thus, it could be tied to either a power or ground plane to help dissipate any heat from the package.



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

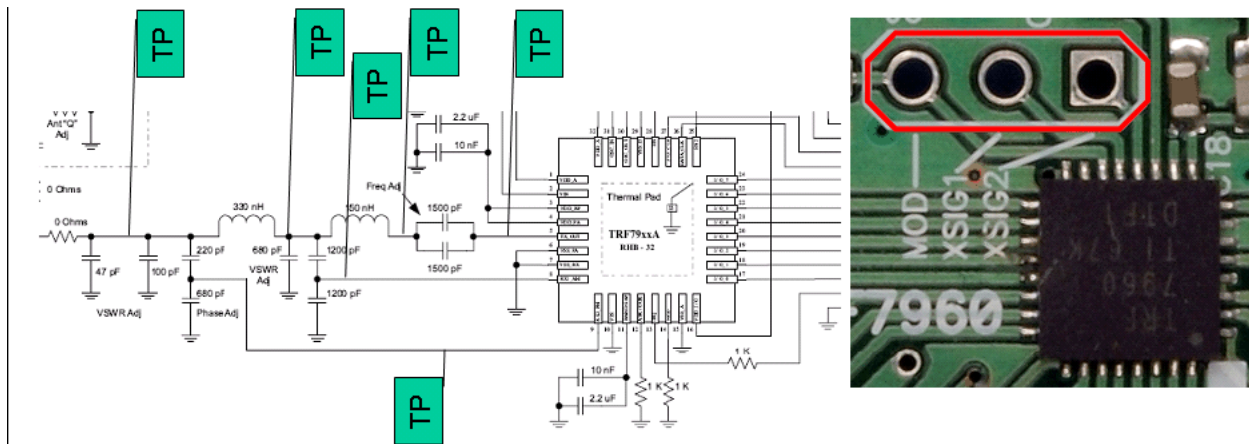
- Trace line lengths should be minimized whenever possible. The RF output path, crystal connections, and control lines from the reader to the microprocessor are the most important. Proper placement of the reader, microprocessor, crystal, and RF connection or connector help to minimize these lengths.



Avoid the following:

- Crossing of digital lines under analog and RF signal lines.
- Crossing of digital lines with other digital lines.
- If the crossings are unavoidable, use 90° crossings to minimize coupling of the lines.

- Depending on the production test plan, consider possible implementations of test pads or test vias for use during testing. The necessary pads or vias should be placed in accordance with the proposed test plan to enable easy access to those test points.



9. If the system implementation is complex (for example, if the RFID reader module is a subsystem of a larger system with other modules such as *Bluetooth*[®], Wi-Fi[®], microprocessors, and clocks), special considerations should be taken to ensure that no noise is coupled into the supply lines.

If needed, special filtering or regulator considerations should be used to minimize or eliminate noise in these unique systems. This helps to ensure optimal RFID reader performance.
10. A suggested reference schematic with the output match from 4 Ω to 50 Ω is provided in the data sheet and the EVM user's guide (see [Section 2](#)). If the customer chooses to follow this suggested schematic, the following conditions should be verified as each implementation will be slightly different.
 - (a) Verify the TX output power
 - (i) If the desired output is detected, then the component and system matches the EVM.
 - (ii) If not detected, then the component value or quality is incorrect.
 - (b) Verify the output impedance
 - (i) If 50 Ω, then the match is correct and maximum power transfer will be achieved.
 - (ii) If not 50 Ω, then it will require tuning of the output to obtain a 50-Ω output match. When this is achieved, you will achieve maximum power transfer.
11. Avoid crossing of digital lines under RF signal lines. Also, avoid crossing of digital lines with other digital lines whenever possible. If the crossings are unavoidable, use 90° crossings to minimize coupling of the lines.

2 References

1. *TRF7970A Multiprotocol Fully Integrated 13.56-MHz RFID and NFC Transceiver IC* ([SLOS743](#))
2. *TRF7964A Multiprotocol Fully Integrated 13.56-MHz RFID Reader and Writer IC* ([SLOS787](#))
3. *TRF7963A Fully Integrated 13.56-MHz RFID Reader/Writer IC, ISO14443A,B/NFC* ([SLOS758](#))
4. *TRF7962A Fully Integrated 13.56-MHz RFID Reader/Writer IC, ISO15693/ISO18000-3* ([SLOS757](#))
5. *TRF7960A Multiprotocol Fully Integrated 13.56-MHz RFID Reader/Writer IC* ([SLOS732](#))
6. *TRF7970A Evaluation Module (EVM) User's Guide* ([SLOU321](#))

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 30, 2009 to April 18, 2016

Page

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- Changed all instances of TRF796x to TRF79xxA, including in the document title 1
 - Added [Section 2, References](#) 5
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