# TPIC6595 Power+ Logic™ Eight-Bit Shift Register With Low-Side Power DMOS Switches

TEXAS
INSTRUMENTS

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## Introduction

The TPIC6595 is a monolithic Power+ Logic™ device that contains eight 1.5-A peak/45-V low-side DMOS power switches packaged in a 20-pin dual-in-line plastic package. The logic functions of the TPIC6595 consist of the logic functions existing in the high-speed CMOS (HCMOS) SN74HC595 catalog parts except the outputs are inverted relative to the HCMOS version. The eight DMOS switches are controlled from a single input, SER IN (serial input), and by an 8-bit serial word. Data is transferred through an 8-bit shift register on the rising edge of SRCK. SER OUT is provided at the last bit of the shift register to allow cascading in applications requiring more than eight DMOS switches.

Each of the eight DMOS switches are equipped with an internal 45-V drain-to-gate zener clamp that greatly enhances their capability to switch unclamped inductive loads. Since the zener clamp causes the DMOS switch to be forward biased instead of being avalanched during inductive-load turn off, a power switch avalanche energy rating of 75 mJ maximum is achieved.

This device provides a cost-effective single-chip solution for direct control of motors, relays, solenoids, and other high-energy, high-electrical stress loads including lamps. Since the device implements a direct control link between the microcontroller and the system electrical loads, use of multiple logic integrated circuits and discrete power devices are eliminated. The reduction of discrete devices not only reduces cost, but saves circuit space and improves system reliability by the reduction of active components.

## Functional Description

The TPIC6595 is an 8-bit serial-in-to-parallel-out power driver having separate power and logic ground pins. A functional block diagram is shown in Figure 1. Data is transferred through an 8-bit shift register on rising edges on SRCK. The data in the shift register is latched to the outputs by the rising edge on RCK. All outputs are placed in a high-impedance mode with a high level on $\overline{G}$, but the data is not cleared from the storage register latches. $\overline{SRCLR}$ clears all data in the shift register only. SER OUT is provided at the last bit of the shift register to allow for cascading in applications requiring more than eight output bits.

The logic used is specified within the data sheet to operate from 4.5 V to 5.5 V, but it is capable of operation down to 3 V and up to an absolute maximum voltage of 7 V. The CMOS transistors used in the digital logic have small feature sizes and short channel lengths as well as tightly controlled, low threshold voltages. Due to these characteristics, the CMOS gains are high, and the parasitic capacitance is minimized. Because of this, the logic is able to function at greater than 25-MHz operation over the full $V_{CC}$ range of 3 V to 7 V and over the temperature range of –40°C to 125°C. Another result of using primarily CMOS-type transistors in the design of the power logic is a low quiescent current ($I_{CC}$).

The predrive circuitry is a CMOS buffer stage that provides adequate sink/source drive to the gate of the output power DMOS. A series resistor has been added between the buffer stage and the gate of the DMOS in order to provide a more controlled gate-drain capacitor charging current than could be achieved with a CMOS buffer alone. The current-limit resistor serves two purposes: first, it limits power dissipation in the drain-to-gate zener clamp structure under inductive transient conditions, and second, it controls the voltage rise and fall of the DMOS gate. This reduces radio frequency interference (RFI) during output switching. The rise and fall times at the gate are controlled by the effective RC time constant, which consists of the series resistor and the $C_{iss}$ of the DMOS.

The DMOS outputs are designed to have a typical static drain-source on-state resistance of 1.3 Ω with a continuous output current of 250 mA at 25°C and $V_{CC}$ of 5 V. The DMOS transistors are designed to have

a low threshold voltage. The low threshold voltage along with the high gain of the devices allow the gates to be driven without the aid of any additional supply voltage above $V_{CC}$. Thus a charge pump or additional level shifting voltage supply is not necessary. The elimination of a charge-pump circuit reduces turn-on times, thereby minimizing power dissipation in the outputs during switching. The use of a charge pump also increases the susceptibility of generating RFI due to the need for an internal oscillator. An oscillator provides little interference due to its low power, but the DMOS may serve as a transconductance amplifier for the oscillator circuit, especially when switching small resistive loads.

Variation of the output characteristics is primarily a function of temperature and $V_{CC}$. With the CMOS predrive buffer used, the $V_{GS}$ of the output DMOS varies directly with $V_{CC}$. A typical $r_{DS(on)}$ of 1.8 $\Omega$ at 25°C can be achieved with a $V_{CC}$ of 3 V. This low static drain-source on-state resistance is directly attributable to the low DMOS threshold voltage in the process. Output $r_{DS(on)}$ primarily consists of the intrinsic DMOS resistance, the series resistance of the source and drain lead busing, bonding resistance, and lead frame resistance. All of these resistances have a positive temperature coefficient.
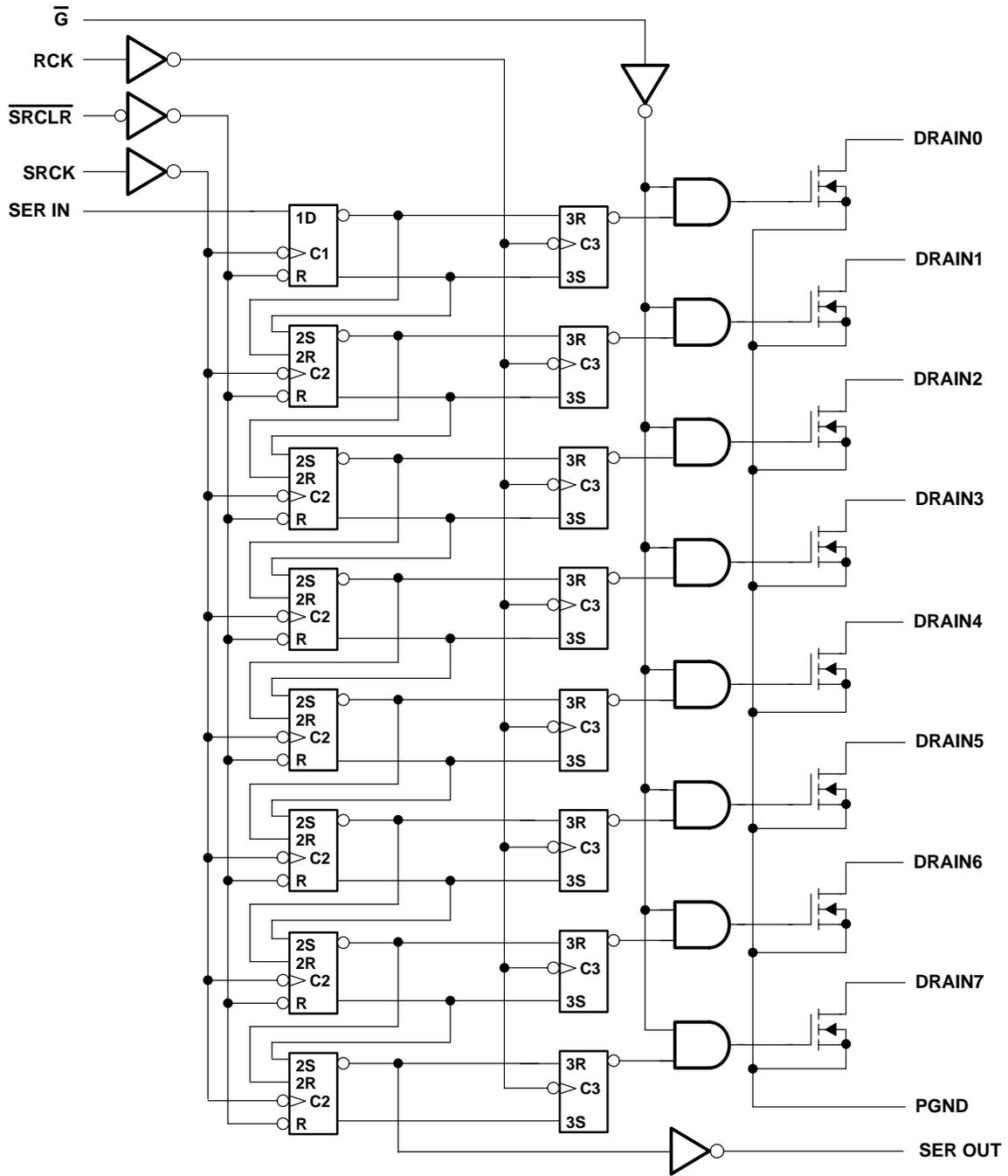
**Figure 1. Functional Block Diagram**

# Application Design Considerations

## Power and Thermal Considerations

Three important application considerations for a power device are the power, thermal, and inductive energy ratings with respect to the operational load demands. The following illustrate analytical approaches that ensure that the device is operating within these maximum ratings.

To calculate the current $I_D$ for a single output with n outputs conducting equal current, use equation (1)

$$I_D = \sqrt{\frac{T_J - T_A}{R_{\theta JA} \times r_{DS(on)} \times 8}} \ K_n \tag{1}$$

Where:

$K_n$ = current coefficient for the current of a single output with n outputs simultaneously conducting equal current

$R_{\theta JA}$ = thermal resistance or junction-to-ambient, 90°C/W

$r_{DS(on)}$ = static drain-source on-state resistance at 150°C (worst case) 3.5 Ω

$T_J$ = junction operating temperature, °C

$T_A$ = operating ambient temperature, °C

**Table 1. Values for the Current Coefficient $K_n$**

| Total Outputs On<br>n | Current Coefficient<br>$K_n$ |
|:---:|:---:|
| 1 | 2.67 |
| 2 | 1.95 |
| 3 | 1.61 |
| 4 | 1.40 |
| 5 | 1.26 |
| 6 | 1.50 |
| 7 | 1.07 |
| 8 | 1.00 |

The current coefficient values, $K_n$, shown in Table 1 are derived from the thermal model shown in Figure 2 and the TPIC6595 data sheet thermal resistance values.
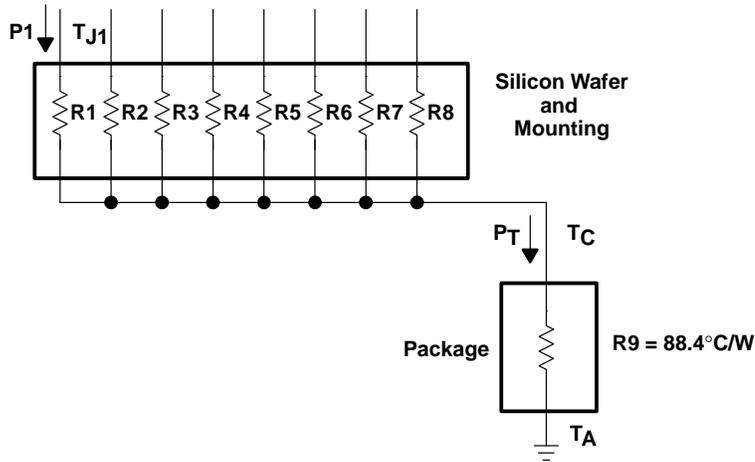
**Figure 2. Thermal Model-Thermal Equilibrium, No Heat Sink**

The following equations apply for the thermal model in Figure 2:

R1 || R2 || R3 || R4 || R5 || R6 || R7 || R8 + R9 = 90°C/W
R1 || R2 || R3 || R4 || R5 || R6 || R7 || R8 = 1.6°C/W
$R_{n, n = 1–8}$ = 12.8°C/W
R9 = 88.4°C/W
$T_{J(n)}$ = junction temperature of an individual output with n outputs conducting equal current
P1 = P2 = P3 = P4 = P5 = P6 = P7 = P8

Therefore:

$$T_{J(n)} \ = \ P1R1 \ + \ nP1R9 \ + \ T_A$$

From the thermal model in Figure 2, P1 can be calculated using equation 1.

$$P_1 \ = \ \frac{T_{J(n)} \ - \ T_A}{R1 \ + \ nR9} \ = \ I_D{}^2 \ r_{DS(on)} \ = \ I_D{}^2 \ 3.5 \ \Omega \tag{2}$$

## Switching Unclamped Inductive Loads and Turn-Off Power Dissipation, $P_{OFF}$

The data sheet shows an energy rating of 75 mJ. This energy rating is a specific point on the curve shown in Figure 5 on the data sheet, which is repeated here as Figure 3 for clarity.

The energy capability of the device in Figure 3 is not described in a traditional manner but as a graph of peak-switching current versus avalanche time for a starting junction temperature of 25°C.
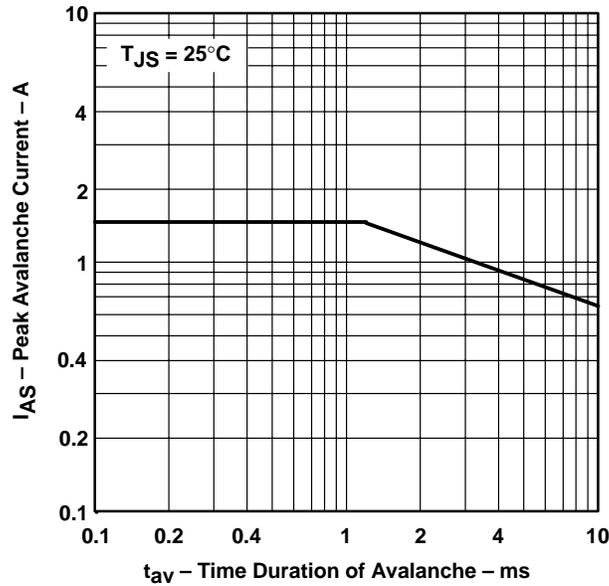
Figure 3. Peak Avalanche Current Versus Time Duration of Avalanche

It has been established that the energy limitations of these devices during inductive switching is due to the self heating of the silicon structure. Figure 4(a) shows the measurements of the peak-switching current versus starting junction temperature and idealized inductive switching waveforms. The power absorbed by the device during switching is proportional to the peak switched current, $I_{av}$. If the failure mechanism is thermal, the power capability of the device is related to the transient thermal impedance, starting temperature of the device, and maximum physical temperature that the silicon can withstand. It is well known[1] that for the typical resistivities used in the manufacture of these devices, the maximum temperature that silicon can operate at is in the range of 400°C. Therefore, if the peak switching temperature is plotted as a function of starting temperature, the relationship should be linear and intercept the temperature axis at 400°C. Study of Figure 4(a) shows that the 0.5-ms line has an intercept with the starting temperature is directly attributable to the zener diode that has been integrated between the drain and the gate of the device. The zener diode forces the whole DMOS structure to be active during voltage clamping and therefore gives the maximum possible energy absorption capability.

As a consequence of a thermally-limited failure mechanism, the concept of a single energy rating for the device does not fully characterize its capabilities, since the maximum energy capability is related to the time duration over which the energy is absorbed. Consequently, the inductive switching energy characterization of the TPIC6595 has been expanded to show peak switching current, $I_{as}$, versus avalanche time for the device, $t_{av}$.

The equation, $|V| = L\, di/dt$, can be used to relate this curve to a practical application circuit. Given a supply voltage, $V_{DD}$, and an internal clamp voltage of $V_{BR(DSX)}$ the avalanche time, $t_{av}$, is given by $(V_{(BR)DSX} - V_{DD})/L$, and the peak switching current $I_{av}$ is simply the maximum current at switch off.

[1]Physics of Semiconductor Devices, Second Edition. Sze. John Wiley & Sons, pp. 19–26.
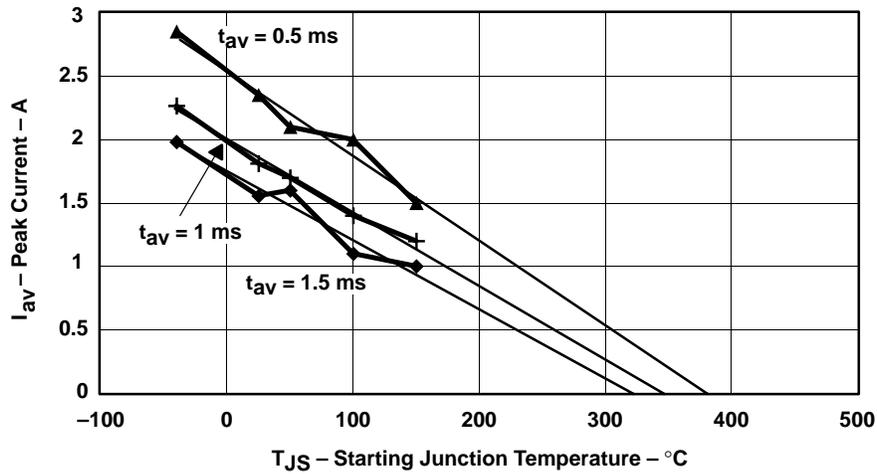
**(a) PEAK SWITCHING CURRENT VERSUS JUNCTION TEMPERATURE**
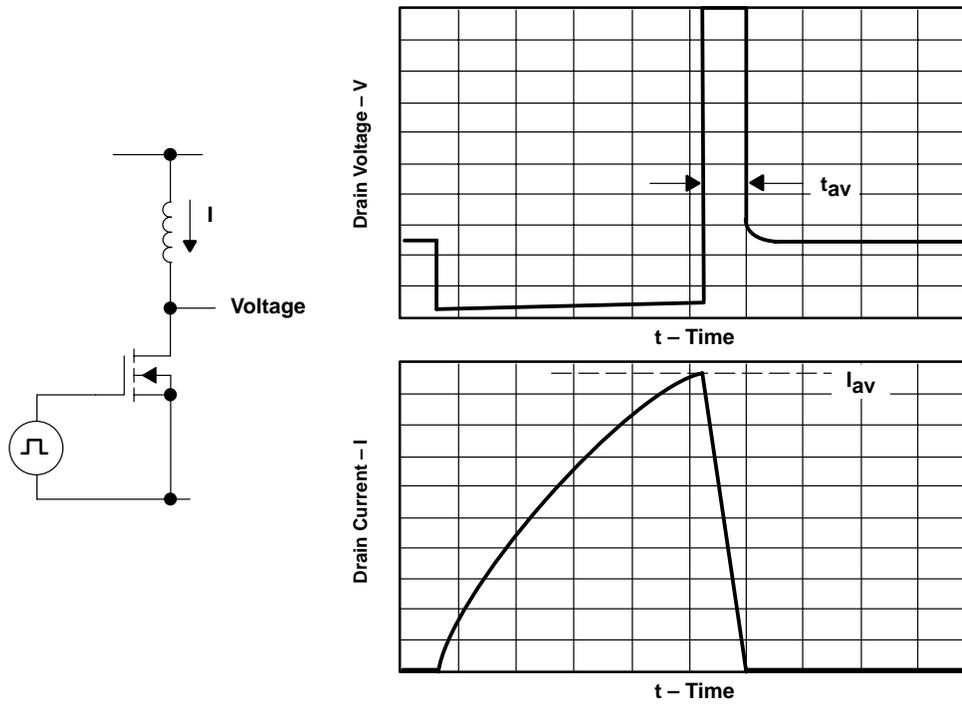


**(b) IDEALIZED INDUCTIVE SWITCHING WAVEFORMS**

**Figure 4.  Peak Switching Current Versus Starting Junction Temperature**

If the maximum power dissipation of the device is not exceeded, it is possible to drive an inductive load by operating a number of the devices in parallel. This is due to the close matching of the gate-drain zener diodes.

Figure 5(a) shows four switches operating in parallel while driving a 105-mH/11.5-$\Omega$ load at 1 A. The power absorbed during switching is often greater than the power dissipated during the on period.

$$E_{off} = \frac{3L_H I_{DM}{}^2 BV_{(BR)DSX}}{\left[6(V_{(BR)DSX} - V_{DD}) + 4R_L I_{DM}\right]} \qquad (3)$$

Where:

| | | |
|---|---|---|
| $E_{off}$ | Total energy absorbed by TPIC6595 during turn-off transient | 59.6 mJ |
| f | Switching frequency | 25 Hz |
| $L_H$ | Load inductance | 105 mH |
| $I_{DM}$ | Peak output load current | 1 A |
| $P_{off}$ | Turn-off power dissipation | 1.26 W |
| $R_L$ | Inductor resistance | 11.5 $\Omega$ |
| $V_{(BR)DSX}$ | Clamp voltage | 45 V |
| $V_{DD}$ | Load supply voltage | 13 V |

$$P_{off} = E_{off}f = 1.49 \text{ W} \qquad (4)$$

In the above example, switching frequency of only 25 Hz can result in a power dissipation that is greater than the package rating device. If it is assumed that $T_A = 25°C$ and $T_J = 150°C$, the maximum power dissipation, $P_{max}$, is given by

$$P_{max} = (T_{Jmax} - T_A)/R_{\theta JA}$$

Where:

    $T_{Jmax}$ is the maximum junction temperature,
    $T_A$ is the ambient temperature, and

    $R_{\theta JA}$ is the thermal resistance.

Thus,

    $P_{max}$    $= (150 - 25)/90 = 1.39$ W and at a switching speed of 25 Hz,
    $P_{off}$     $= 59.6 \text{ mJ} \times 25 \text{ Hz} = 1.49$ W

The above example demonstrates that the power dissipation associated with load turn off is often significantly greater than during the on period.
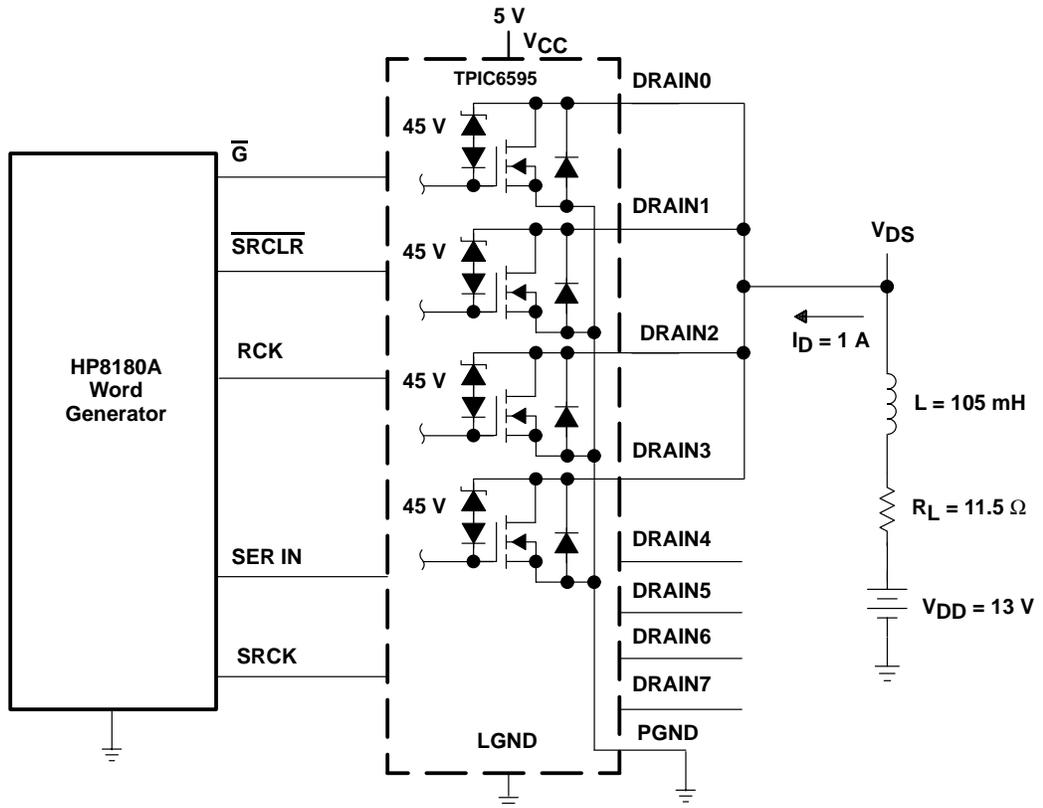
**(a) POWER SWITCHES CONNECTED IN PARALLEL**
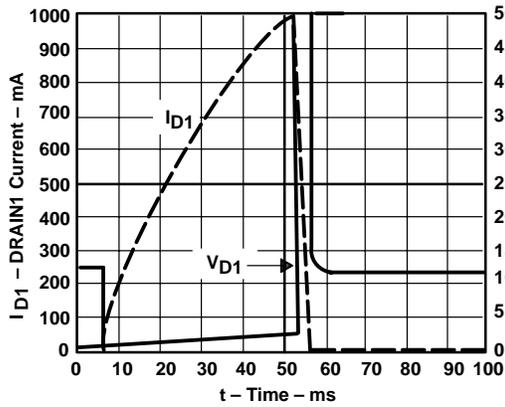


**(b) FULL CYCLE INDUCTIVE LOAD SWITCHING**
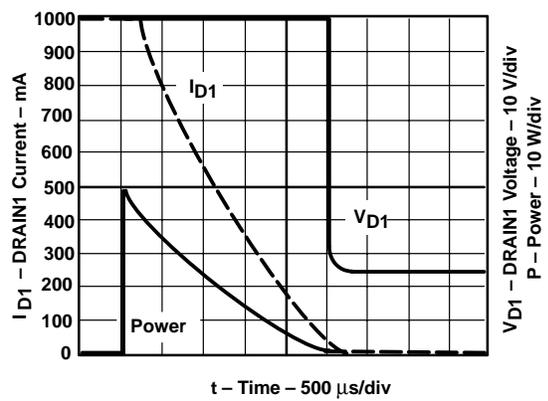


**(c) TURN-OFF INDUCTIVE LOAD SWITCHING**

**Figure 5.  Power Switches Connected in Parallel**

## Parallel Operation of Output Switches for Extended Current Capability

If all eight output switches are not needed for an application and a continuous output load current greater than 0.25 A is required, the switches can be connected in parallel for extended current capability. The current-sharing capability of the switches is demonstrated in a circuit while operating at $T_A = 40°C$ (see Figure 6). The individual switch current, $I_D$, is determined by equation (5).
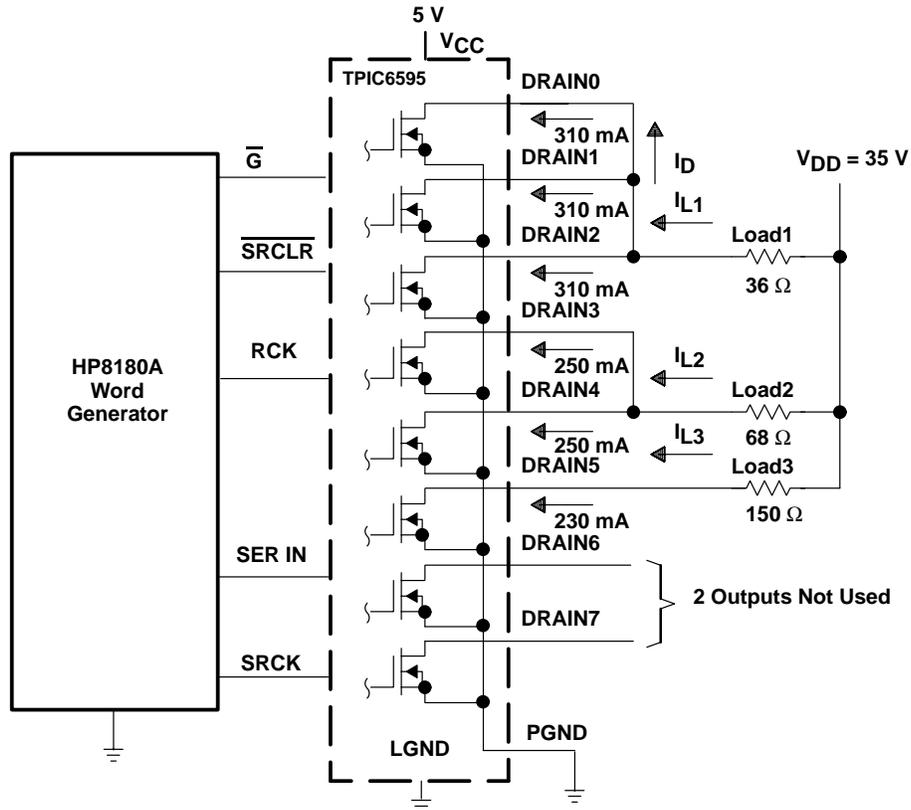


**Figure 6. Parallel Operation of Output Switches for Extended Current Capability**

$$I_D = \sqrt{\frac{T_J - T_A}{R_{\theta JA} \times r_{DS(on)} \times 8}} \; K_n \tag{5}$$

$K_n$ = current coefficient = 1.5, 6 outputs on

Where:

$$I_D = \sqrt{\frac{150°C - 40°C}{90°C \times 3.5 \; \Omega \times 8}} \; K_n$$

$I_D$ = 0.209 A × 1.5 = 0.313 A each switch
$I_{L1}$ = 3 X $I_D$ = 0.940 A max current for Load1
$I_{L2}$ = 2 X $I_D$ = 0.627 A max current for Load2
$I_{L3}$ = 1 X $I_D$ = 0.313 A max current for Load3

# Application Design Examples

## Direct Drive of Eight Lamps

Figure 7 shows the TPIC6595 circuit simultaneously switching eight No. 194 automotive lamps from a 14.3-V source and various waveforms, which demonstrate the internal current limiting at approximately 1.8 A.



**(a) LAMP SWITCHING TEST CIRCUIT**



**(b) INITIAL LAMP IN-RUSH CURRENT**



**(c) HOT FILAMENT LAMP CURRENT**
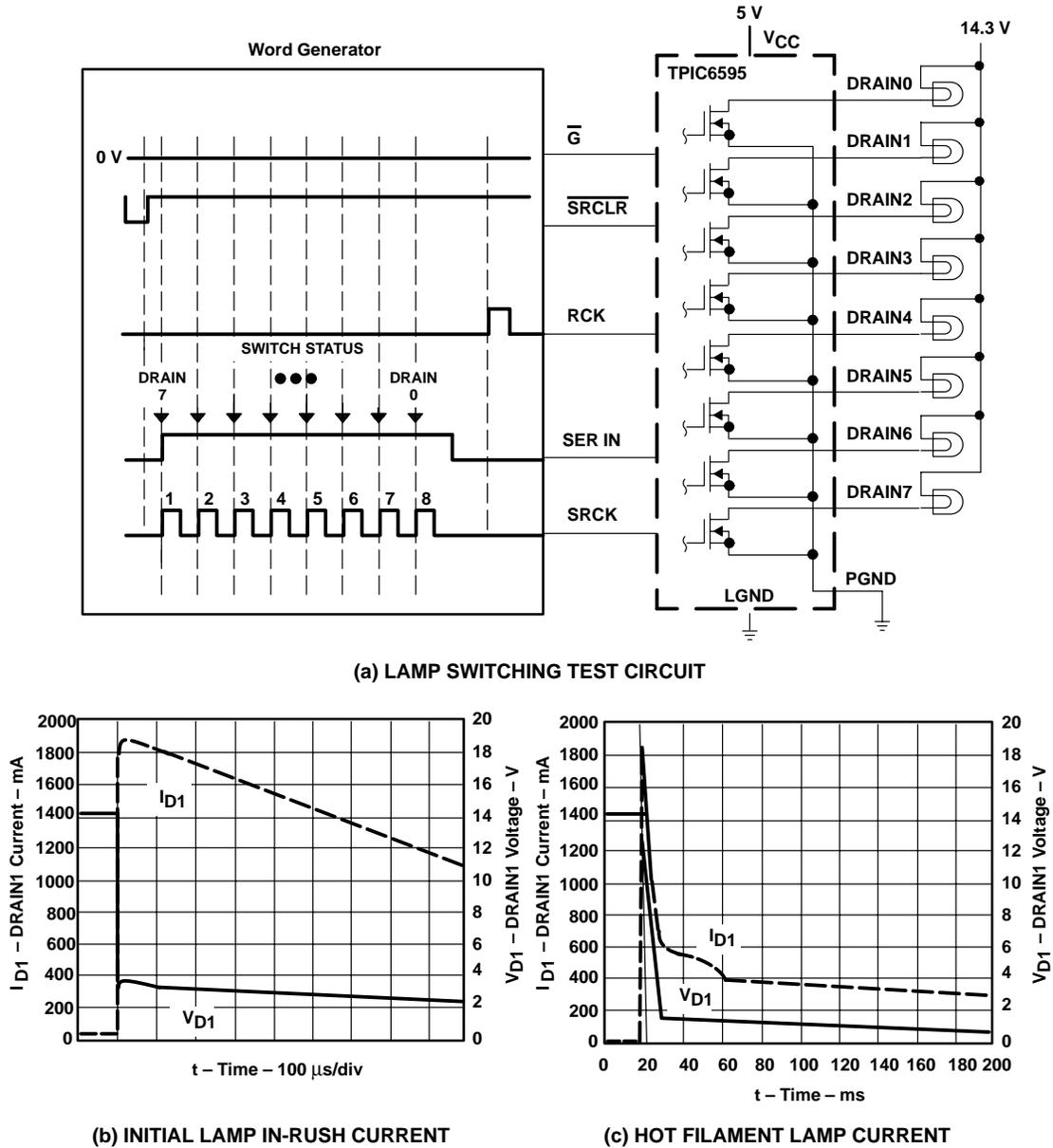
**Figure 7.  Simultaneous Switching of Eight Lamps**

The nature of an incandescent lamp is capacitive during turn on and represents an instantaneous short circuit. Previous measurements have indicated that the in-rush current (peak switching current) of the incandescent bulbs shown in Figure 7 is typically 2.6 A. As shown on the previous page, the TPIC6595 limits this current to approximately 1.8 A.

### Direct Drive of Eight Relays

The worst-case power dissipation for continuous operation of all outputs is calculated as 0.438 W based on the device measurements.

Maximum $r_{DS(on)} = 3.5\ \Omega$ ($T_J = 150°C$):
$$I_{rms} \approx 0.125\ A \text{ (see Figure 9)}$$
$$P = I_{rms}^2 \times r_{DS(on)} \times 8 \text{ outputs on}$$
$$P = (0.125\ A)^2 \times 3.5\ \Omega \times 8 = 0.438\ W$$

The power dissipation created by inductive energy is insignificant in this case because the resistance component of the load is large compared to the inductance. Based on $R_{\theta JA} = 90°C\ /\ W$ and $T_J = 150°C$, the maximum permissible ambient operating temperature ($T_J$) for driving the eight relays at continuous operation is 110°C.

$$T_A = T_J - PR_{\theta JA} = 150°C - 0.438 \times 90°C$$
$$= 110°C$$
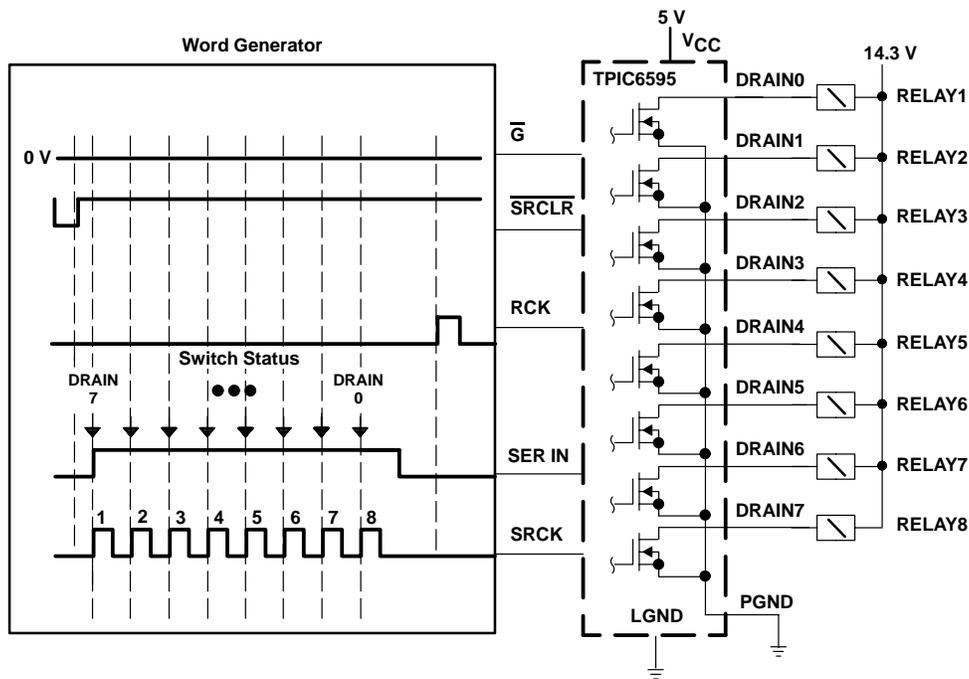


**Figure 8.  Simultaneous Switching of Eight 12-V, 10/20-A Relays**
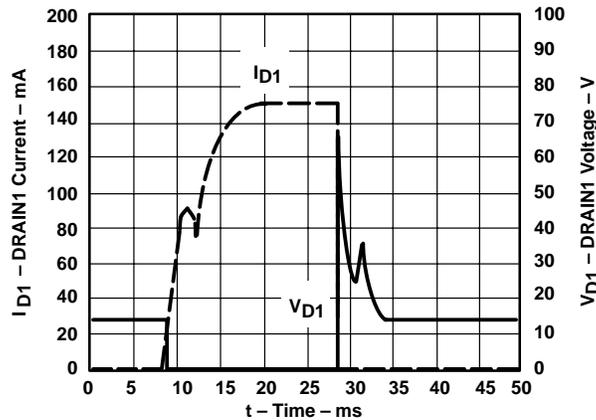
**Figure 9. DRAIN1 Voltage and Current Waveforms of Figure 8 Application Circuit**

## Unipolar Stepper Motor Drive

Stepping motors, due to their digital drive requirements, are natural motion providers for microprocessors or ASIC-based systems. The TPIC6595 provides a simple solution to the problem of translating logic-level timing to high-voltage and current requirements of stepping motors.

The permanent magnet stepping motor has two types of stator winding. The bipolar type has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar type, the flux reversal is accomplished by individually driving a bifilar winding on each pole. The windings are phased such that when current is passed through one winding, a given flux polarity is generated. By passing current through the other winding, the opposite flux polarity is produced. The overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by devices with open-drain outputs such as the TPIC6595.

Printers are one major application of stepping motors because the stepping motor is ideally matched to the needs of paper feeding. In this application, the paper is required to move in well-defined increments, which through gearing equate to fixed numbers of motor steps. Since the paper position is initialized by the user or at paper loading, there is no need for positional feedback. Therefore, the motion system is an open loop, and the paper is advanced by stepping the motor's rotor a given amount.

The system clock is set for a frequency of 4 kHz. This is based on time per motor step of 2.5 ms and a total of ten clock pulses required per each motor step. This is seen in equation (6), i.e., eight clock pulses for the data word plus one additional clock pulse before and after the data word.

$$t_{CLK} = \frac{2.5 \text{ ms/step}}{10 \text{ clock pulses step}} = 0.25 \text{ ms or } f_{CLK} = 4 \text{ kHz} \tag{6}$$

Figures 10, 11, and 12 illustrate two different techniques for driving a unipolar stepping motor with the TPIC6595. The motor is driven at its rated 1-A peak by operating two output DMOS transistors in parallel. In these examples the input logic, which would normally be provided by the system's microprocessor, is generated by a Hewlett Packard HP8180A Data Generator; the logic steps are shown in Table 2 and illustrated in Figure 10.
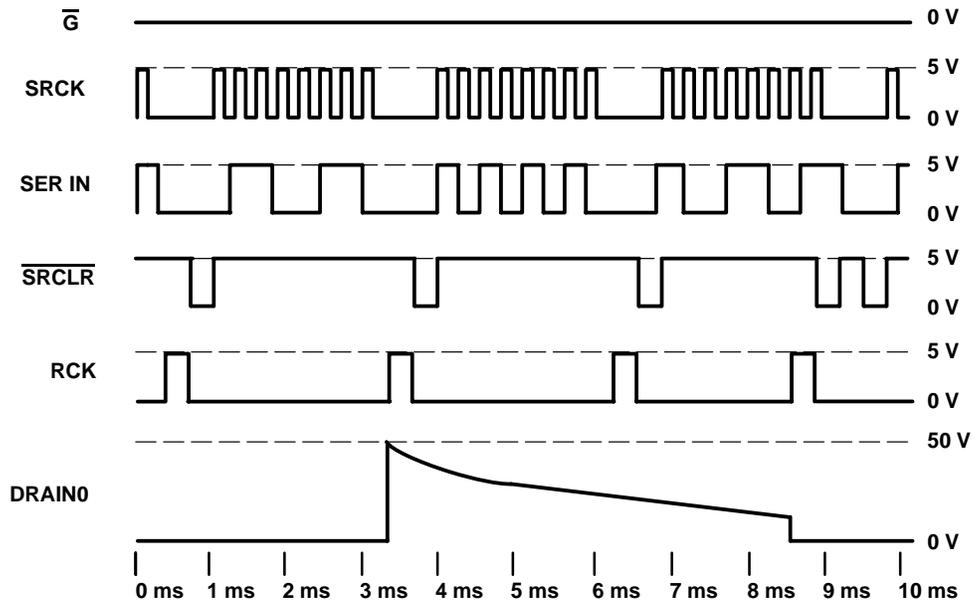
**Figure 10.  Logic and DRAIN0 Output Waveforms**

**Table 2. Word Generator Program (Four-Step Sequence)**

| CW STEP[†] | SER IN INPUT DATA WORD | TPIC6595 SWITCHES ON |
|---|---|---|
| 1 | 01010101 | DRAIN0 \|\| DRAIN4, DRAIN2 \|\| DRAIN6 |
| 2 | 01100110 | DRAIN1 \|\| DRAIN5, DRAIN2 \|\| DRAIN6 |
| 3 | 10101010 | DRAIN1 \|\| DRAIN5, DRAIN3 \|\| DRAIN7 |
| 4 | 10011001 | DRAIN0 \|\| DRAIN4, DRAIN3 \|\| DRAIN7 |
| 1 | 01010101 | DRAIN0 \|\| DRAIN4, DRAIN2 \|\| DRAIN6 |

[†] For CCW rotation, read step sequence up from bottom.

In Figure 11(a), the construction of a stepper motor results in strong magnetic coupling between the stator windings. Consequently, a change in magnetic flux that occurs when the current in winding L1 is interrupted results in an induced current within winding L2. The timing of this motor is such that when D1 parallel with D5 are switched off, D0 parallel with D4 are switched on. The current that is induced in winding L1 is in the negative direction and first flows through the body-drain diode of the DMOS transistors, decays to zero, and then increases in a positive manner. The voltage and current waveforms are shown in Figure 11(b), where it can be seen that the decay time for the negative current is approximately 700 μs. Consequently, the nature of a stepper-motor load causes both positive and negative current to flow through the DMOS power transistor.

It is possible to block the recirculating negative current by placing a diode in series with each pole winding. This is shown in Figure 12(a). In this circuit, the drain is allowed to fly to its clamp voltage, since no current is induced in another motor pole winding. The decay time of the current is now reduced to approximately 310 μs, which is considerably faster than in the previous example. However, since the energy of the pole winding is not transferred to another pole, it must be absorbed by the DMOS transistor. The device then runs considerably warmer than in the previous case. This technique can only be used in an application that does not result in the device's thermal rating being exceeded.
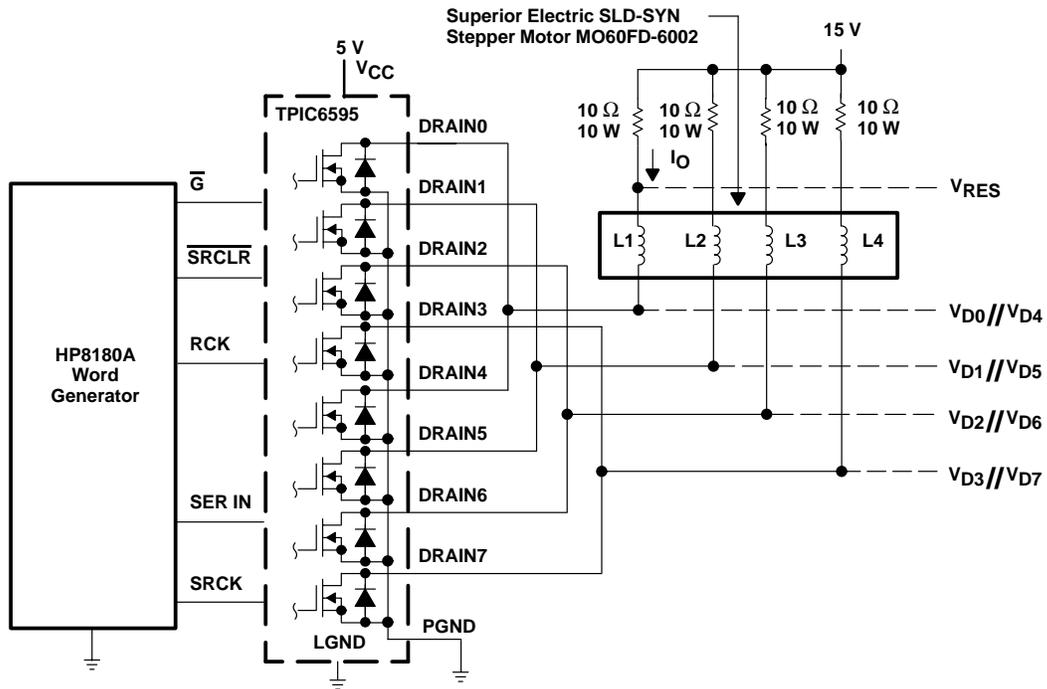
**(a) MOTOR DRIVE CIRCUIT**
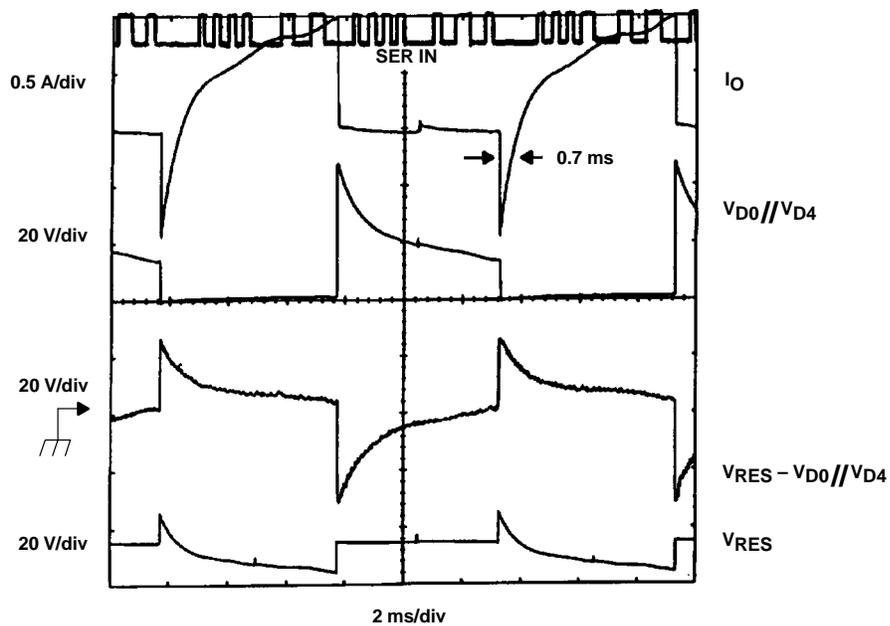


**(b) VOLTAGE AND CURRENT WAVEFORMS AT NODES SHOWN IN FIGURE 11(a)**

**Figure 11.  Unipolar Stepper Motor Drive Circuit**
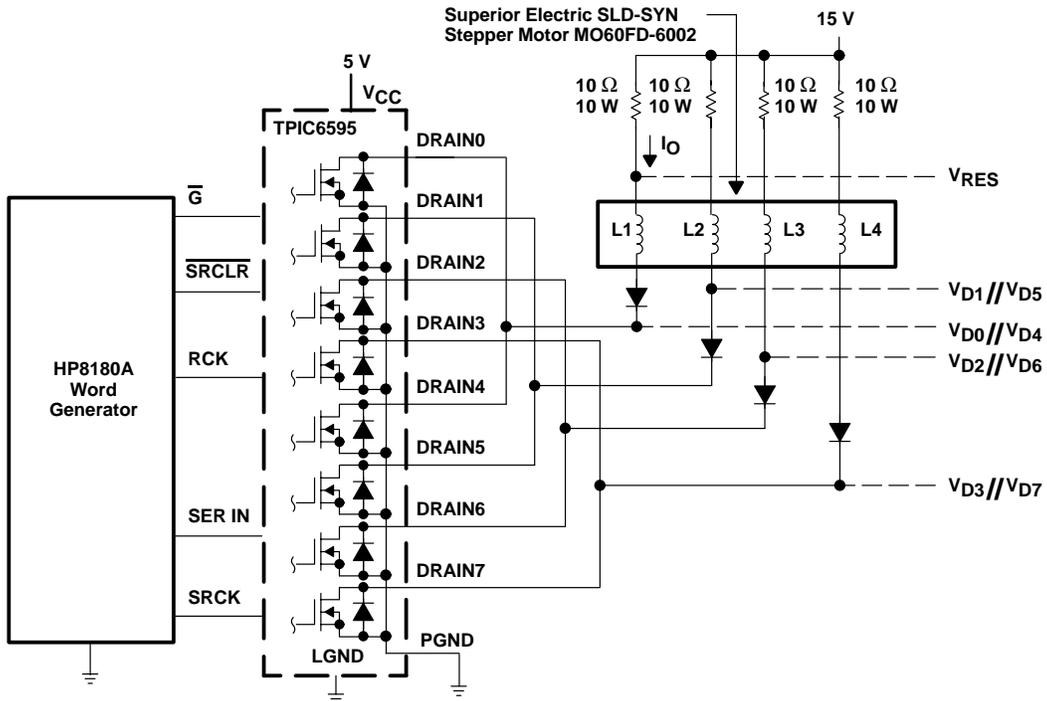
**(a) MOTOR DRIVE CIRCUIT**
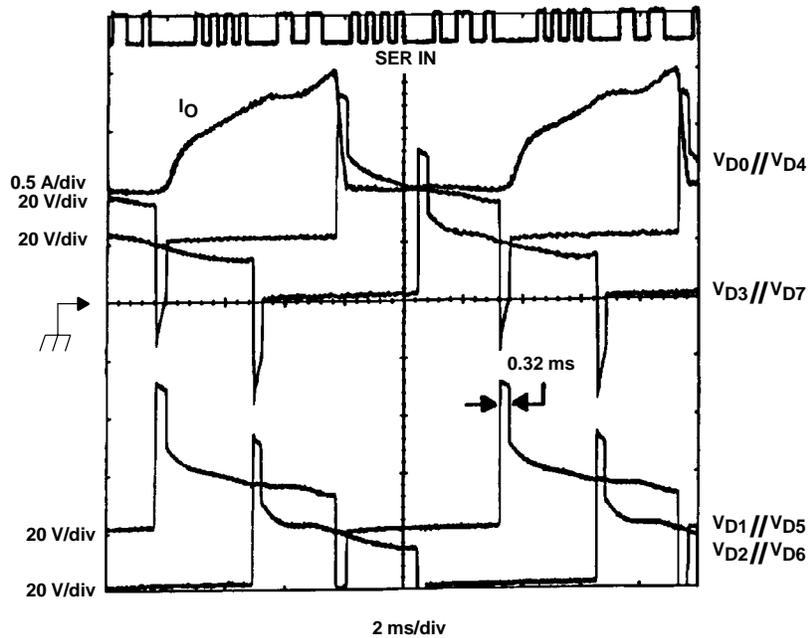


**(b) VOLTAGE AND CURRENT WAVEFORM AT NODES SHOWN IN FIGURE 12(a)**

**Figure 12.  Current and Voltage Waveforms That Occur in the Winding L1**

**200 mA/div**

**200 mV/div**

**0**

**200 $\mu$s/div**
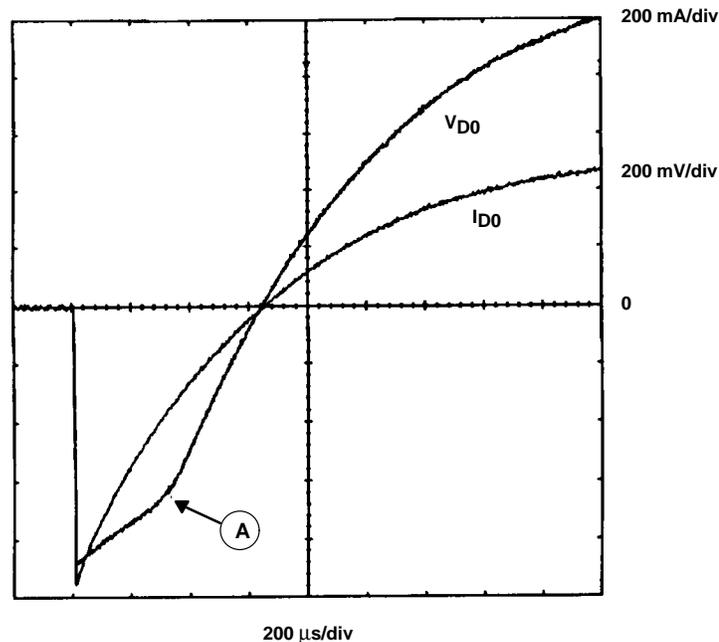
**Figure 13.  Expansion of Body Diode Reverse-Current Waveform From Figure 10(b)**

The current waveform shown within Figure 11 shows that during each winding pulse, both negative and positive current flows through the power switch. A time expansion of the negative current flow region is given in Figure 13.

Figure 13 reveals an inflection point (denoted as point A) in the voltage waveform at approximately –700 mV. When the voltage across the device is less than 700 mV, the DMOS transistor is conducting in the reverse direction, and the power dissipation is given by the product of $R_{DS(on)}$ and the square of the drain current. When the voltage across the device is greater than 700 mV, the current flow is split between the source-drain diode and the power DMOS transistor.

A feature of power integrated circuits that is often neglected is their ability to conduct current in the reverse direction. When driving inductive loads, the body drain diode is forced to conduct in the reverse direction and the resulting current flow through this device can have effects on the integrated drive logic, causing functional problems within the device. Special consideration to these problems has been given during the design phase of the TPIC6595, and no susceptibility to this type of problem has been found to exist.

## Cascade Operation of Multiple TPIC6595s

By shifting data into SER IN and out SER OUT, TPIC6595s can be connected in cascade. Figure 14 shows two TPIC6595s connected in cascade including an example SER IN timing diagram of the 16-bit data word for turning on the device number 2's output switches DRAIN6(2), DRAIN4(2), DRAIN2(2), and DRAIN0(2) and the device number 1's output switches DRAIN3(1), DRAIN2(1), DRAIN1(1), and DRAIN0(1). Also, Figure 14(b) is an oscilloscope waveform of device number 1's operation per the conditions described.

The HP8180A data generator data page for generating the example 16-bit timing diagram explained above is listed in Table 3.
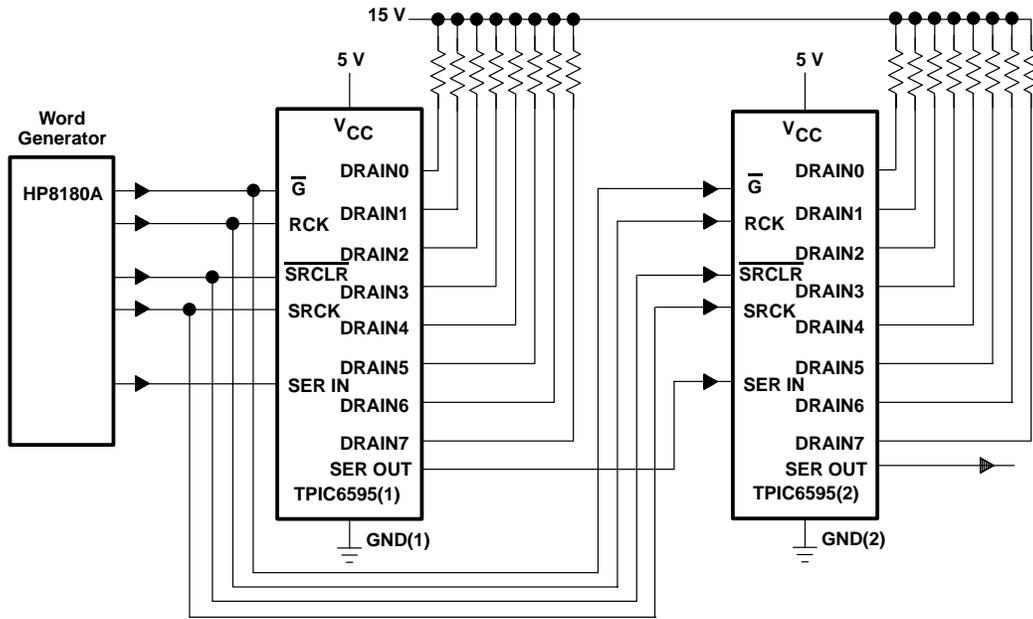
**(a) TWO TPIC6595s CONNECTED IN CASCADE**
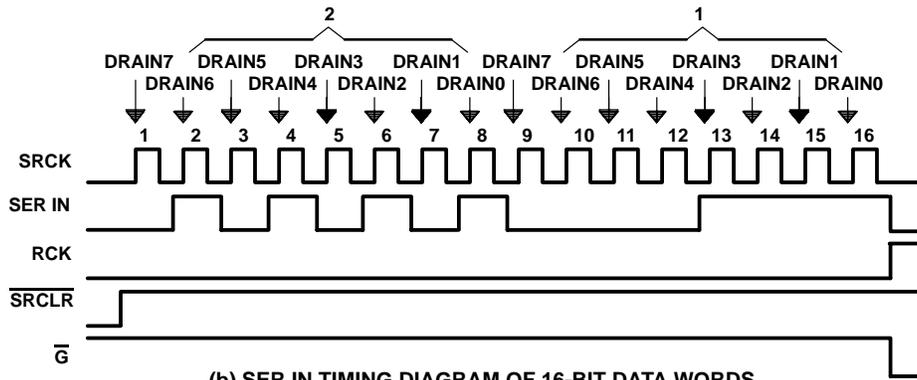


**(b) SER IN TIMING DIAGRAM OF 16-BIT DATA WORDS**



Horizontal = 20 μs/cm
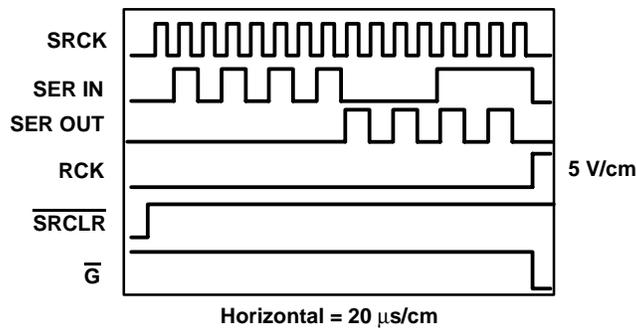
**(c) WAVEFORMS OF FIGURE 14(a) AND SER OUT**

**Figure 14.  Cascade Operation of Multiple TPIC6595s**

Table 3.  HP8180A Data Generator Data

| ADDRESS | STR | DATA (for generator outputs) | | | | |
|---------|-----|------------------------------|---|---|---|---|
|         |     | 1−0 Out NRZ RCK | 0−3 Out NRZ SRCLR | 0−2 Out RZ SRCK | 0−1 Out NRZ G | 0−0 Out NRZ SER IN |
| 0000 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0001 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0002 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0003 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0004 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0005 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0006 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0007 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0008 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0009 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0010 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0011 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0012 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0013 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0014 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0015 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0016 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0017 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0018 | 0 | 1 | 1 | 0 | 0 | 0 |

† The width is equal to 50 µs, delay 0.20 µs.
NOTE:  The frequency is equal to 20 kHz.

## Simultaneous Turn-on/Turn-off of Eight Inductors That Simulate Driving Solenoids Under Worst-Case Conditions

Figure 15 shows the test circuit and oscilloscope waveforms switching eight high-inductance inductors (R = 60 Ω and L = 250 mH) from a 15.6-V source. The device provides 0.25-A current to each inductor and dissipates 1.12 W as seen in equation (10), which is a safe-operating condition based on the 1.39-W continuous dissipation rating.

$$E_T = E_L + E_s - E_R = \frac{3L_H I^2_{DM} V_{(BR)DSX}}{6\left[V_{(BR)DSX} - V_{DD}\right] + 4R_L I_{DM}} = 9 \text{ mJ} \tag{7}$$

The calculated power dissipation $P_{OFF}$ is 1.58 W as seen in equation (5).

$$P_{OFF} = E_T \times f = 0.009 \text{ J} \times 10 \text{ Hz} = 0.087 \text{ W} \tag{8}$$

$$P_{ON} = I_{DM}{}^2 \times r_{DS(on)} = (0.25 \text{ A})^2\, 3.5 \text{ Ω} = 0.219 \text{ W} \tag{9}$$

$$\begin{aligned} P_{T(AV)} &= P_{OFF} \times n + P(QUIES) + P_{ON} \times d \times n \\ &= 0.087 \times 8 + 0.0001 \times 5 + 0.219 \times 0.24 \times 8 \\ &= 1.12 \text{ W} \end{aligned} \tag{10}$$

Where:

| | | |
|---|---|---|
| $E_L$ | Inductive energy stored in inductor | 7.7 mJ |
| $E_R$ | Energy absorbed by resistance during turn-off transient | 1.7 mJ |
| $E_S$ | Energy from power supply during turn-off transient | 2.7 mJ |
| $E_T$ | Total energy absorbed by each switch during turn-off transient | 8.7 mJ |
| f | Switching frequency | 10 Hz |
| d | Duty cycle | 0.24 |
| $L_H$ | Load inductance | 250 mH |
| $I_{DM}$ | Peak output load current | 0.25 A |
| N | Number of switches operating | 8 |
| $P_{OFF}$ | Turn-off power dissipation each switch | 0.087 W |
| $P_{ON}$ | On-state power dissipation each switch (see Equation 9) | 0.219 W |
| P(QUIES) | Bias power dissipation | 0 W |
| $P_{T(AV)}$ | Average total power dissipation | 1.12 W |
| $R_L$ | Inductor resistance | 60 Ω |
| $V_{(BR)DSX}$ | Clamp voltage [measured, see Figure 15(b)] | 50 V |
| $V_{DD}$ | Load supply voltage | 15.6 V |
| $r_{DS(on)}$ | Static drain-source on-state resistance, $T_J = 150°C$ | 3.5 Ω |
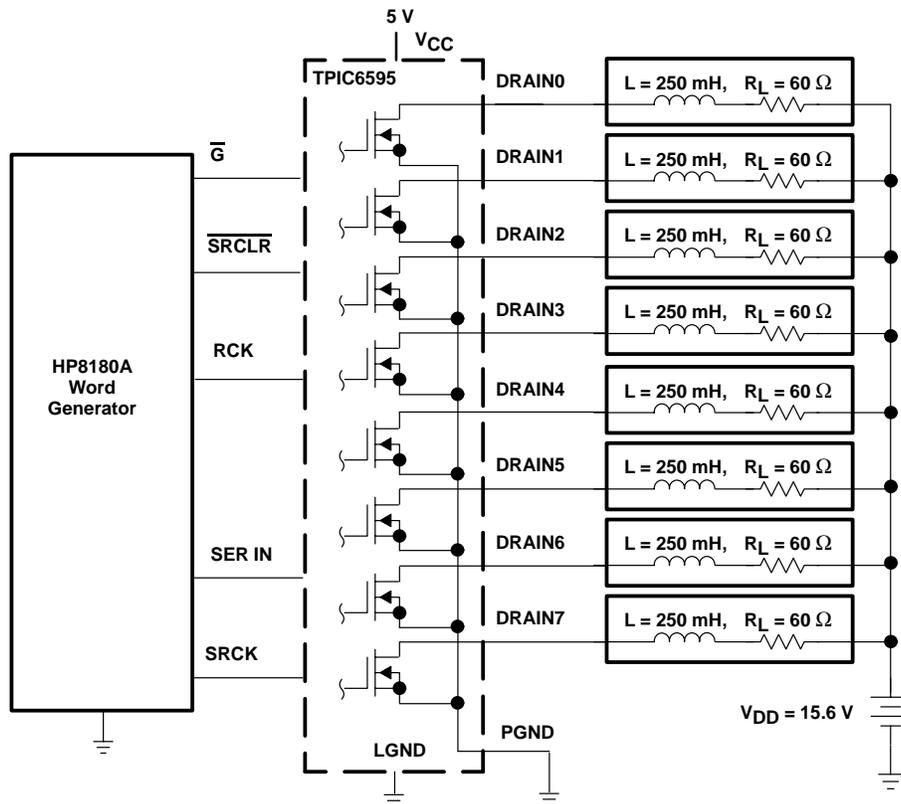


(a) SIMULTANEOUS TURN-ON/TURN-OFF CIRCUIT

**Figure 15.  Driving Solenoid Under Worst-Case Conditions**
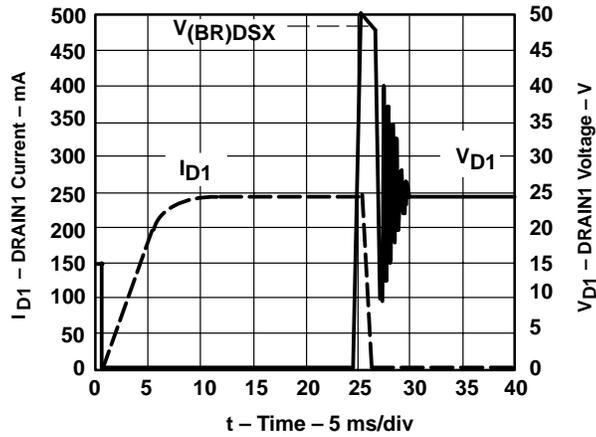
**(b) SWITCHING EIGHT HIGH INDUCTIVE LOADS**

**Figure 15.  Driving Solenoid Under Worst-Case Conditions (continued)**

### Circuit Mechanical Layout Considerations

As in any application where power is being controlled by digital and/or analog signals, it is recommended that special attention be given to the circuit layout. There are a few standard layout techniques that eliminate false triggering of the logic inputs due to noise coupling from the power components. A suggested layout is given in Figure 16.
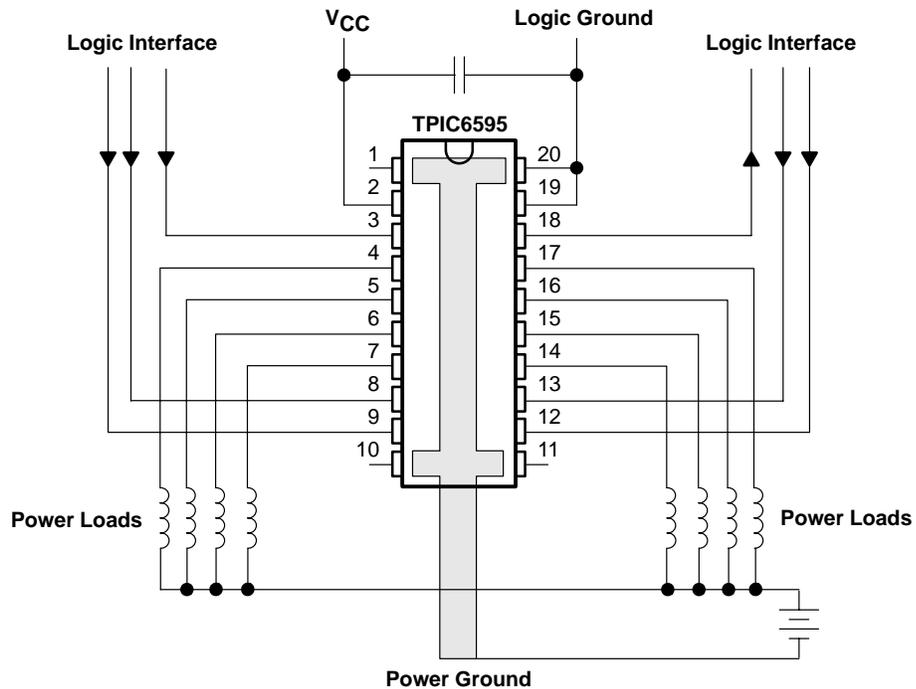


**Figure 16.  Mechanical Layout**

A 0.1-μF ceramic bypass capacitor should be connected across $V_{CC}$ and LGND and placed physically close to the TPIC6595.

A power ground bus should be created on the circuit board that is the return ground for the power loads. The PGNDs connect to the power ground bus.

The ground for the logic interface circuits should be routed separately from the power ground bus. The logic ground and power ground runs should tie in common at only one point; this one connection pin should be placed close to LGND.

The logic components that drive the TPIC6595 should be placed close to the IC.

## Conclusion

The TPIC6595 is a monolithic power logic device that contains eight 1.5-A peak/45-V low-side DMOS power switches packaged in a 20-pin dual-in-line plastic package (DIP) and wide-body surface-mount package (DW). Control of the eight power switches is accomplished from a single input by an 8-bit serial word that independently controls each of the eight power switches. All inputs accept standard TTL- and CMOS-logic levels.

The TPIC6595 is a cost-effective single-chip solution for direct control of motors, relays, solenoids, and other high energy, high electrical stress loads. Since the device implements a direct control link between the microcontroller and the system electrical loads, use of multiple logic ICs and discrete power devices are eliminated. The reduction of discrete devices not only reduces cost but saves circuit space and improves system reliability by the reduction of active components.

## Acknowledgment

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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