U UNITRODE

Design Note

UCC5343 Evaluation Board, Schematic and List of Materials

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INTRODUCTION

The UCC5343 evaluation board is supplied assembled and ready to test. This board is a complete interface of the IrDA physical layer to a standard UART at speeds up to 115Kbps. The user needs to supply power, an IrDA compliant input pulse train and a UART with an available 16X baud clock to use the board.

The board was built to allow some user configuration. The jumper block J1 allows the user to select the transmitter mode. J2 will put the chip into its run or sleep modes. An area is provided on the board where a mounting hole may be drilled or a clamp may be attached without affecting performance.

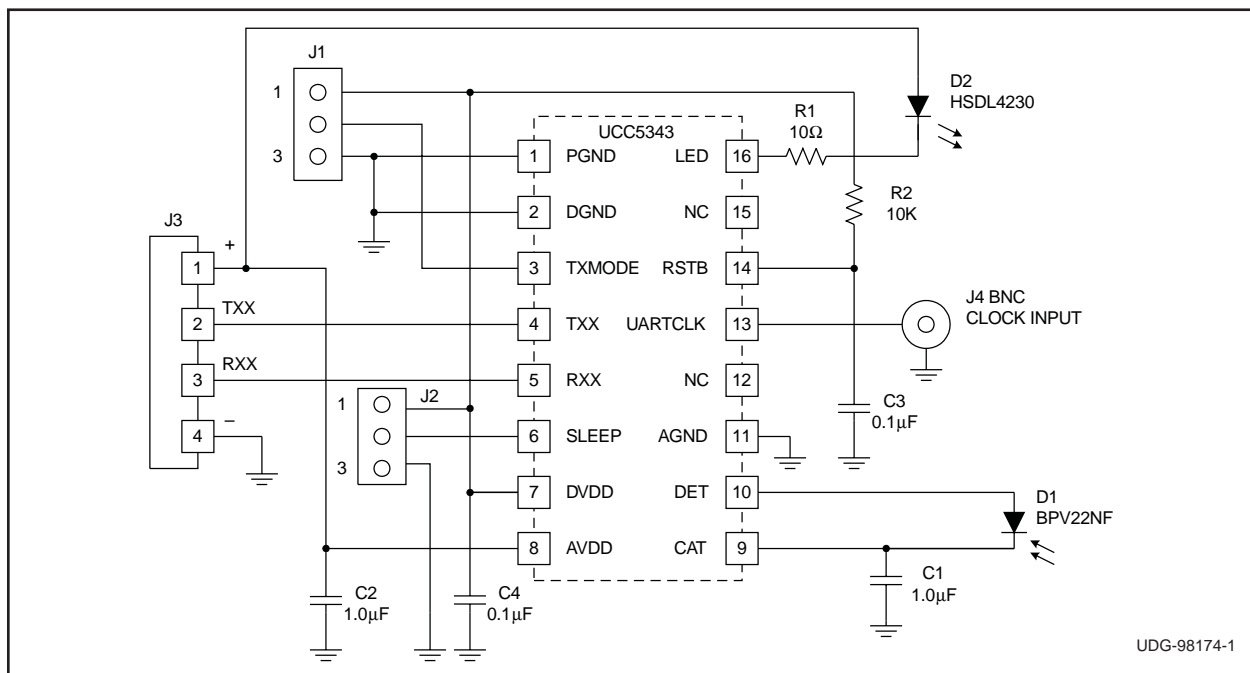The schematic of the board as supplied is shown in Fig. 1.

Figure 1. Schematic.

CONNECTIONS TO THE BOARD

There are only five connections to make to the board - two power connections, two signal connections (RXX and TXX) and a clock signal.

Power connections are made at terminals 1 and 4 (positive is 1, negative is 4) on J3. The power supply must be clean, since this part is sensitive to

noise on the power supply. The voltage must be between 2.7V and 5.5V. If two boards are being used to talk to each other, separate power supplies for each board are strongly recommended to reduce the possibility of noise coupling from the transmitter board to the receiving board's power supply. The TXX terminal should be connected to the transmit output of a standard UART.

The voltage on this connection should not be allowed to go higher than the voltage at pin 1 of J3. The RXX terminal can be monitored with an oscilloscope or connected to the receive input of a standard UART. The connector marked J4 is for connecting the 16X baud clock from the UART. A BNC connector is used here to minimize the possibility of coupling the UARTCLK signal into the DET line on the UCC5343, and causing erroneous operation. If a coaxial cable is not used to connect this

signal, twisted pair is recommended. Connect the pair to the bottom of the board, active line to the center terminal of J4, return line to one of the outer terminals of J4.

Fig. 2 shows a typical connection of the evaluation board to a 16550 type UART.

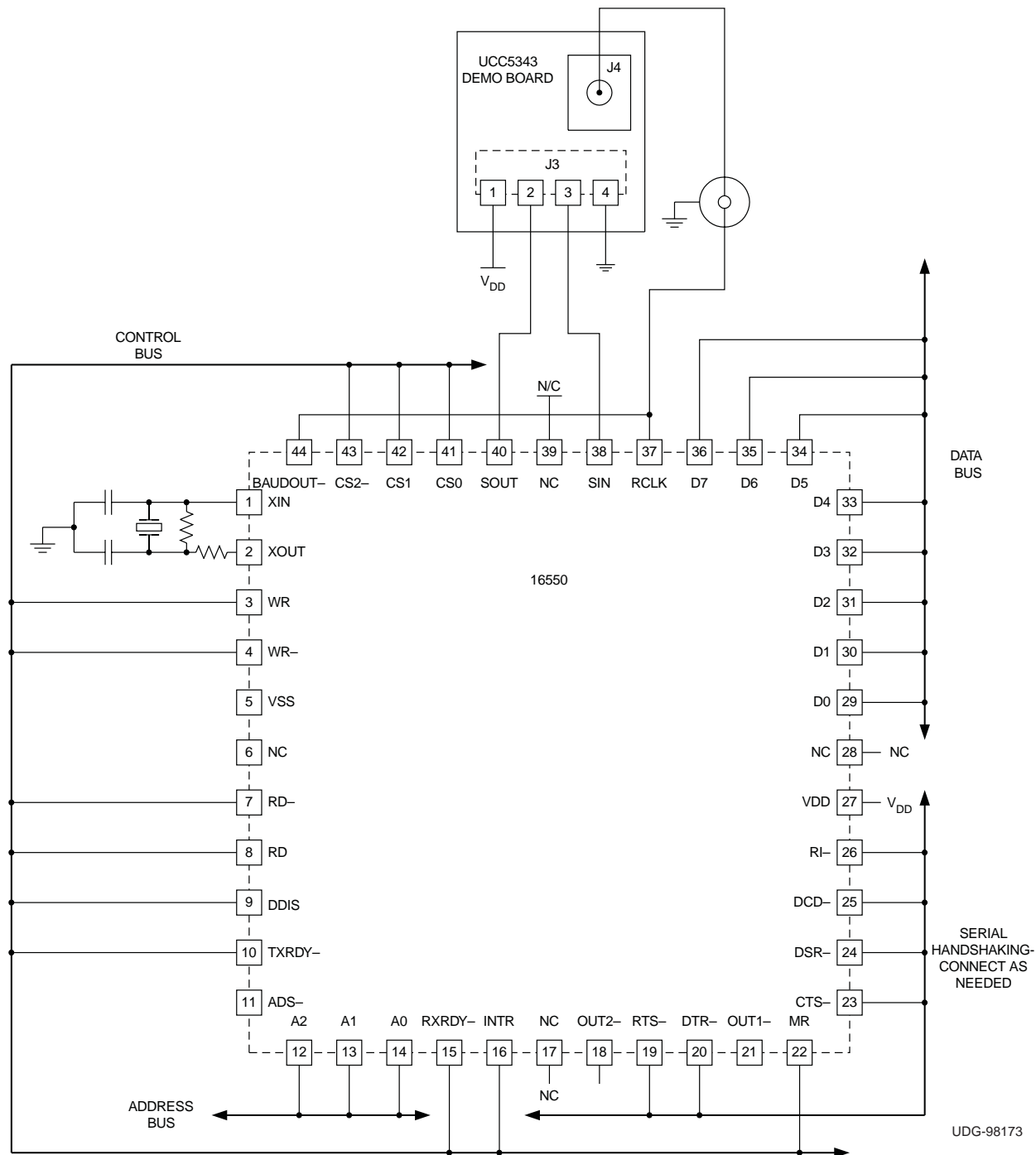With this setup, a pair of UARTS can perform half duplex communication over an IR link.

Figure 2. Interface to 16550 UART.

DET Considerations

The DET circuit board trace is surrounded with AGND in order to shield leakage noise from DET. The DET circuit board trace length is minimized. Since the PIN diode connected to DET is capacitive, noise coupling to the cathode of the diode will be coupled directly to DET. For this reason, the $1.0\mu F$ capacitor on CAT should be located physically close to the cathode of the PIN diode.

There is natural parasitic coupling from RXX to DET. RXX is routed to minimize the parasitic capacitive coupling from RXX to DET.

It is extremely important to keep the UARTCLK line as far away from the DET and CAT lines as possible. This relatively noisy signal will cause erroneous operation if it is allowed to couple into the IR detection circuitry. As an example, in one application the UARTCLK line was on the opposite side of the board and orthogonal to the DET trace. Even so, there was enough coupling between the two to cause problems.

Analog Power Supply De-coupling

The UCC5343 has a highly sensitive amplifier section capable of detecting extremely low current levels (200nA typical). Achieving this sensitivity requires quiet analog power supply rails. As a minimum, a 100nF high frequency capacitor in close proximity to AVDD and AGND is required for quiet analog rails.

The transmitter section of the chip runs from the AVDD supply and draws high peak currents (~ 500 mA in a typical application). A bulk capacitor may be required physically close to the AVDD and AGND pins if the connection length to the power supply is long or if the supply is or appears to be relatively high impedance. This bulk capacitor is in addition to the 100nF high frequency capacitor mentioned above. The bypass capacitors on CAT and AVDD should present very low equivalent series resistance and inductance to the circuit.

Digital Power Supply

DVDD is fed directly from AVDD through an internal 2K resistor. The DVDD bypass cap handles all transient current produced by the digital section of the chip. If more drive is required from RXX than the internal 2K resistor will allow, an external resistor can shunt it. This technique should always be accompanied by increasing the value of the de-coupling capacitor on DVDD and AVDD.

Jumper Settings

J1: This jumper selects the operating mode of the transmitter encoder in the UCC5343. The two modes available differ in the length of the transmitted pulse that the chip puts out. See Table 1.

J2: This jumper places the chip into its normal running mode or its sleep mode as described in Table 3.
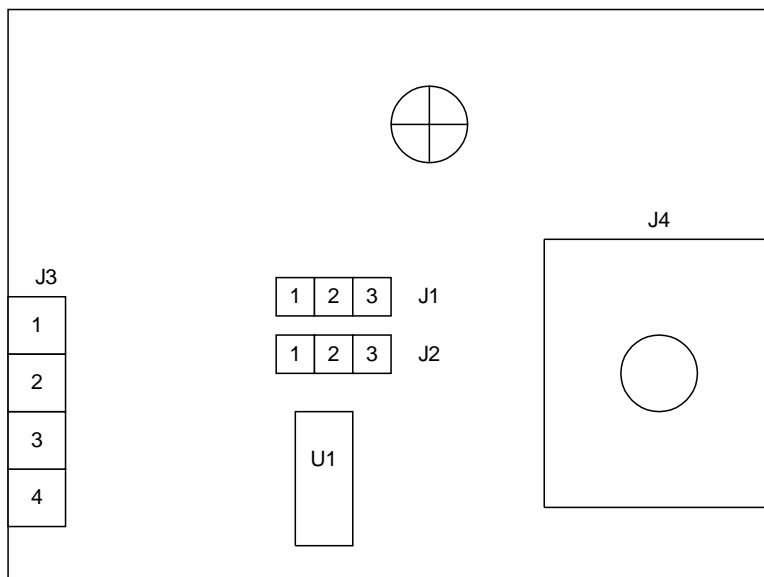
Figure 3. Jumper locations on the UCC5343 evaluation board

UDG-98175

Table 1. J1 Settings

Position	Mode
1-2	1.6µs pulse
2-3	3/16 bit time pulse

Table 2. J2 Settings

Position	Mode
1-2	Sleep
2-3	Run

Table 3. Parts List

Designator	Description	Manufacturer	Part Number
C1	1.0µF 16V Ceramic Capacitor	Murata	GRM42-6Y5V105Z16BL
C2	1.0µF 16V Ceramic Capacitor	Murata	GRM42-6Y5V105Z16BL
C3	100nF 50V Ceramic Capacitor	Murata	GRM42-6X7R104K050BL
C4	100nF 50V Ceramic Capacitor	Murata	GRM42-6X7R104K050BL
D1	Infrared Photodiode	Temic	BPV22NF
D2	Infrared LED	Hewlett Packard	HSDL4230
J1	3 Position Single Row Header	AMP	4-103321-0
J2	3 Position Single Row Header	AMP	4-103321-0
J3	4 Position Compression Terminal Block	OST	ED1601 (2 req'd)
J4	BNC Jack	AMP	227699-2
R1	10Ω, 1/8W Metal Film		Resistor
R2	10K, 1/8W Metal Film		Resistor
U1	115Kbps IrDA Transceiver with Encoder/Decoder	Unitrode	UCC5343

For more complete information, pin descriptions and specifications for the UCC5343, IrDA Transceiver with Encoder/Decoder, please refer to the UCC5343 data sheet or contact your Unitrode Field Applications Engineer at (603) 424-2410.

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