

bq20z80 Printed Circuit Board Layout Guide

Battery Management

1 Introduction

Attention to layout is critical to the success of any battery management circuit board. The mixture of high current paths with an ultralow current microcontroller creates the potential for design issues that are not always trivial to solve. Guidelines are presented to provide a stable and well performing project. Careful placement and routing is required with regard to the principles described in this document.

2 Component Placement

2.1 Power Supply Decoupling Capacitors

Power supply decoupling is important for optimal operation of the bq20z80 advanced gas gauge. To keep the loop area small, place these capacitors next to the IC. Use the shortest possible traces to the IC. Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSSD pin to the digital ground plane and another from the VSSA pin to the analog ground plane

Figure 1 is an example of what NOT to do. The decoupling caps are close to the IC, but the loop area too wide, rendering the capacitor useless and forming an antenna for noise pickup

2.2 AFE Decoupling and LDO Compensation Capacitor

Power supply decoupling for the bq29312 can best be achieved by placing a 1- μ F / 25-V capacitor mid way between pin 1 and pin 12.

The LDO voltage regulator within the bq29312 requires a 4.7- μ F capacitor to be placed close to the REG pin. This cap is for amplifier loop stabilization as well as an energy for the load.

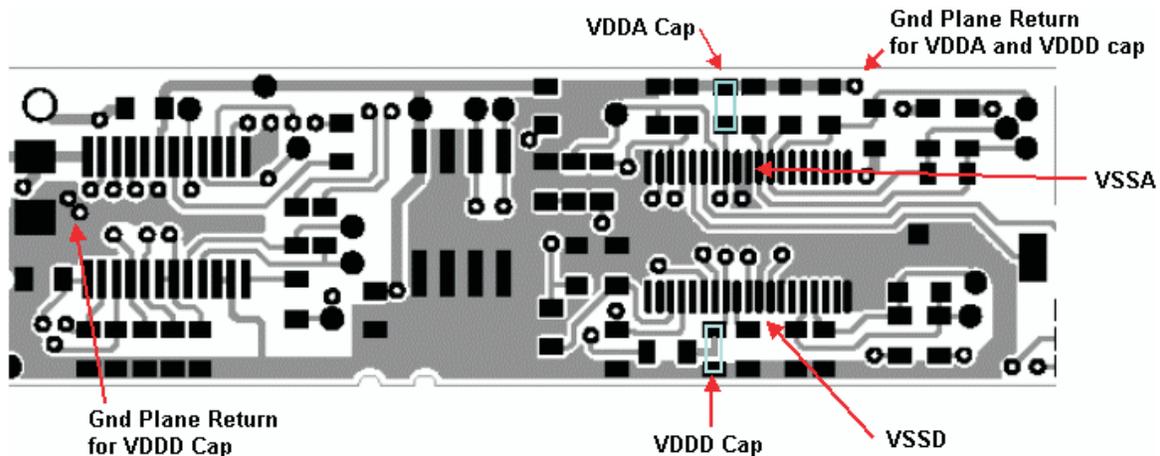


Figure 1. Bad example of decoupling capacitor placement and routing

2.3 PLL, Oscillator and Master Reset Components

The VCO in the phase locked loop (PLL) requires a low pass filter. Since this is a sensitive circuit, care should be used to place these components close to pin 32 of the IC.

The 100-K oscillator resistor, if used instead of a crystal, is perhaps the most critical component surrounding the bq20z80. Because the clock circuit is based on an extremely low level current source, any ground noise can introduce unwanted jitter into the 32 KHz clock. Place the resistor close to the IC, connecting to pins 33 and 34. Pin 34 must be connected to the analog ground when an oscillator resistor is used. Use a separate trace to connect pin 34 to analog ground at pins 29/30. This prevents any unwanted ground current from interfering with the clock

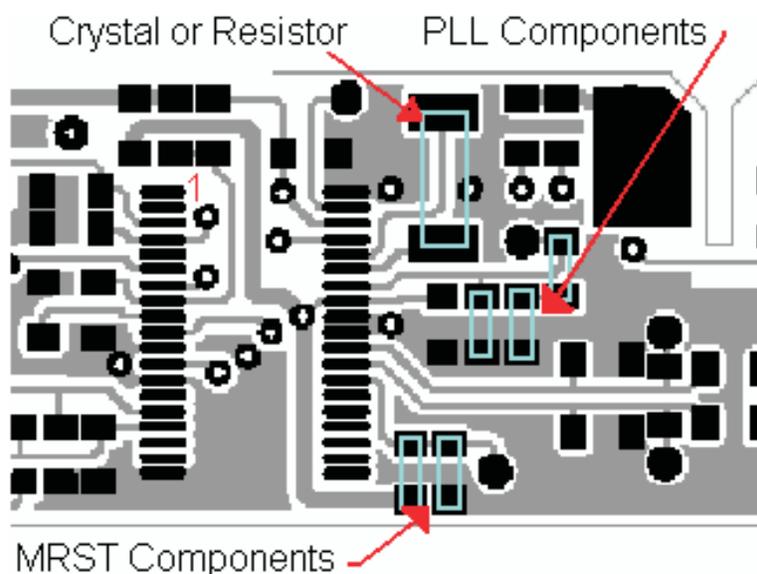


Figure 2. Minimize Length and Loop Area for These Critical Components to Reduce Noise Pickup.

2.4 Communication Line Protection Components

The 5.6-V zener diodes, used to protect the communication pins of the bq20z80 from ESD should be located as close to the pack connector as possible. The grounded end of these zeners should be returned to the Pack – node, rather than to the low current digital ground system. Therefore, ESD is diverted away from the sensitive electronics as much as possible.

2.4.1 Protector FET Bypass and Pack Terminal Bypass Capacitors

The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuit. In [Figure 3](#), an example layout demonstrates this technique.

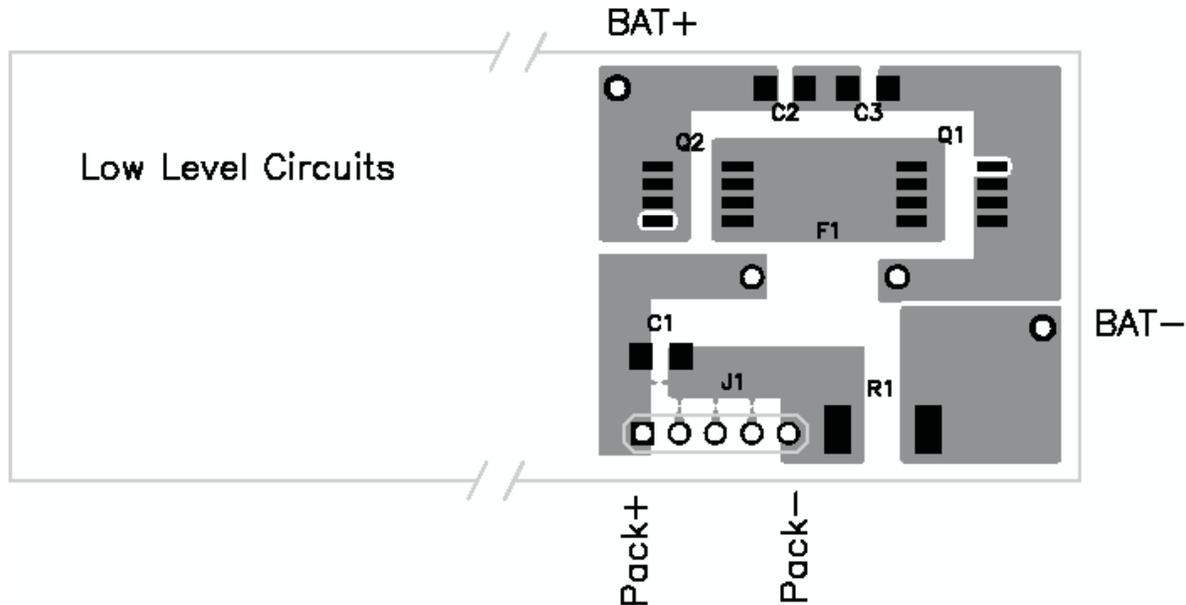


Figure 3. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, C3.

2.5 Ground Systems

The bq20z80 performs optimally when two separate low current ground systems are defined – analog and digital. In addition, ESD ground is defined along the high current path from the Pack- terminal to the sense ground. Refer to the ground symbols in the bq20z80 reference design, and provide separate low current ground systems accordingly. It is important that these two ground systems only connect at the sense resistor Kelvin pick-off point as shown in [Figure 4](#). Use inner layer ground planes, if possible, for each low current ground system.

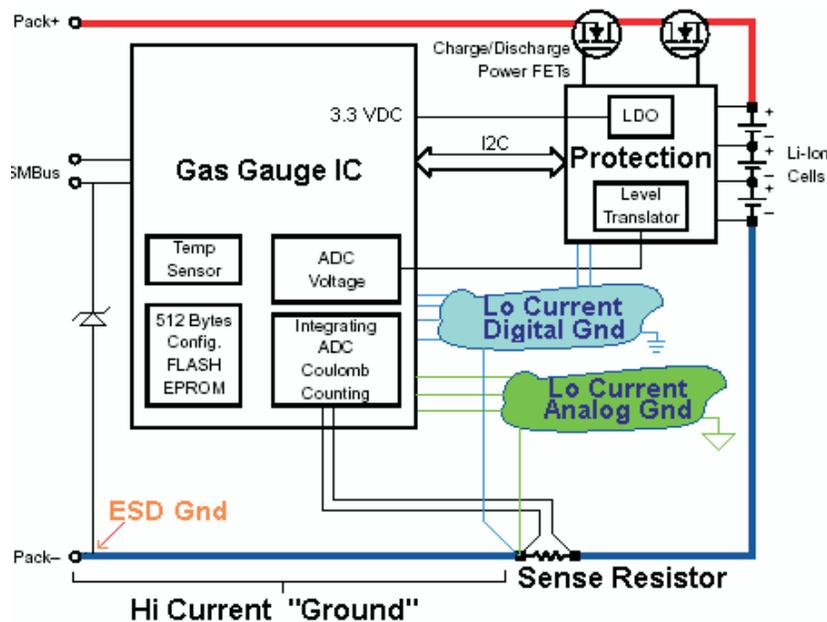


Figure 4. Use Separate Analog and Digital Low-Current Ground Systems

3 Kelvin Connections

Kelvin voltage sensing is important in order to accurately measure current, and top and bottom cell voltages. The figures below demonstrate “right” and “wrong” techniques

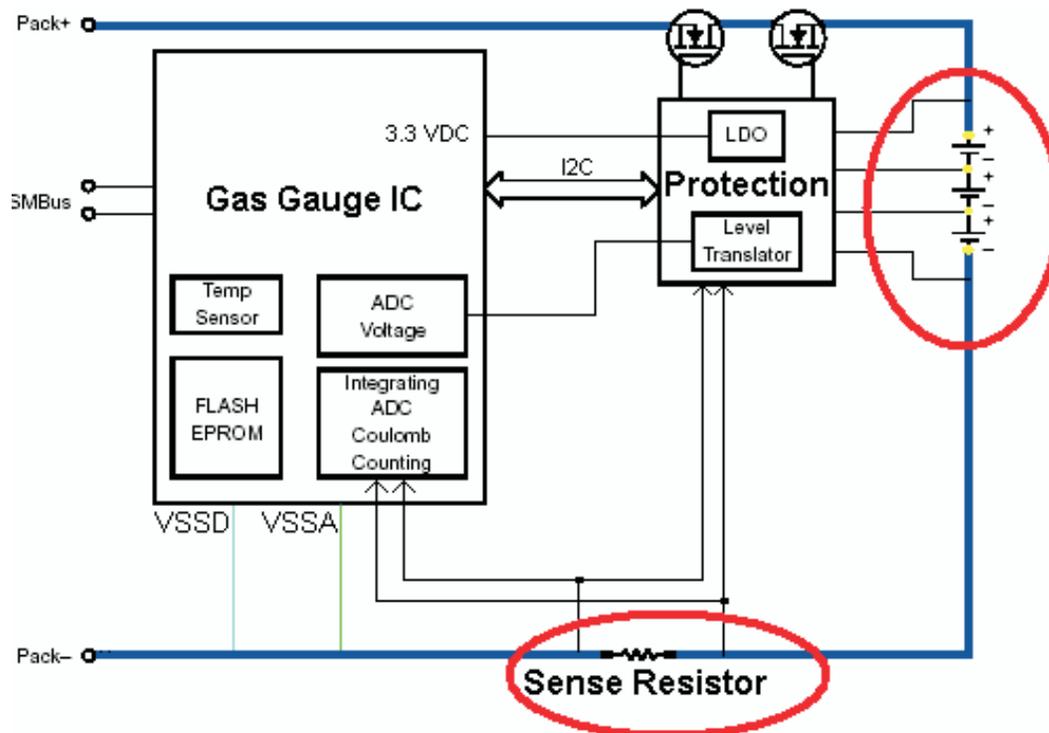


Figure 5. WRONG! Sensing Through High Current Copper Traces Produces Measurement Errors.

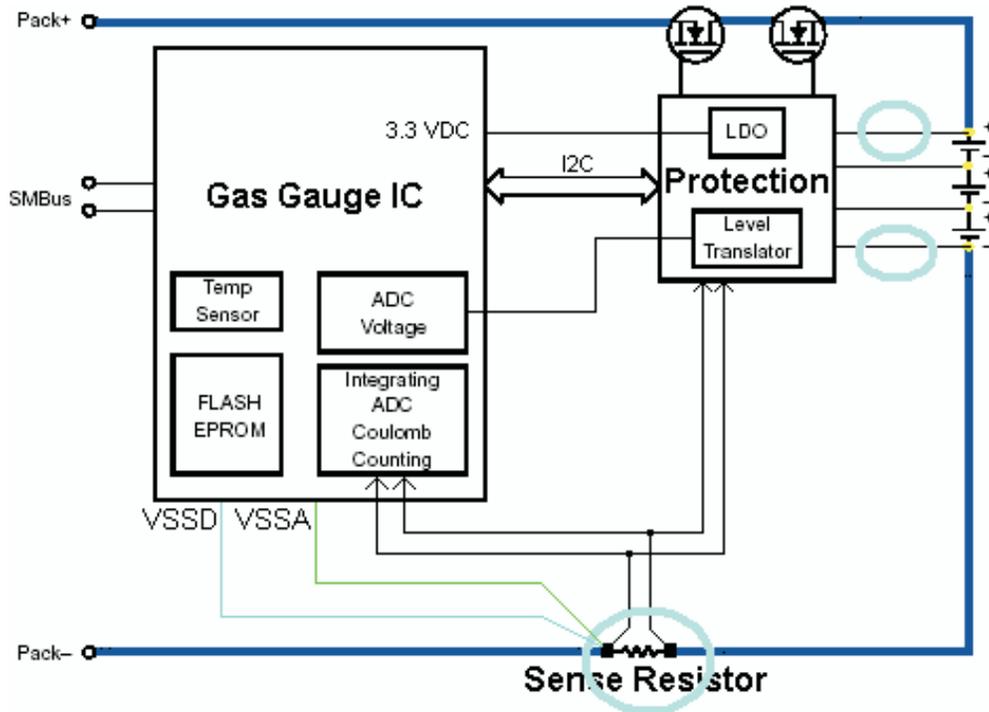


Figure 6. Fig 6. RIGHT! In Some Cases, Top and Bottom Cell Voltage Sensing may be Extended out to the Cells.

4 Board Offset Considerations

While the most important component for board offset reduction is the decoupling capacitor for VDDA, an additional benefit is possible by using this recommended pattern for the Coulomb Counter differential low pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100 ohm resistors

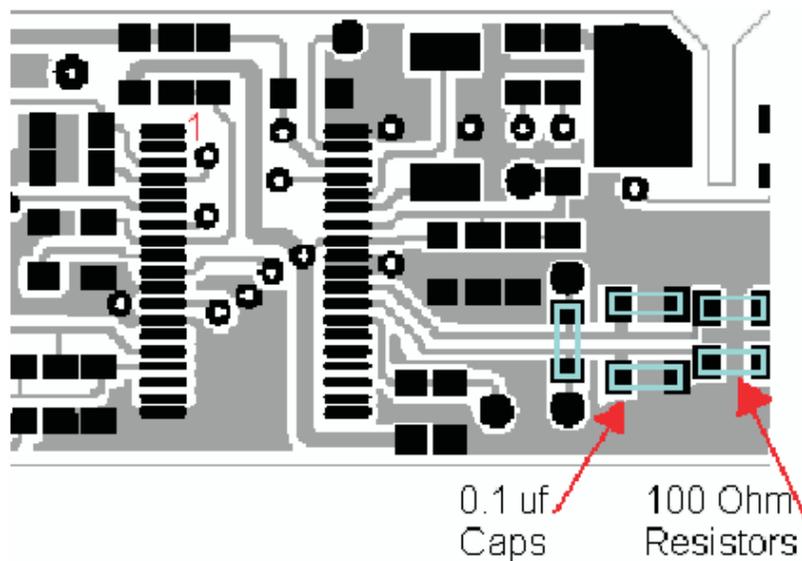


Figure 7. Differential Filter Components With Symmetrical Layout.

5 ESD Spark Gap

Protect SMBus Clock, Data, and other communication lines from ESD with a spark gap at the connector. The pattern below is recommended, with 0.2 mm spacing between the points.

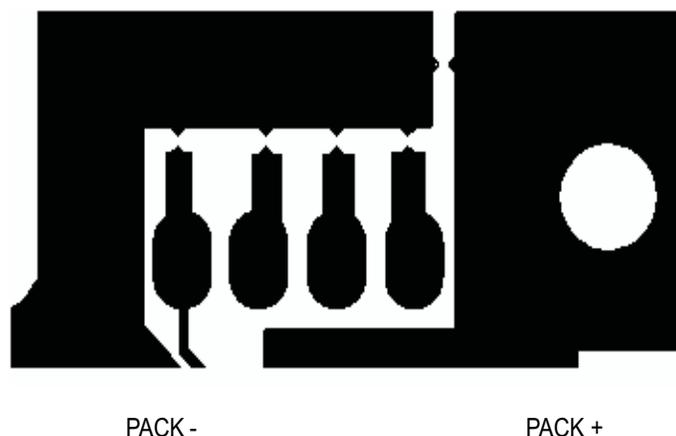


Figure 8. Recommended Spark Gap Pattern Helps Protect Communication Lines From ESD.

6 Unwanted Magnetic Coupling

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high current traces and ultralow current semiconductor devices. The best way to protect against unwanted trace to trace coupling is with a component placement such as that shown in Figure 3, where the high current section is on the right and electronics devices on the left. This is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high current traces away from signal traces, which enter the bq20z80 directly. ICs can be damaged due to magnetic and capacitive coupling from the high current path. Note that during current and ESD events, the high current traces appear inductive due to the fast current rise time

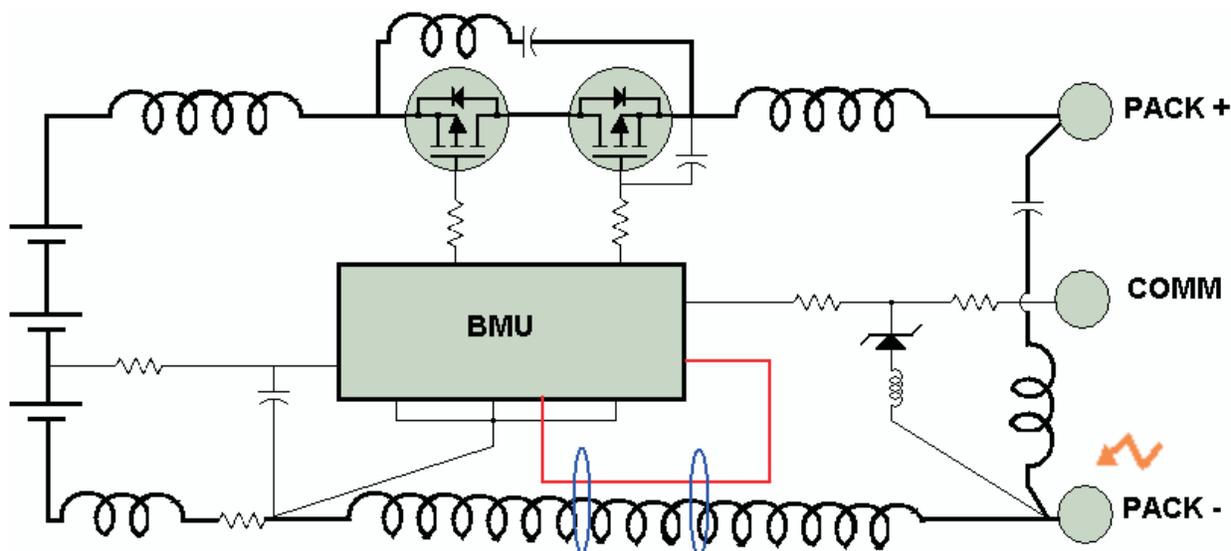


Figure 9. Avoid Close Spacing Between High Current and Low Level Signal Lines

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