Application Report
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ESD and RF Mitigation in Handheld Battery Pack Electronics

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ABSTRACT

It is imperative to protect the electronics in a consumer-removable battery pack from ESD damage. Even an upset without permanent damage may be unacceptable to the end-user. Handheld equipment that contains a transmitter also may require protection to guard against improper measurement and/or upset due to the affect of the radio frequency (RF) on the circuitry. Because the RF field strength varies as the cube of the distance from the RF source, a battery pack located close to the antenna in handheld equipment is exposed to a strong RF field.

ESD Issues

The typical gas gauge integrated circuit (IC) is rated for 2 kV at the IC pin without damage to the IC. It requires external ESD suppression to reduce the system ESD requirements, generally at least 8 kV, to a safe level for the IC. The design must further reduce the ESD level so that even an upset to the IC is avoided. For example, RAM corruption may occur as a result of ESD and is unacceptable if it causes the misreporting of available capacity or other critical information.

ESD Mitigation

Protecting the Communication Lines. The TI-recommended ESD protection for communication lines is a 5.6-V zener diode with a 100-Ω resistor between the zener diode and the battery connector pin and a second 100-Ω resistor between the zener diode and the communication pin on the IC. This circuitry appears in the reference schematics contained in the typical application schematics of the the gas gauge data sheet. The resistance between the connector pin and the zener diode limits the current flow if the pin is accidentally shorted to the positive pack terminal. Otherwise, the zener diode may likely fail and render the pack useless, as a zener diode often fails as a short. The resistance between the zener diode and the IC pin will limit the substrate current flow in the IC if the communication line suffers a negative voltage ESD event. Without the 100-Ω limiting resistance, the current divides between the zener diode and the ESD protection diode internal to the IC. The resulting substrate current flow may upset the gauge operation and result in device reset and/or RAM corruption. The protection zener diode must be connected to the high-current ground etch with a low-inductance connection. Some customers may use a transient suppressor instead of a conventional zener diode for communication line protection.

Recognizing Where the ESD Current Flows and Its Effects. One key to controlling ESD is to recognize where the current from the ESD event may flow and then take steps to reduce the amplitude, minimize the effect of the induced voltage spike along the path of the ESD current flow, and minimize the capacitive and magnetic field coupling from the ESD voltage and current pulse into sensitive circuitry. The ESD event results in a fast-rising voltage and current pulse on the line that receives the discharge. The discharge seeks the lowest-impedance path to earth ground. In a battery pack, the largest capacitance to earth ground is from the battery cells through the case to a hand or other surface adjacent to the pack. If the ESD event occurs on the Pack+ or Pack– connector terminals, the current path is obviously the high-current path from the connector to the cell. This path may pass through the lithium-ion protector FETs or through capacitors around these FETs, assuming that these capacitors are connected with low-impedance etch runs. If the ESD event occurs on a communication or other interface signal, the current finds the lowest-impedance path to the cells. Hopefully, this path is not through the communication pin of the IC. The ESD event may cause a 1-ns rise-time voltage pulse of several thousand volts and/or over 30 A of momentary current flow. The fast-rising voltage spike can capacitively couple onto any etch and components adjacent to the affected line. The fast-rising current flow from the discharge creates a large inductive voltage drop along the path of the current flow. The ESD current pulse also creates a magnetic field that can couple the transient into nearby components and etch runs.

Reducing the ESD Current Spike Amplitude. Placing a capacitor between the Pack+ and Pack– connector pins close to the connector with short and wide etch runs can improve the ESD susceptibility. This capacitor can provide an alternate path for a portion of the current pulse from a Pack+ or Pack– ESD event and reduce the peak current amplitude through any single etch run to the battery cells. This may provide some improvement in the peak ESD voltage transient level that the pack can withstand.

Avoiding ESD Currents in the Low-Current Ground Path. The recommended design practice is to separate the high-current ground etch from the low-current ground etch. Even a small inductance in the high-current ground path can develop a large potential due to the extremely fast dI/dt from the ESD event. If sensitive circuitry has multiple connections along the high-current discharge path, a large differential voltage between these connection points may occur during an ESD event. This differential voltage may allow some inputs to be momentarily pulled lower than Vss and the resulting substrate current flow can cause upset of the circuit performance. The best way to handle this issue is to connect all the low-current grounds and then tie the low-current ground to the high-current ground at a single point. Ensure that none of the ESD protection components, such as zener diodes or transient suppressors on the communication lines, tie to the low-current ground, but instead shunt any ESD fault currents directly to the high-current etch path. Ensure that the current path for these fault currents is indeed the lowest impedance path for the ESD current to flow by connecting the ESD protection components with short and wide etch to minimize the inductance in series with the components. A long, skinny etch run destroys the effectiveness of these components.

Avoiding Coupling From ESD Voltage and Current Pulse. It is difficult to eliminate coupling from the ESD pulse into the sensitive circuitry without physical separation of the high-current discharge path from the sensitive circuitry. This is difficult, if not impossible, in most miniature designs. Placing internal shield layers in the printed-circuit board (PCB) that shield the high-current path from the sensitive components may be the only practical thing that can be done. If the high-current etch path runs directly under sensitive components and etch that connects the sensitive components, then the ESD susceptibility of the design may be degraded.

Adding Spark Gaps. An approach that some designers have used to improve ESD susceptibility is the addition of spark gaps between the signal pins and Pack– at the connector etch pads. Figure 1 shows an example of this approach. The etch structure provides a small clearance between points, or corners, in the etch to encourage a breakdown from a high voltage across the clearance. The clearance must be kept free from the solder mask, as the solder mask would increase the voltage breakdown of the gap enormously. A 20-mil gap has a voltage breakdown at sea level of less than 3 kV and could help a marginal design pass the required ESD levels.

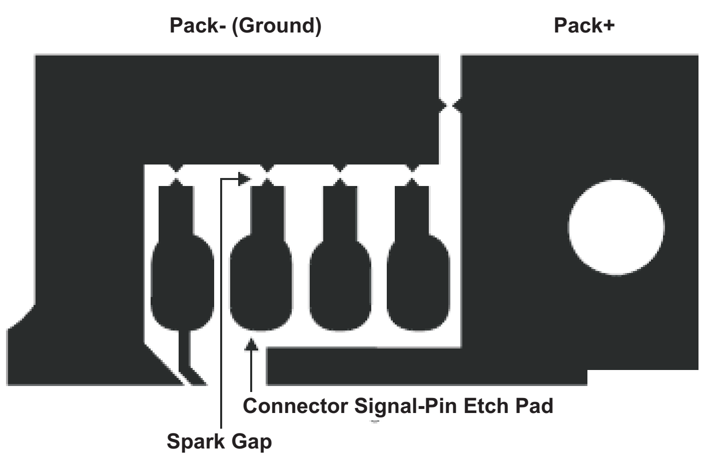

Figure 1. Typical ESD Spark-Gap Structure at Pack Connector

RF Issues

It is easy to demonstrate that radio-frequency (RF) energy can seriously affect the measurement accuracy and performance of various pieces of laboratory equipment. Just key a walkie-talkie or other transmitter while holding it close to a DVM and try to make a measurement. You can also key the transmitter while holding it close to the case of a laboratory power supply and observe how much the supply output is disturbed. A lot of laboratory equipment is not designed to operate accurately in the presence of a strong RF field. In these experiments, the RF is picked up by the wiring in the equipment, is rectified by various diode structures, and the resulting unexpected bias voltage at various nodes causes the circuitry to produce the undesirable behavior.

Likewise, RF can affect the gas gauge operation without proper precautions. The RF energy may be either conducted into the battery pack on the wiring from the battery pack connector or it may be coupled onto the battery pack wiring that may look like an RF antenna. Sometimes, the battery pack wiring may inadvertently act as an efficient antenna for the particular RF wavelength that is being used. For example, a 2.4-GHz, quarter-wavelength antenna is 3.125 cm long. It would not be unusual to find conductors in the battery pack wiring of approximately 3 cm long, that may efficiently pick up this frequency.

Many IC inputs are high impedance and do not significantly attenuate the RF amplitude present on the etch connecting to the IC input. Typical bypass capacitors, like a 0.1-µFd ceramic surface-mount capacitor, have low self-resonant frequencies and look inductive at the offending RF frequency. Small ceramic capacitors, like 68 pF to-100 pF, generally have much higher self-resonant frequencies and may have a much lower impedance than a larger ceramic capacitor, making them much more effective in filtering out RF at the IC input pins. The inputs to the gas gauge IC have ESD diode structures between the IC pins and Vss of the IC. These diodes can rectify the RF present at the IC pin and turn the energy into a negative bias at that pin and may even cause some small substrate current to flow. The extremely low current operation of some of the circuitry in the low-power IC can be disrupted by unwanted substrate current flow. Most inputs also have an ESD diode structure connected to Vcc of the IC. (They are purposely not used on the communication lines.) If the input is normally biased close to Vcc, rectified RF may bias the pin above Vcc which also causes substrate current flow and potentially upset the gauge performance.

RF Mitigation

Avoiding Critical Etch Run Lengths. It may be worthwhile to evaluate the various unshielded interconnects to ensure that none are sub-multiples of the transmitting wavelength. Avoiding quarter-wavelength and half-wavelength etch runs may help reduce the RF susceptibility. Shielding these etch runs from the RF through use of ground planes can significantly reduce the RF pickup on these runs.

Physical Separation and Shielding. Because the RF field strength drops with the cube of the distance from the transmitter antenna, physical separation of the sensitive components from the antenna is important. There are practical limitations as to how far the antenna can be physically separated from the components; shielding of the battery pack electronics may be required. However, if the transmitting antenna runs along one side of the battery pack and the critical circuitry is located on the side of the PCB nearest the antenna, reversing the PCB layout to move the circuitry to side of the PCB fartherest from the antenna can make a significant difference. For example, if the nominal distance from the antenna to the critical circuitry is 2.5 cm, moving the circuitry may result in a nominal 5-cm separation. This reduces the RF field strength by a factor of 8. A metal shield around the battery pack electronics would be desirable, but even a foil-backed insulator provides some shielding. Burying long etch runs in the PCB with ground planes as shields between the etch runs and the RF source helps reduce the RF coupled into the long etch runs.

RF filtering. If the sensitive components are separated and shielded sufficiently, wiring that is close to the antenna that connects to the battery pack can conduct the RF directly into the sensitive circuitry. RF feedthrough capacitors on all connections going into the battery pack is ideal, but difficult to implement in most designs. The large (low-frequency) bypass capacitors are minimally effective at removing RF from etch runs. Use of smaller ceramic capacitors, like 68 pF to 100 pF, are much more effective than the larger value capacitors at RF frequencies. Filtering RF off the connections to the battery pack and shielding long conductors may not eliminate all the RF. Filter capacitors may be needed on some of the critical inputs to further reduce the RF amplitude. These capacitors must be placed as close to the IC as practical and connected with short and wide conductors. Note that the Vss end of the capacitors must be connected with as much care as the signal end, as interconnect inductance in either connection can render it ineffective.