Application Report
SLUA479B–August 2008–Revised July 2010

UCC28070 300-W Interleaved PFC Pre-Regulator Design Review

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ABSTRACT

In higher power applications to utilize the full line power and reduce line current harmonics PFC Pre-regulators are generally required. In these high power applications interleaving PFC stages can reduce inductor volume and reduce input and output capacitor ripple current. This results in smaller overall magnetic volume and filter capacitor volume increasing the converters overall power density. This is made possible through distributing the power over two interleaved boost converters and the inductor ripple current cancellation that occurs with interleaving, reference [5]. This application note will review the design of a 300W two-phase interleaved power factor corrected (PFC) pre-regulator. This power converter achieves PFC with the use of the UCC28070 interleaved PFC controller, reference [7].

1 Design Goals

The specifications for this design were chosen based on the power requirements of a medium power LCD TV.

Table 1. Design Specifications

PARAMETER		MIN	TYP	MAX	UNITS
V_{IN}	RMS input voltage	85 (V_{IN_MIN})		265 (V_{IN_MAX})	V
V_{OUT}	Output voltage		390		
	Line frequency	47 Hz (f_{LINE})		63	Hz
PF	Power factor at maximum load	0.90			
P_{OUT}	Output power			300	W
η	Full load efficiency	90%			
f_s	Individual phase switching frequency	200			kHz

2 Schematic

UCC28070 PFC controller in a two-phase average current mode control interleaved PFC pre-regulator.

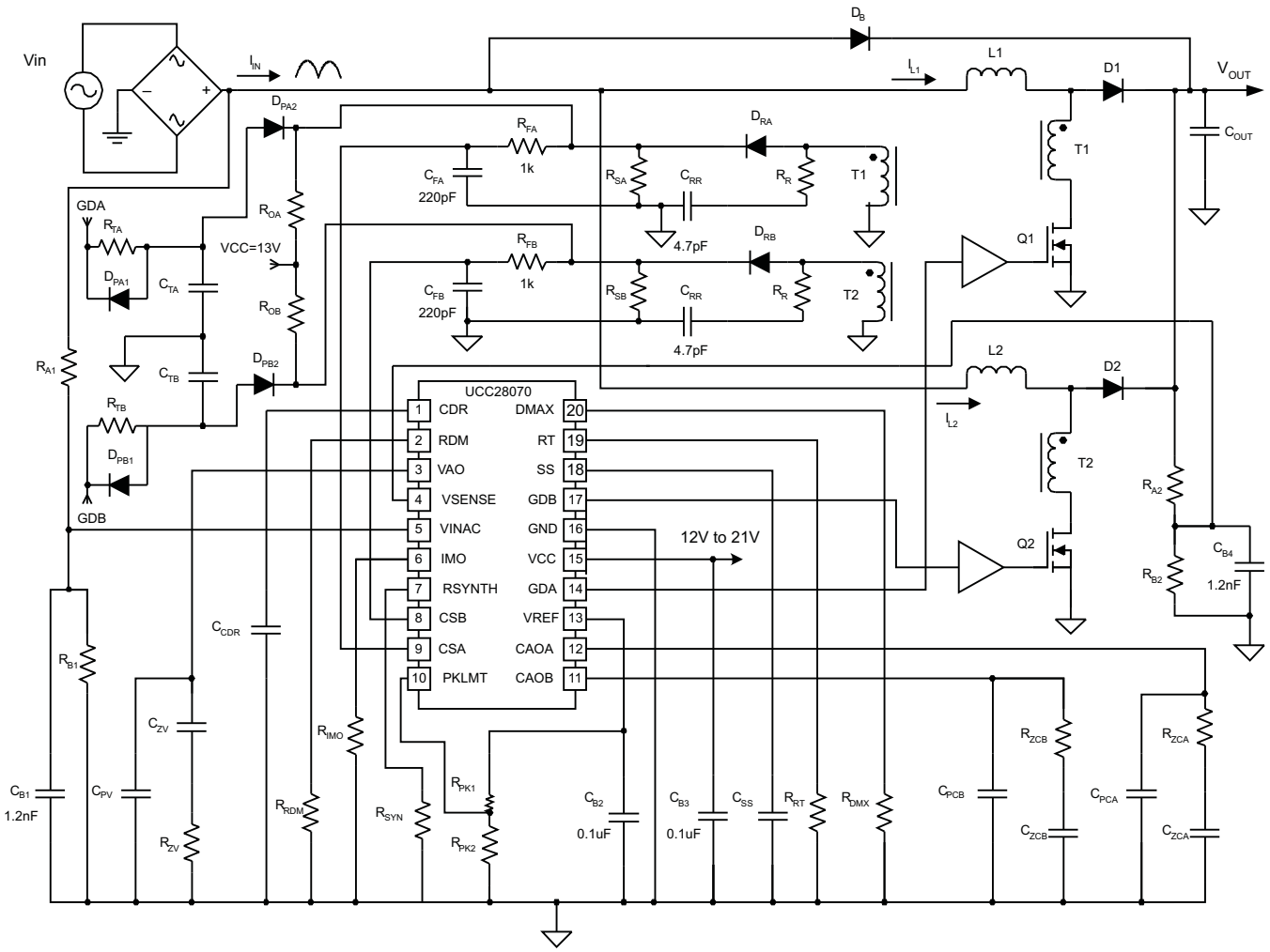

Figure 1. Typical Average Current Mode Interleaved PFC Pre-Regulator

3 Inductor Selection

One of the benefits of interleaved PFC boost pre-regulators is inductor ripple current reduction that is seen at the input of the converter. The following equations and Figure 2 show the ratio of input ripple current (ΔI_{IN}) to individual inductor ripple current (ΔI_{L1}) in a two-phase interleaved PFC as a function of duty cycle (D). Because of this inductor ripple current cancellation, the designer can allow each inductor to have more inductor ripple current than in a single stage design.

$$K(D) = \frac{\Delta I_{IN}}{\Delta I_{L1}} \quad (1)$$

$$K(D) = \frac{1-2D}{1-D} \text{ if D is < 05 = 0.5} \quad (2)$$

$$K(D) = \frac{2D-1}{D} \text{ if D is > 0.5} \quad (3)$$

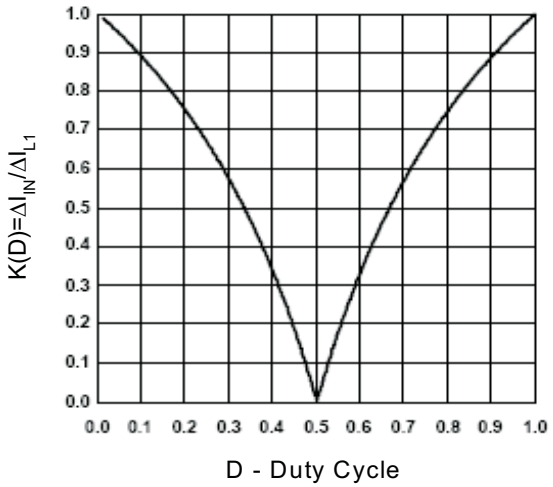

Figure 2. Input Inductor Ripple Current Cancellation

The boost inductors (L1 and L2) are selected based on the maximum allowable input ripple current. In universal applications (e.g., 85 V to 265 V RMS input) the maximum input ripple current occurs at the peak of low line and for this design the maximum input ripple current was set to 30% of the peak nominal input current at low line.

The following calculations are used to select the appropriate inductance for L1 and L2. Where, variable D_{PLL} is the converter's duty cycle at the peak of low line operation. Variable $K(D_{PLL})$ is the ratio of input current to inductor ripple current at the peak of low line operation. ΔIL is the boost inductor ripple current at the peak of low line based on the converters input ripple current requirements.

$$D_{PLL} = \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}}{V_{OUT}} = \frac{390V - 85V\sqrt{2}}{390\ V} \approx 0.69 \tag{4}$$

$$K(D_{PLL}) = \frac{2 \times 0.69 - 1}{0.69} = 0.55$$

$$\Delta IL = \frac{P_{OUT} \times \sqrt{2} \times 0.3}{V_{IN\_MIN} \times \eta \times K(D_{PLL})} = \frac{300W \times \sqrt{2} \times 0.3}{85V \times 0.90 \times 0.55} \approx 3.0\ A$$

$$L1 = L2 = \frac{V_{IN\_MIN} \times \sqrt{2} \times D_{PLL}}{\Delta IL \times f_s} = \frac{85V \times \sqrt{2} \times 0.69}{2.96A \times 200\ kHz} \approx 140\ uH \tag{5}$$

The following equation can be used to calculate total inductor RMS current (I_{L1_RMS} and I_{L2_RMS}).

$$I_{L1\_RMS} = I_{L2\_RMS} = \sqrt{\left(\frac{\frac{P_{OUT}}{2}}{V_{IN\_MIN} \times \eta}\right)^2 + \left(\sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{V_{IN\_MIN}\sqrt{2}\sin(\theta)}{L1 \times f_s} \times \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}\sin(\theta)}{V_{OUT}}}{\sqrt{12}}\right)^2} \tag{6}$$

$$I_{L1\_RMS} = I_{L2\_RMS} = \sqrt{\left(\frac{\frac{300W}{2}}{85V \times 0.90}\right)^2 + \left(\sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{85V\sqrt{2}\sin(\theta)}{140uH \times 200kHz} \times \frac{390V - 85V\sqrt{2}\sin(\theta)}{390V}}{\sqrt{12}}\right)^2} \approx 2A \tag{7}$$

A 140-µH boost inductor from Cooper Electronic Technologies part number CTX16-18060 was chosen for the design. The inductance during normal operation will swing from 140µH to 350µH.

$$L1_{MIN} = L2_{MIN} = 140\ uH \tag{8}$$

$$L1_{MAX} = L2_{MAX} = 350\ uH \tag{9}$$

The average inductance is calculated for current loop compensation purposes. This will be used in the current loop compensation section of the application note:

$$L1_{AVG} = L2_{AVG} = \frac{L1_{MIN} + L1_{MAX}}{2} = \frac{140\ uH + 350\ uH}{2} = 245\ uH \tag{10}$$

4 Output Capacitor Selection

The output capacitor (C_{OUT}) is selected based on holdup requirements.

$$C_{OUT} \geq \frac{\frac{2 \times P_{OUT}}{f_{LINE}}}{V_{OUT}^2 - (V_{OUT} \times 0.75)^2} = \frac{\frac{2 \times 300W}{47\ Hz}}{(390V)^2 - (292.5V)^2} \approx 192\ uF \quad (11)$$

Two 100-µF capacitors were used in parallel for the output capacitor.

$$C_{OUT} = 200\ \mu F \quad (12)$$

For this size capacitor the output peak to peak voltage ripple (V_{RIPPLE}) is:

$$V_{RIPPLE} = \frac{2 \times P_{OUT}}{\eta} \frac{1}{V_{OUT} \times 2\pi \times 2f_{LINE} \times C_{OUT}} = \frac{\frac{2 \times 300W}{0.90}}{390V \times 2\pi \times 2 \times 47Hz \times 200\ \mu F} \approx 14.5V \quad (13)$$

In addition to holdup requirements, a capacitor must be selected so that it can withstand both the low-frequency RMS current (I_{COUT_LF}) and the high-frequency RMS current (I_{COUT_HF}). High-voltage electrolytic capacitors generally have both low frequency (100 Hz to 120 Hz) and high frequency RMS current ratings on their data sheets.

$$I_{COUT\_LF} = \frac{P_{OUT}}{\eta V_{OUT} \sqrt{2}} = \frac{300W}{0.90 \times 390V \times \sqrt{2}} \approx 0.604A \quad (14)$$

$$I_{COUT\_HF} = \sqrt{\left(\frac{P_{OUT}}{\eta V_{OUT}} \sqrt{\frac{16 \times V_{OUT}}{6\pi \times V_{IN\_MIN}\sqrt{2}} - \eta^2} \right)^2 - \left(I_{COUT\_LF}\right)^2} \quad (15)$$

$$I_{COUT\_HF} = \sqrt{\left(\frac{300W}{0.90 \times 390V} \sqrt{\frac{16 \times 390V}{6\pi \times 85V\sqrt{2}} - (0.90)^2} \right)^2 - (0.604)^2} \approx 1.0A \quad (16)$$

5 Power Semiconductor Selection (Q1, Q2, D1, D2)

The selection of Q1, Q2, D1, and D2 are based on the power requirements of the design. Application note (SLUA369), *UCC28528 350-W Two Phase Interleaved PFC Pre-regulator*, explains how to select power semiconductor components for interleaved PFC pre-regulators using average current mode control techniques, reference [4]. To meet the power requirements of this design IRFB11N50A N channel FETs from IR were chosen for Q1 and Q2. To reduce reverse recovery losses SiC diodes CSD10060G from CREE were chosen for the design.

Boost Diode (D1, D2) and FET (Q1, Q2) peak current (I_{PEAK}) calculation:

A factor of 1.2 was added to the equation for added design margin.

$$I_{PEAK} = \left(\frac{P_{OUT} \times \sqrt{2}}{2 \times V_{IN\_MIN} \times \eta} + \frac{\Delta I_{L1}}{2} \right) 1.2 = \left(\frac{300W \times \sqrt{2}}{2 \times 85V \times 0.90} + \frac{2.97A}{2} \right) 1.2 \approx 5.1A \quad (17)$$

Q1 and Q2 RMS current (I_{DS}) calculation:

$$I_{DS} = \frac{\frac{P_{OUT}}{\eta}}{2 \times V_{IN\_MIN}\sqrt{2}} \sqrt{2 - \frac{16 \times V_{IN\_MIN}\sqrt{2}}{3 \times \pi \times V_{OUT}}} = \frac{\frac{300W}{0.90}}{2 \times 85V\sqrt{2}} \sqrt{2 - \frac{16 \times 85V\sqrt{2}}{3 \times \pi \times 390V}} \approx 1.685A \quad (18)$$

D1 and D2's average current calculation (I_D):

$$I_D = \frac{P_{OUT}}{V_{OUT}} = \frac{300W}{2 \times 390V} \approx 0.39A \quad (19)$$

6 Current Sense Transformers Setup and Selection (T1, T2, D_{RA}, D_{RB})

The current sense transformer is selected to handle I_{PEAK} and have a peak current sense signal (I_{RS}) of roughly 100 mA.

$$N_{CT} = \frac{N_S}{N_P} \geq \frac{I_{PEAK}}{I_{RS}} = \frac{5.1A}{0.1A} = 51 \quad (20)$$

For this design a current sense transformer with a turns ratio (N_{CT}) of 50 was chosen for the design.

$$N_{CT} = 50 \quad (21)$$

The magnetizing inductance (L_M) of the current sense transformer should be selected or designed so the magnetizing current is less than 2% of the maximum current sense signal. The following equation calculates the minimum L_M where V_S is the maximum current sense signal voltage. For this design a current sense transformer was designed by Cooper Electronic Technologies (CTX16-18294) with a magnetizing inductance of 8.25 mH.

$$L_M \geq \frac{V_S}{\frac{I_{PEAK}}{N_{CT}} \times 0.02 \times f_s} \times \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}}{V_{OUT}} = \frac{3.7V}{\frac{5.1A}{50} \times 0.02 \times 200kHz} \times \frac{390V - 85V\sqrt{2}}{390V} \approx 6.24mH \quad (22)$$

$$L_M = 8.25 \text{ mH} \quad (23)$$

Selection of the current sense resistors (R_{SA} and R_{SB}) is based on the peak current limit signal (V_S) and the peak current on the secondary side of the current sense transformer. A factor of 0.9 was multiplied by the current sense signal to leave room for the 10% PWM ramp that is used to make this design more noise immune at lighter loads.

$$R_{SA} = R_{SB} = \frac{0.9 \times V_S}{\frac{I_{PEAK}}{N_{CT}}} = \frac{0.9 \times 3.7V \times 50}{0.102A} \approx 32.5\ \Omega \quad (24)$$

Select a standard resistor for the design:

$$R_S = 33.2\ \Omega \quad (25)$$

Resistor R_R is used to reset the current sense transformer:

$$R_R \geq \frac{R_S \times D_{MAX}}{1 - D_{MAX}} = \frac{33.2\ \Omega \times 0.97}{1 - 0.97} \simeq 1\ k\Omega \quad (26)$$

Current sense transformer's rectifying diodes (D_R) need to be designed to withstand the current sense transformers reset voltage (V_R):

$$V_R = I_{PEAK} \times \frac{N_P}{N_S} \times R_R = \frac{5.1A \times 1\ k\Omega}{50} \geq 103V \quad (27)$$

To improve noise immunity at extremely light loads, a PWM ramp with a dc offset is recommended to be added to the current sense signals. Electrical components R_{TA}, R_{TB}, C_{TA}, C_{TB}, D_{PA1}, D_{PA2}, D_{PB1}, and D_{PB2} form a PWM ramp that is activated and deactivated by the gate drive outputs of the UCC28070. Resistor R_{OA} and R_{OB} add a DC offset to the CS resistors (R_{SA} and R_{SB}).

When the inductor current becomes discontinuous the boost inductors ring with the parasitic capacitances in the boost stages. This inductor current rings through the CTs causing a false current sense signal. Refer to the following graphical representation of what the current sense signal looks like when the inductor current goes discontinuous. Note that the inductor current and V_{RSA} may vary from this graphical representation depending on how much inductor ringing is in the design when the unit goes discontinuous.

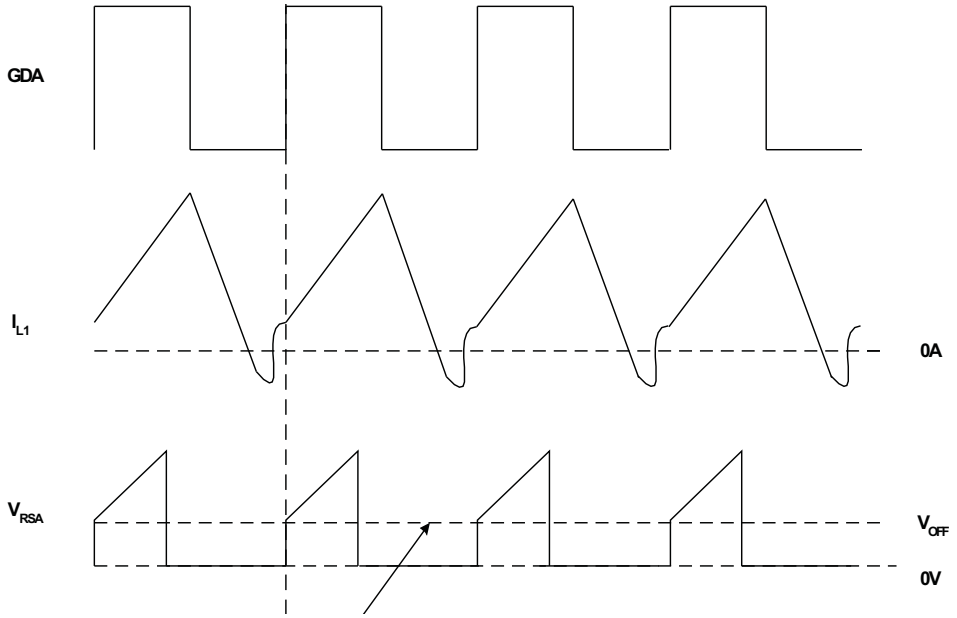

Figure 3. False Current Sense Signal

To properly select the offset (V_{OFF}) just requires adjusting resistors R_{OA} and R_{OB} to add a dc offset to the current sense resistors, that is high enough to block D_{RA} and D_{RB} from conducting when a false current sense signals is present. This occurs when the inductors are operating with discontinuous inductor current and was described above in detail. Setting the offset to 200 mV is a good starting point and may need to be adjusted based on individual design criteria and the amount of noise and parasitic elements present in the system.

$$V_{OFF} = 0.2\ V \tag{28}$$

$$R_{OA} = R_{OB} = \frac{(V_{VCC} - V_{OFF})R_{SA}}{V_{OFF}} = \frac{(13V - 0.2V) \times 33.2}{0.2V} \approx 2.1\ k\Omega \tag{29}$$

Select a standard resistor for the design:

$$R_{OA} = 2.05\ k\Omega \tag{30}$$

$$R_{TA} = R_{TB} = \frac{(V_{VCC} - (V_s \times 0.1 - V_{OFF} + V_{DPA2})R_{SA}}{V_s \times 0.1 - V_{OFF}} = \frac{(13V - (3.7V \times 0.1 - 0.2V) + 0.6V) \times 33.2}{3.7V \times 0.1 - 0.2V} \approx 2.62\ k\Omega \tag{31}$$

Chose a standard resistor for the design:

$$R_{TA} = R_{TB} = 2.49\ k\Omega \tag{32}$$

$$C_{TA} = C_{TB} = \frac{1}{R_{SA} \times f_S \times 3} \approx 50\ nF \tag{33}$$

A standard capacitor needs to be chosen for the design:

$$C_{TA} = 47\ nF \tag{34}$$

7 Setting Up Peak Current Limiting (RPK1, RPK2)

The UCC28070 has an adjustable peak current limit comparator that can be set up by selecting R_{PK1} and calculating the required R_{PK2}. For this design to keep the reset voltage of the current sense transformer manageable the peak current sense signal (V_S) was set to 3.7 V.

$$R_{PK2} = \frac{V_S \times R_{PK1}}{V_{REF} - V_S} = \frac{3.7V \times 3.65\ k\Omega}{6V - 3.7V} \approx 5.9\ k\Omega \quad (35)$$

Converter Timing and Maximum Duty Cycle Clamp

Resistor R_{RT} and R_{DMX} set up converter timing and the maximum PWM duty cycle clamp:

$$R_{RT} = \frac{7.5 \times 10^9\ \Omega \times Hz}{f_s} = \frac{7.5 \times 10^9\ \Omega \times Hz}{200\ kHz} = 37.5\ k\Omega \quad (36)$$

A standard resistor was selected for the design:

$$R_{RT} = 37.4\ k\Omega \quad (37)$$

Resistor R_{DMX} was selected to set the maximum duty cycle clamp (D_{MAX}) to 0.97:

$$R_{DMX} = R_{RT}\left(2 \times D_{MAX} - 1\right) = 37.4\ k\Omega\left(2 \times 0.97 - 1\right) = 35\ k\Omega \quad (38)$$

Chose a standard resistor for the design:

$$R_{DMX} = 34.8\ k\Omega \quad (39)$$

8 Programming VOUT

Resistor R_A is selected to minimize the error due to VSENSE input bias current and to minimize loading on the power line when the PFC is disabled. Construct resistor R_A from two or more resistors in series to meet high voltage requirements. Resistor R_B is sized to program the converters output voltage (V_{OUT}).

$$R_A = 3M\Omega \quad (40)$$

$$R_B = \frac{\frac{VREF}{2} \times R_A}{V_{OUT} - \frac{VREF}{2}} = \frac{3V \times 3M\Omega}{390V - 3V} \approx 23.3\ k\Omega \quad (41)$$

A standard resistor was chosen for the design.

$$R_B = 23.2\ k\Omega \quad (42)$$

The resistor divider formed by R_A and R_B from the output voltage to the VSENSE pin also sets the over voltage protection threshold (V_{OVP}).

$$V_{OVP} = 3.18V\ \frac{R_A + R_B}{R_B} = 3.18V\ \frac{3M\Omega + 23.2\ k\Omega}{23.2\ k\Omega} \approx 414V \quad (43)$$

9 VINAC Divider Setup

The UCC28070 also requires sensing the line input for proper operation. This requires a divider from the rectified line voltage to the VINAC pin of the UCC28070. For simplicity the UCC28070 was designed to use the same resistor divider values as the VSENSE pin. Resistors R_A and R_B need to be the same ratio for the VINAC voltage divider as thouse in the VSENSE voltage divider to ensure the UCC28070 controller operates correctly. Please refer to the applications schematic for proper component placement.

10 Voltage Loop Configuration

The methodology used to compensate the voltage loop is based on the compensation methodology developed by Lloyd Dixon. A detailed explanation of this compensation scheme written by Mr. Dixon can be found in the 1990 Unitrode Power Supply Design SEM700, High Power Factor Switching Pre-regulator Design Optimization, Topic 7, reference [2].

Capacitor C_{PV} is sized to attenuate low frequency ripple to less than 3% of the voltage amplifier output range. This will ensure good power factor and low input current harmonic distortion.

Voltage Amplifier Transconductance Amplifier gain:

$$gm_V = 70\ \mu S \tag{44}$$

Voltage Divider Feedback Gain:

$$H = \frac{V_{VREF}}{V_{OUT}} = \frac{3V}{390V} \approx 0.0077 \tag{45}$$

Output impedance (Z_O) is required to attenuate the low frequency boost capacitor output ripple (V_{RIPPLE}) to less than 3% of the effective voltage amplifier output range (ΔVAO). This impedance is set by properly selecting feedback capacitor C_{PV}:

$$Z_O = \frac{\Delta VAO \times 0.03}{V_{RIPPLE} \times H \times gm_V} = \frac{3.2V \times 0.03}{14.5V \times 0.0077 \times 70\ \mu S} \approx 12.3\ k\Omega \tag{46}$$

$$C_{PV} = \frac{1}{2\pi \times 2 \times f_{LINE} \times Z_o} = \frac{1}{2\pi \times 2 \times 47Hz \times 12.3k\Omega} \approx 138nF \tag{47}$$

Choose as standard capacitor for the design:

$$C_{PV} = 150\ nF \tag{48}$$

For the highest possible power factor the voltage loop crossover frequency (f_{CV}) needs to be set based on the following equation:

$$\Delta VAO = 3.2\ V \tag{49}$$

$$f_{CV} = \sqrt{H \times gm_V \times \frac{\frac{P_{OUT}}{\eta}}{\Delta VAO} \times \frac{\frac{1}{j \times 2\pi \times C_{OUT}}}{V_{OUT}} \times \frac{1}{2 \times \pi \times C_{PV}}} \tag{50}$$

$$f_{CV} = \sqrt{0.0077 \times 70\mu S \times \frac{\frac{300W}{0.90}}{3.2V} \times \frac{1}{2 \times \pi \times 200\mu F \times 390V} \times \frac{1}{2 \times \pi \times 150nF}} \approx 11Hz \tag{51}$$

Voltage compensation resistor R_{ZV} is then sized to put a pole at the converter's voltage loop crossover frequency:

$$R_{ZV} = \frac{1}{2\pi \times f_{CV} \times C_{PV}} = \frac{1}{2\pi \times 10.6Hz \times 150nF} \approx 96.4\ k\Omega \tag{52}$$

Select a standard resistor for the design:

$$R_{ZV} = 100\ k\Omega \tag{53}$$

Voltage compensation capacitor C_{ZV} is used to increase the dc gain of the voltage loop and gives some added phase margin before crossover. The zero added to the voltage loop needs to be set at 1/10th the crossover frequency.

$$C_{ZV} = \frac{1}{2\pi \times \frac{f_{CV}}{10} \times R_{ZV}} = \frac{1}{2\pi \times \frac{11Hz}{10} \times 100\ k\Omega} \approx 1.5\ \mu F \tag{54}$$

The following equations can be used to estimate voltage compensation network gain, voltage loop power stage gain and voltage loop gain. These equations can also be used to graphically check loop stability.

Voltage Compensation Network Gain ($G_{CV}(f)$) as function of frequency:

$$G_{CV}(f) = \frac{\Delta V_{VAO}}{\Delta V_{OUT}} = H \times gm_V \times \frac{j \times 2\pi \times f \times R_{ZV} \times C_{ZV} + 1}{\left(j \times 2\pi \times f \times \left(C_{ZV} + C_{PV}\right)\right)\left(\frac{j \times 2\pi \times f \times R_{ZV} \times C_{ZV} \times C_{PV}}{C_{ZV} + C_{PV}} + 1\right)} \quad (55)$$

Voltage Loop Power Stage Gain ($G_{PSV}(f)$) as function of frequency:

$$G_{PSV}(f) = \frac{\Delta V_{OUT}}{\Delta V_{VAO}} = \frac{\frac{P_{OUT}}{\eta}}{\Delta VAO} \times \frac{\left(\frac{1}{j \times 2\pi \times f \times C_{OUT}}\right)}{V_{OUT}} \quad (56)$$

Voltage Loop Gain in dB (TvdB(f)) as function of frequency:

$$TvdB(f) = 20\log\left(\left|G_{PSV}(f) \times G_{CV}(f)\right|\right) \quad (57)$$

Figure 4 shows the theoretical loop gain (TvdB(f)) as a function of frequency and Figure 5 shows the theoretical loop phase ($\theta v(f)$) as a function of frequency. From these figures it can be observed that the voltage loop crossed over at roughly 9 Hz with a phase margin of 60 degrees. Compensating the voltage loop is not an exact science and should be checked with a network analyzer and adjusted if necessary.

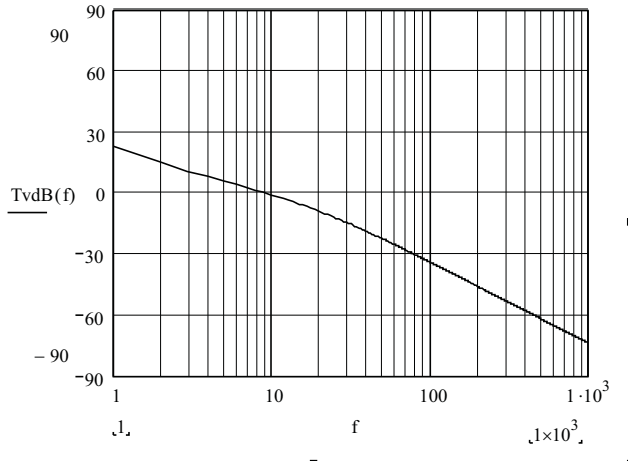

Figure 4. Theoretical Voltage Loop Gain (TvdB(f))

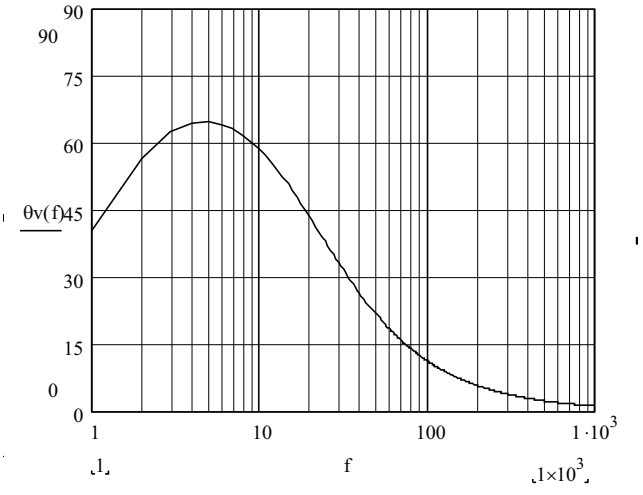

Figure 5. Theoretical Voltage Loop Phase ($\theta v(f)$)

11 Current Loop Compensation

Setting up the current synthesizer is accomplished by correctly selecting R_{SYN}:

The inductor used in this design example swings from 350 μH to 140 μH from no load to maximum load. When calculating R_{SYN} the highest inductance value ($L1_{MAX}$) should be used.

$$R_{SYN} = \frac{N_{CT} \times L1_{MAX} \frac{R_B}{R_A + R_B}}{R_S \times 0.1\ nF} = \frac{50 \times 350\ \mu H \times \frac{23.2\ k\Omega}{3\ M\Omega + 23.2\ k\Omega}}{33.2\Omega \times 0.1nF} \approx 40.5\ k\Omega \quad (58)$$

Chose a standard resistor:

$$R_{SYN} = 38.3\ k\Omega \quad (59)$$

The IMO resistor needs to be set with the following equation to center the digitized multiplier for universal line applications:

$$IMO = \frac{17 \times 10^{-6} A \times V_{INAC}\left(V_{VAOMAX} - 1V\right)}{K_{VFF}} = \frac{17 \times 10^{-6} A \times 0.76V\left(5V - 1V\right)}{0.398V^2} \approx 130\ \mu A \quad (60)$$

$$V_I = \frac{0.76V \times \left(R_A + R_B\right)}{R_B \times \sqrt{2}} = \frac{0.76V \times (3M\Omega + 23.2k\Omega)}{23.2k\Omega \times \sqrt{2}} \approx 70V \quad (61)$$

$$V_2 = \frac{1.1 \times P_{OUT} \times \sqrt{2}}{2 \times \eta \times V1} \times \frac{1}{N_{CT}} \times R_S = \frac{1.1}{2} \times \frac{300W\sqrt{2}}{0.92 \times 72V} \times \frac{1}{50} \times 33.2\Omega \approx 2.458V \quad (62)$$

$$R_{IMO} = \frac{V_2}{IMO} = \frac{2.458\ V}{130\ \mu A} \approx 18.9k\Omega \quad (63)$$

Choose a standard resistor close to the calculated value:

$$R_{IMO} = 19.6\ k\Omega \quad (64)$$

The current loop in a PFC converter is generally designed to crossover at between 1/10th and 1/6th the converter's switching frequency. The current loop in this design example is going to be designed to crossover at 1/10th of the single stage's switching frequency. In order to properly compensate the current loop it is required to calculate the current loop's power stage gain (G_{PS}) at the current loop's crossover and properly select passive components $R_{ZC1/2}$, $C_{ZC1/2}$ and $C_{PC1/2}$:

$$G_{PSC} = \frac{V_{OUT} \times R_S \times \frac{1}{N_{CT}}}{2\pi \times \frac{f_s}{10} \times L1_{AVG} \times V_{RAMP}} = \frac{390\ V \times 33.2\Omega \times \frac{1}{50}}{2\pi \times \frac{200\ kHz}{10} \times 245\ \mu H \times 4.0V} \approx 2.1 \quad (65)$$

Variable gm_C is the current amplifier Transconductance Current Amplifier Gain.

$$gm_C = 100\ \mu S \tag{66}$$

$$R_{ZC1} = R_{ZC2} = \frac{1}{gm_C \times G_{PSC}} = \frac{1}{100\ \mu S \times 2.1} = 4.8\ k\Omega \tag{67}$$

$$C_{ZC1} = C_{ZC2} = \frac{1}{2\pi \frac{f_s}{10} \times R_{ZC}} = \frac{1}{2\pi \frac{200\ kHz}{10} \times 4.8\ k\Omega} \approx 1.7nF \tag{68}$$

$$C_{PC1} = C_{PC2} = \frac{1}{2\pi \frac{fs}{2} \times R_{ZC}} = \frac{1}{2\pi \frac{200\ kHz}{2} \times 4.8\ k\Omega} \approx 333\ pF \tag{69}$$

Standard components close to the calculated values are chosen for the current loop compensation:

$$R_{ZC1} = 4.02\ k\Omega,\ \ C_{ZC1} = 2.2\ nF,\ \ C_{PC1} = 330\ pF \tag{70}$$

Graphically Check Theoretical Current Loop Gain (TcdB(f)) and loop phase (θc(f)): From the plots in Figure 6 and Figure 7 it can be observed that the theoretical loop gain crossed over at roughly 20 kHz with a phase margin of roughly 39 degrees.

$$TcdB(f) = 20\log\left(\left|\frac{V_{OUT} \times Rs \times \frac{N_P}{N_S}}{j \times 2\pi \times f \times L1 \times \Delta V_{RAMP}} \times gm_C \times \frac{j \times 2\pi \times f \times R_{ZC} \times C_{ZC} + 1}{\left(j \times 2\pi \times f \times (C_{ZC} + C_{PC})\right)\left(\frac{j \times 2\pi \times f \times R_{ZC} \times C_{ZC} \times C_{PC}}{C_{ZC} + C_{PC}} + 1\right)}\right|\right) \tag{71}$$

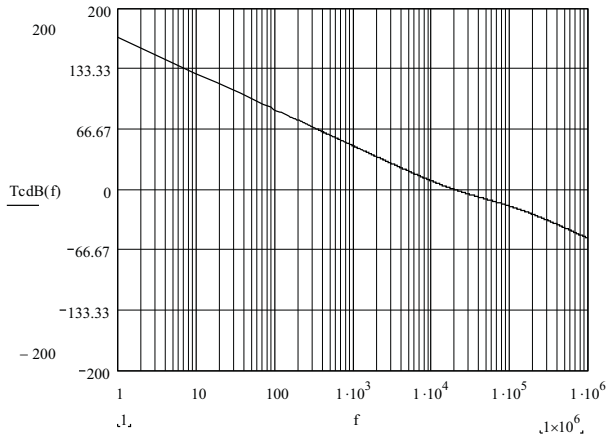

Figure 6. Current Loop Gain (TdB(f))

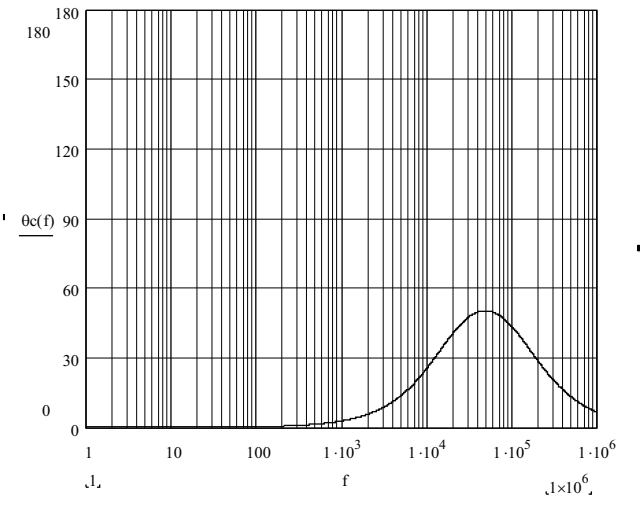

Figure 7. Current Loop Phase (θc(f))

12 Soft Start

To have a controlled soft start the C_{SS} capacitor needs to be set to at least the same value as the C_{ZV} capacitor or larger. This means the design has a minimum soft start time based on the C_{ZV} capacitor

$$t_{SSMIN} = \frac{2.25\ V \times C_{ZV}}{10\ \mu A} = \frac{2.25V \times 1.5\ \mu F}{10\ \mu A} \approx 338\ ms \quad (72)$$

$$C_{SS} \geq C_{ZV} \quad (73)$$

The soft-start timing can be set with timing capacitor C_{SS} once the amount of soft start time (t_{SS}) has been determined. Our original design requirement was to have 200 ms of soft-start time. The calculated capacitance needed for this soft-start time is less than the minimum required capacitance.

$$C_{ss} = \frac{10\ \mu A \times t_{ss}}{2.25V} = \frac{10\ \mu A \times 200\ ms}{2.25\ V} \approx 0.889\ \mu F \quad (74)$$

A C_{SS} capacitor value equal to the C_{ZV} capacitor was chosen for the design.

$$C_{ss} = 1.5\ \mu F \quad (75)$$

13 Spread Spectrum Reduces EMI

It has been shown that dithering the converter's switching frequency can reduce EMI. Resistor R_{RDM} and C_{CDR} program the frequency dithering magnitude and rate. For this design the frequency dither magnitude (f_{DM}) was set to 30 kHz and the frequency dither rate (f_{DR}) was set to 10 kHz. The frequency will dither around the typical frequency programmed by resistor R_{RT}. In this example the frequency will dither from roughly 185 kHz to 215 kHz at a 10 kHz rate.

$$f_{DM} = 30\ kHz \quad (76)$$

$$f_{DR} = 10kHz \quad (77)$$

$$R_{RDM} = \frac{937.5 \times 10^{6}\Omega}{f_{DM}} = \frac{937.5 \times 10^{6}\Omega}{30\ kHz} = 31.13\ k\Omega \quad (78)$$

$$C_{CDR} = \frac{0.0667 \times 10^{-9}F \times R_{RDM}}{f_{RD}} = \frac{0.0667 \times 10^{-9}F \times 31.13\ k\Omega}{10\ kHz} = 208\ pF \quad (79)$$

A standard resistor and capacitor are chosen for the design:

$$R_{RDM} = 31.6\ k\Omega \quad (80)$$

$$C_{CDR} = 220pF \quad (81)$$

14 Recommended PCB Device Layout

Interleaved PFC techniques dramatically reduce input and output ripple current caused by the PFC boost inductor, which allows the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the output filter capacitor should be located after the two phases allowing the current of each phase to be combined together before entering the boost capacitor. Similar to other power management devices, when laying out the PCB it is important to use star grounding techniques and to keep filter and high frequency bypass capacitors as close to the device pins and ground pin as possible. To minimize the interference caused by magnetic coupling from the boost inductor, the device should be located at least one inch away from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements. To verify the application a 300-W interleaved prototype was constructed and evaluated. This prototype consisted of mother board that was the power stage and a daughter board that consisted of the control circuitry. Refer to Figure 8 through Figure 13 for schematics and a recommended layout. The daughter board controller has two jumpers JP1 and JP2. If these jumpers are open the evaluation module is running with frequency dithering. If these jumpers are shorted frequency dither is disabled and the EVM can be synchronized through the sync input.

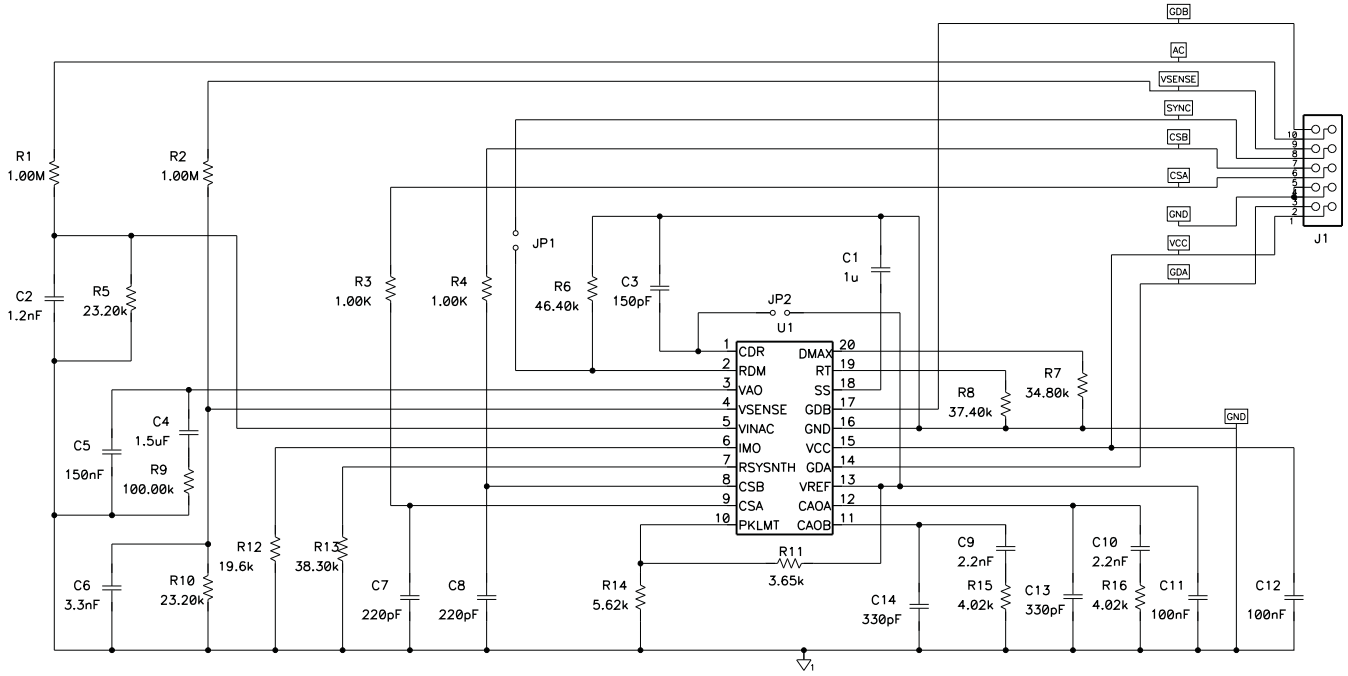

Figure 8. 300-W Prototype Daughter Board Controller Schematic

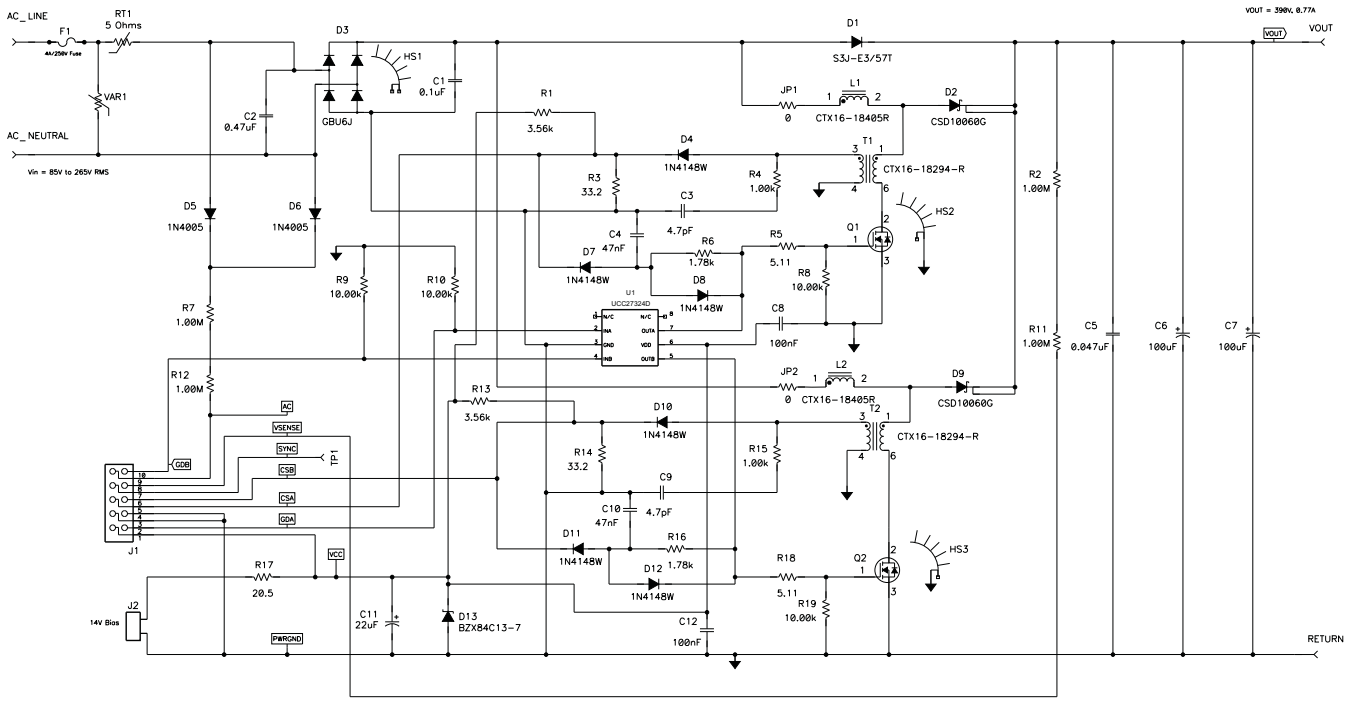

Figure 9. 300-W Prototype Mother Board Power Stage

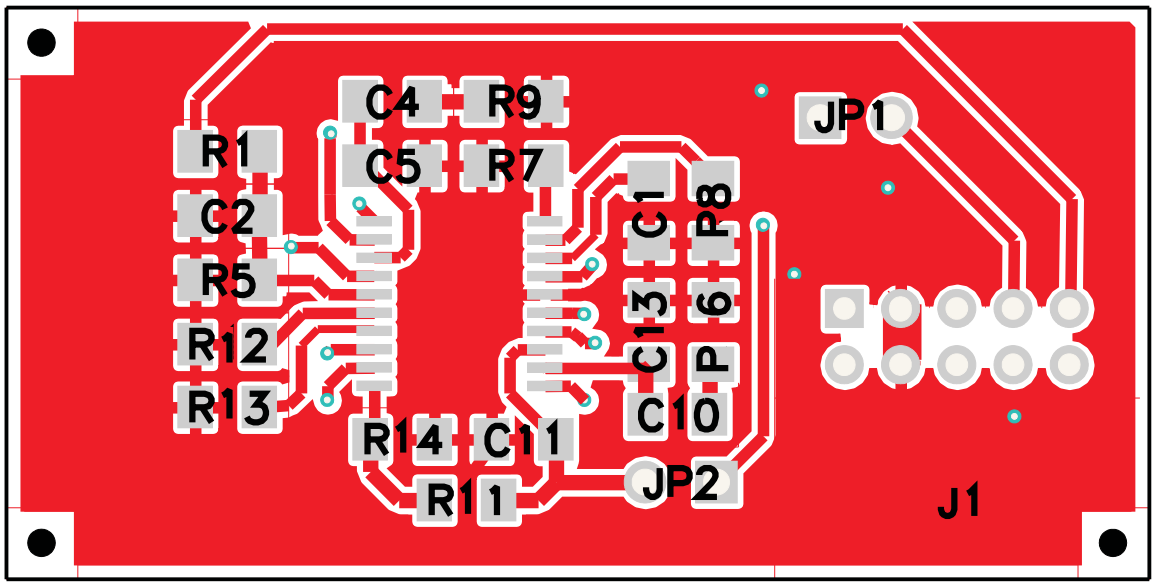

Figure 10. Daughter Board Layout Front

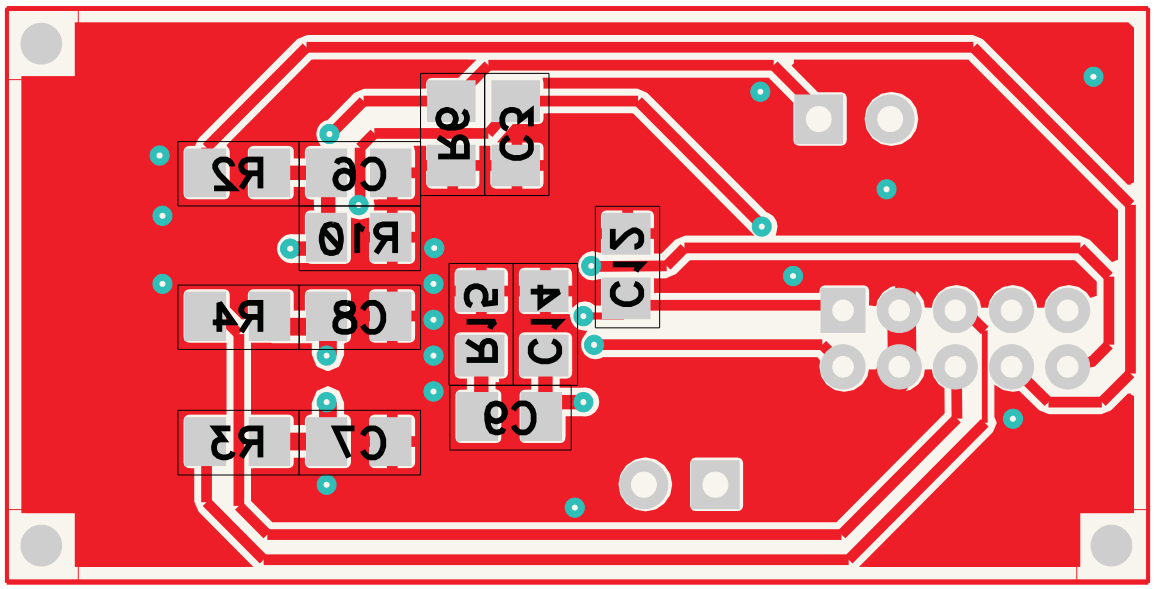

Figure 11. Daughter Board Layout Back

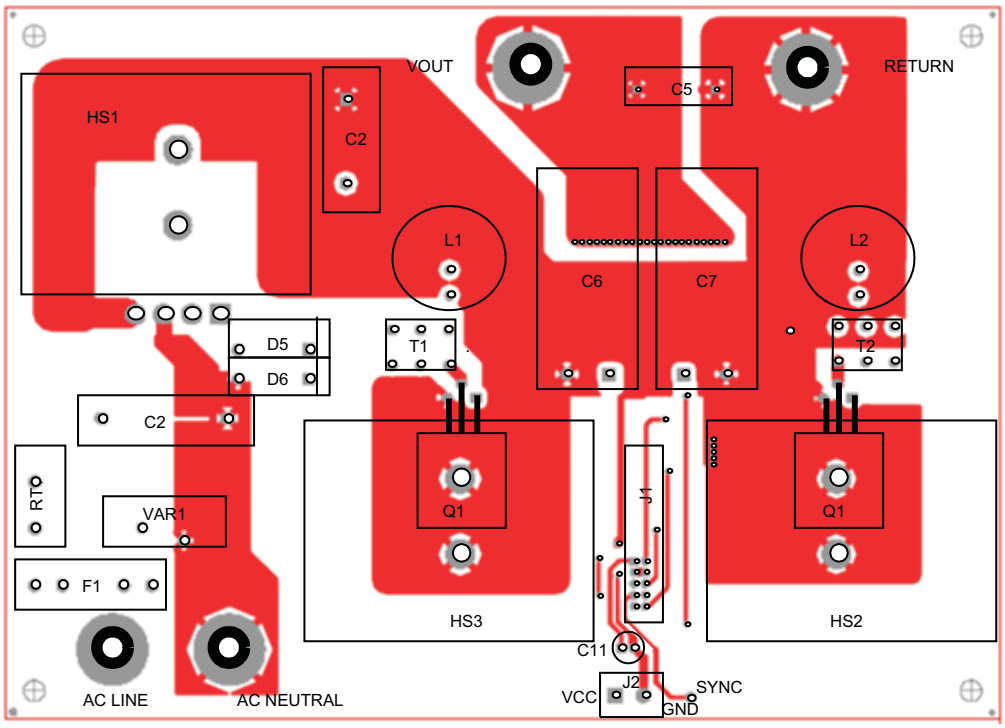

Figure 12. Mother Board Layout Front

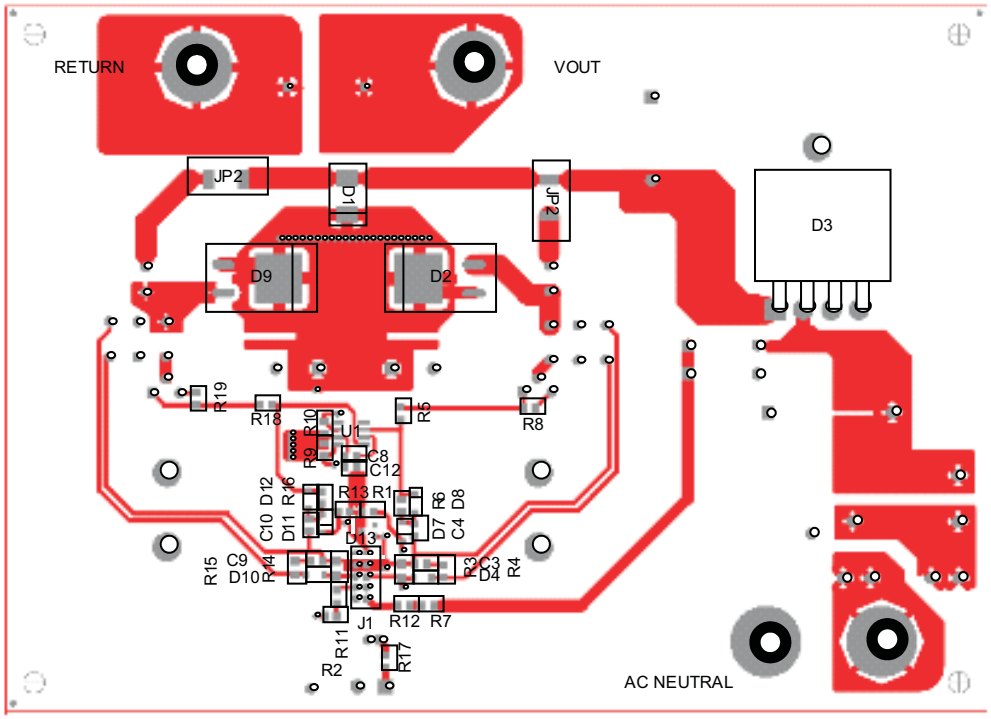

Figure 13. Mother Board Bottom

15 Efficiency Curves

A 300-W prototype was built based on the design information presented in this application note. The following graphs show the performance of this EVM.

15.1 Prototype Efficiency

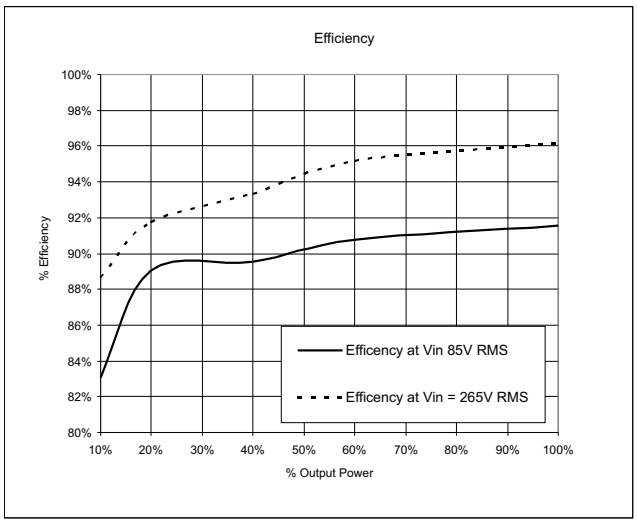

Figure 14.

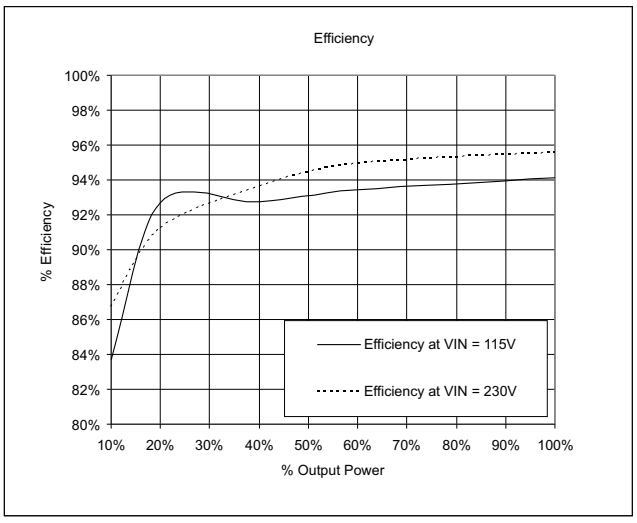

Figure 15.

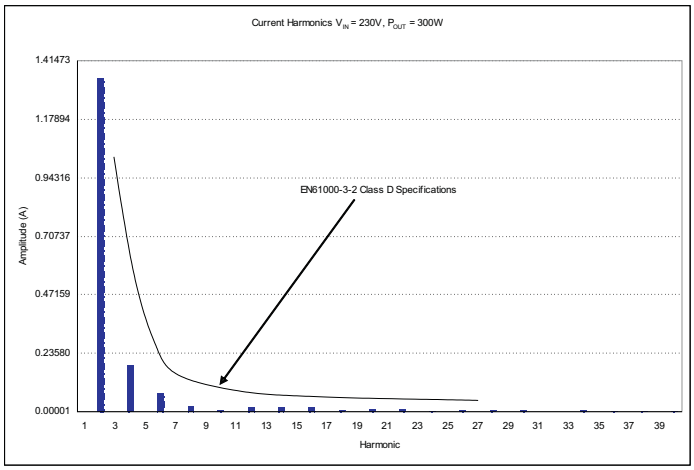

Figure 16. Prototype Harmonic Content at V_{IN} = 230 V, P_{OUT} = 300 W

15.2 Prototype Power Factor

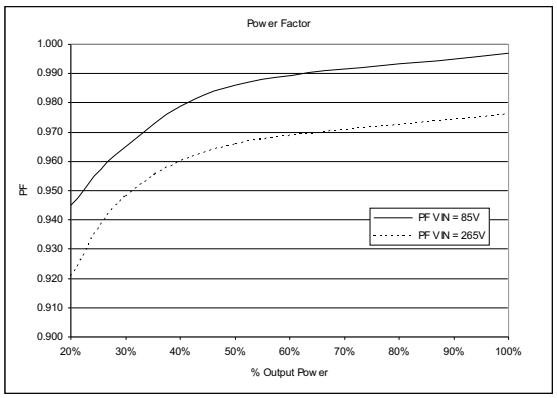

Figure 17.

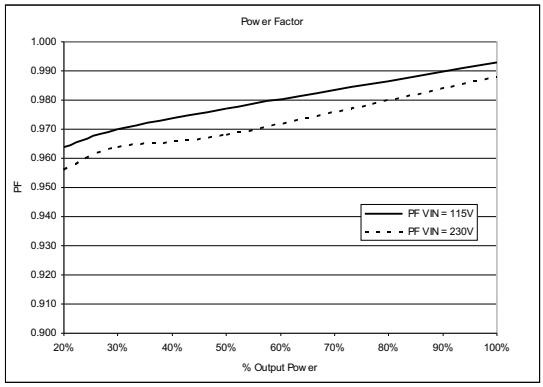

Figure 18. Input Current and Output Ripple Voltage at Maximum Output Power Ch2 = IIN, CH2 = VOUT

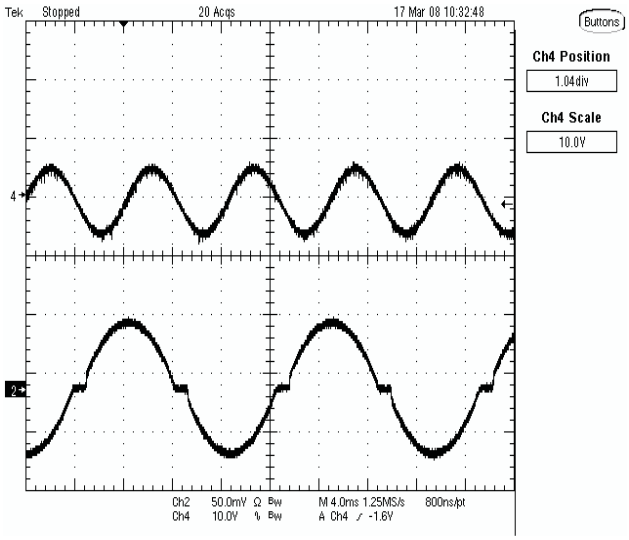

Figure 19. V_{IN} = 85 V RMS

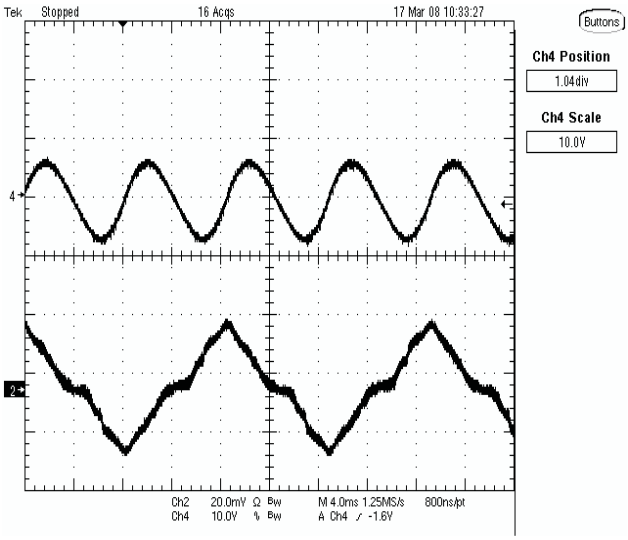

Figure 20. V_{IN} = 265 V RMS

15.3 Inductor Ripple Current Cancellation, CH2=IL1, CH3=IL2, M1=IL1+IL2

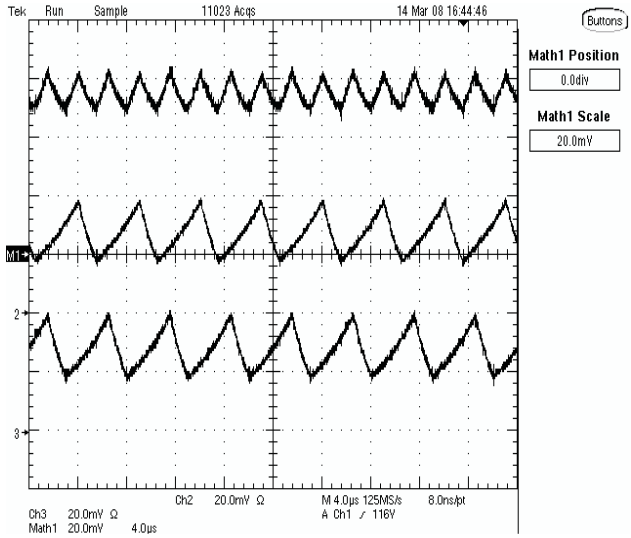

Figure 21. V_{IN} = 85 V RMS, Peak of Line

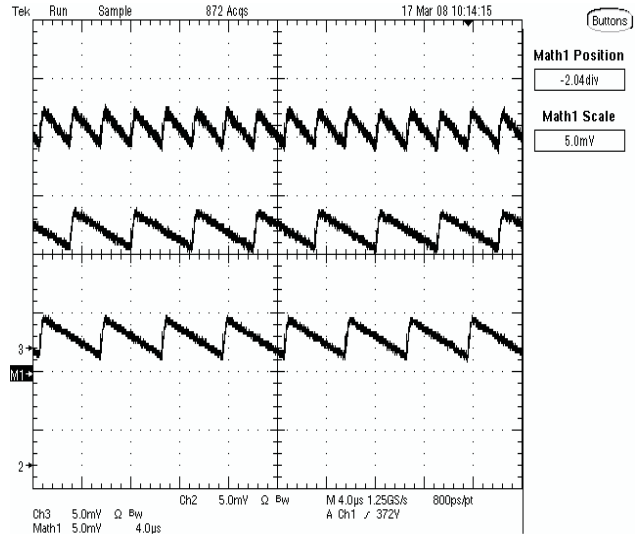

Figure 22. V_{IN} = 265V RMS, Peak of Line

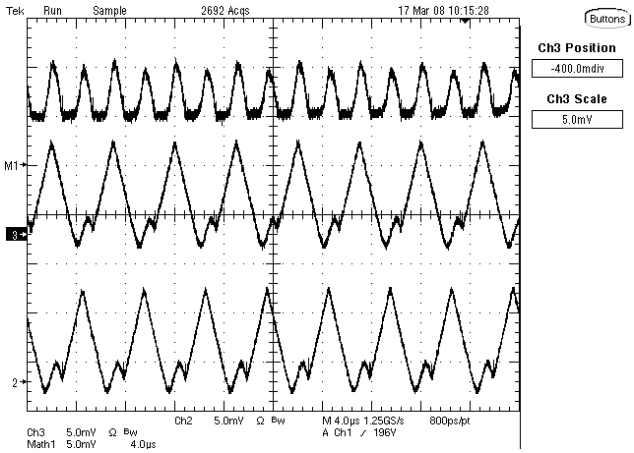

Figure 23. V_{IN} = 265V RMS, Line Voltage at Half the Output Voltage

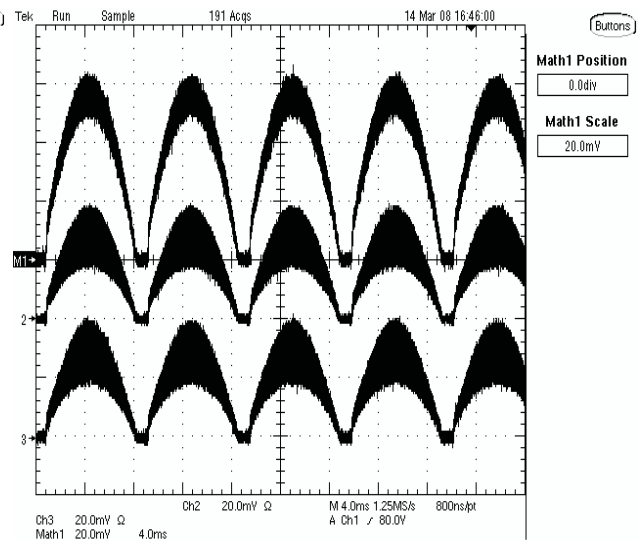

Figure 24. VIN = 85 V, POUT = 300 W

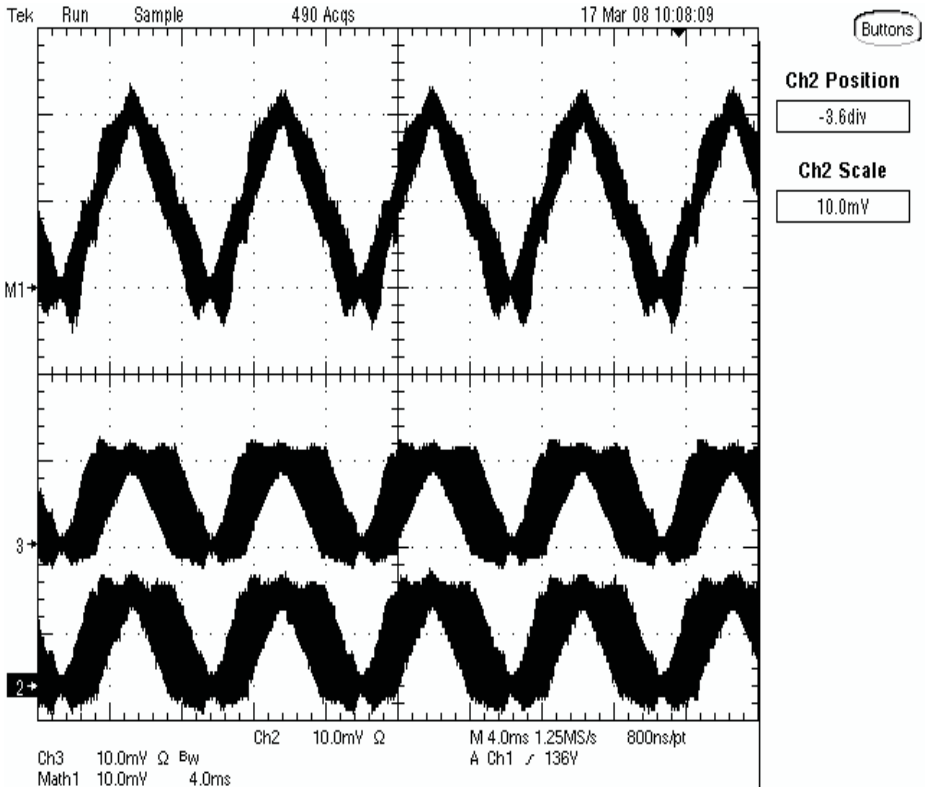

Figure 25. VIN = 265 V, POUT = 300 W

15.4 Recovery from Line Dropout, CH1= Rectified Line Voltage, CH2=IL1, CH3=IL2, CH4 = VOUT

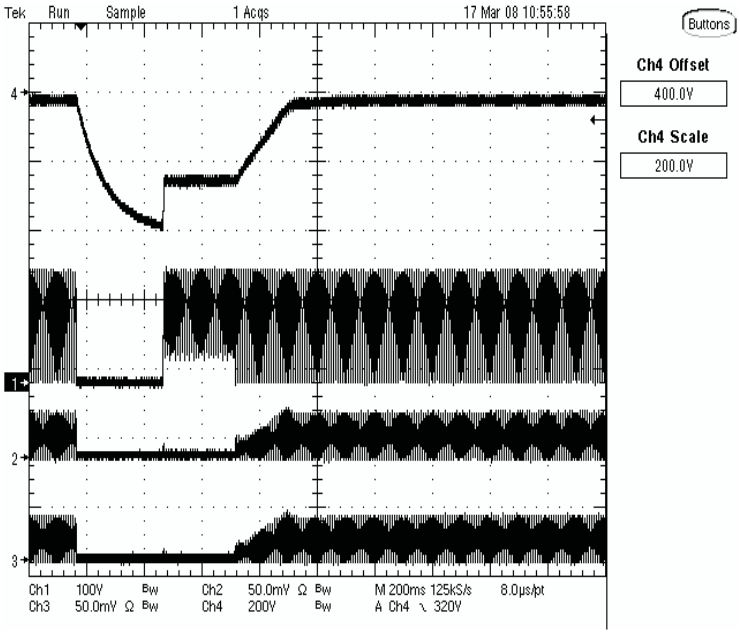

Figure 26. Brownout at V_{IN} = 115V, P_{OUT} = 300 W

15.5 Startup, CH2 = IL1, CH3 = IL2, CH4 = V_{OUT}

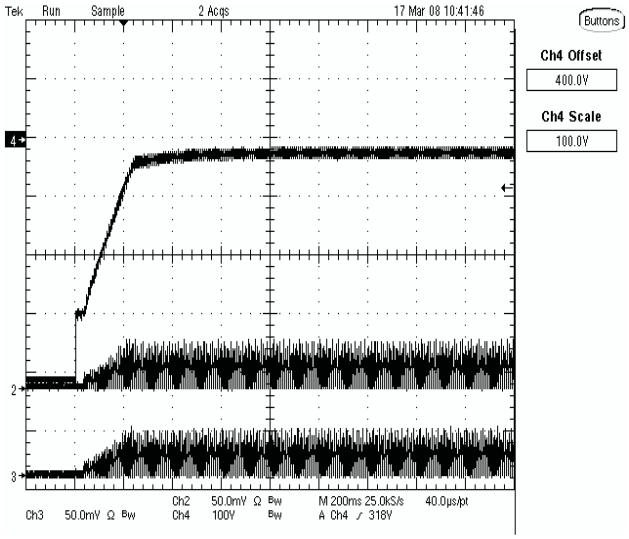

Figure 27. V_{IN} = 85 V, P_{OUT} = 300 W

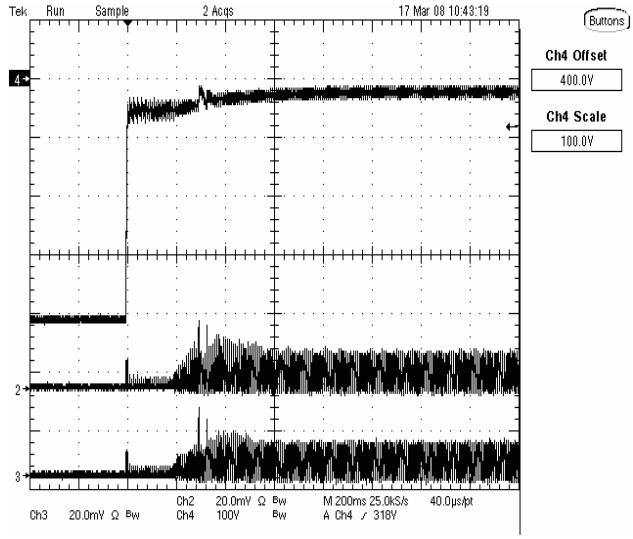

Figure 28. V_{IN} = 265 V, P_{OUT} = 300 W

15.6 EMI Measurements

When dithering was applied to the EVM a 4.35dBuV reduction in the Quasi Peak (QP) measurement was observed. Note a filter was added to the front end of the EVM to clean up some of the noise to take EMI data. Depending on the filter the amount of EMI will vary. Also, this filter was not setup to pass EMI requirements but to show frequency dither reduced EMI.

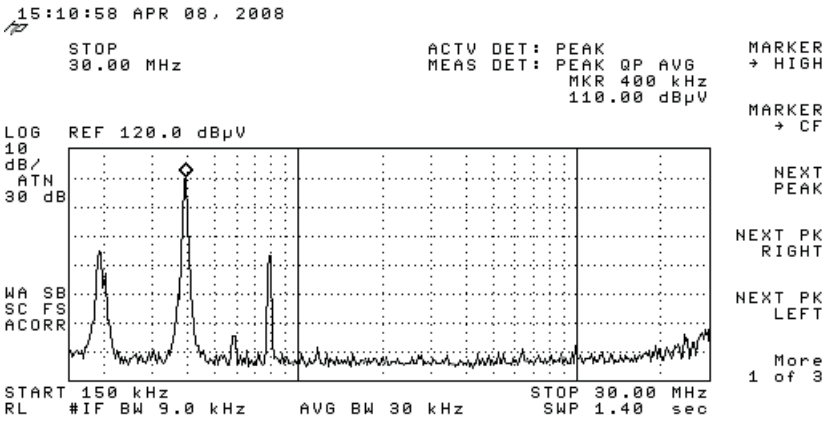

Figure 29. EMI Quasi Peak (QP) Measurement with out Frequency Dithering, No EMI Filter Present

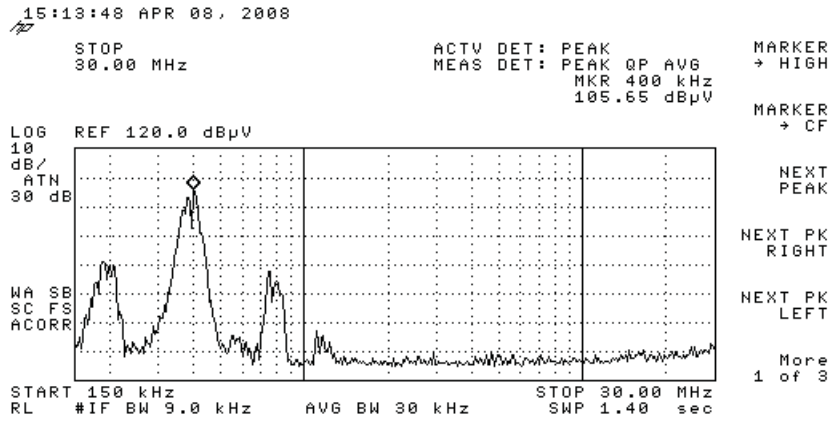

Figure 30. EMI Quasi Peak (QP) Measurement with Frequency Dithering, No EMI filter Present

16 References

1. Lazlo Balogh and Richard Redi, *Power Factor Correction with Interleaved Boost*, APEC 1993, pp. 168-174
2. Lloyd Dixon, *High Power Factor Switching Pre-regulator Design Optimization*, Unitrode Power Supply Design Seminar SEM-700, 1990, Topic 7
3. Brett Miwa, David Otten, Martin F. Schlecht, *High Efficiency Power Factor Correction Using Interleaved Techniques* IEEE 1992, pp. 557 to 568
4. Michael O'Loughlin, *350W, Two Phase Interleaved PFC Pre-regulator Design Review*, Texas Instrument Literature Number SLUA369, 2006
5. Michael O'Louglin, *An Interleaving PFC Pre-Regulator for High-Power Converters* Unitrode/TI Power Supply Design Seminar SEM-1700, Topic 5
6. P. Zumel, O. Garcia, J. A. Cobos, J. Uceda, *EMI Reduction by Interleaving of Power Converters Presentation*, APEC 2004
7. *UCC28070 Data Sheet*, Texas Instruments Literature Number SLUS794, http://focus.ti.com/lit/ds/symlink/ucc28070.pdf

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