Application Report
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Configuring the bq20z40/bq20z45 Data Flash

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ABSTRACT

The bq20z40/bq20z45 has numerous data flash constants that can be used to configure the device with a variety of different options for most features. The data flash of the bq20z40/bq20z45 is split into sections which are described in detail within this document.

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1 Glossary

RSOC: Relative state of Charge

ASOC: Absolute State of Charge

Bit: This word has a different meaning than Flag. This word is used to refer to a configuration setting bit. It is primarily used in data flash settings.

Cell Voltage(Max): This represents the maximum value among all the SBS cell voltage registers.(***Cell Voltage 1*** through ***Cell Voltage 4***)

Cell Voltage(Min): This represents the minimum value among all the SBS cell voltage registers.(***Cell Voltage 1*** through ***Cell Voltage 4***)

Cell Voltage(Any): This represents any of the possible SBS cell voltage registers.(***Cell Voltage 1*** through ***Cell Voltage 4***)

[DSG] in ***Battery Status***: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. This can be confused in many descriptions in this document because different functions require different methods for determining charging or discharging. The SBS description sometimes does not give enough resolution for correct part function so these functions require other data flash registers as described in their respective definitions. SBS states that if the battery is charging then [DSG] is 0, and any other time (Current less than or equal to 0), the [DSG] flag is set. The actual formula that the bq20z40/bq20z45 uses for setting or clearing the [DSG] flag are as follows:

[DSG] clear: [DSG]=0 if ***Current*** ≥ *Chg Current Threshold*

[DSG] set: [DSG]=1 if

1. Current ≤ *Dsg Current Threshold* or
2. Relaxation Mode which is defined by one of the following statements:
   A) ***Current*** transitioning from below (–)*Quit Current* to (above (–)*Quit Current* and below *Quit Current*) for *Dsg Relax Time*
   B) ***Current*** transitioning from above *Quit Current* to (below *Quit Current* and above (–)*Quit Current*) for *Chg Relax Time*

FCC: Full Charge Capacity

FET opened/Closed: It is common to say FET opened or FET closed. This is used throughout this document to mean the FET is turned off or the FET is turned on respectively.

Flag: This word is usually used to represent a read only status bit that indicates some action has occurred or is occurring. This bit usually cannot be modified by the user.

Precharge/ZVCHG: The words Precharge and ZVCHG are interchangeable throughout the document

RCA: Remaining Capacity Alarm

RM: Remaining Capacity

RSOC: Relative state of Charge

RTA: Remaining Time Alarm

SOC: This is used as a generic meaning of State-of-Charge. It can mean RSOC, ASOC, or percentage of actual chemical capacity.

System: The word system is sometimes used in this document. It always means a host system that is consuming current from the battery pack that includes the bq20z40/bq20z45.

Italics: All words in this document that are in italics represent names of data flash locations exactly as they are shown in the EV software.

Bold: All words that are bold italic represent SBS compliant registers exactly as they are shown in the EV software.

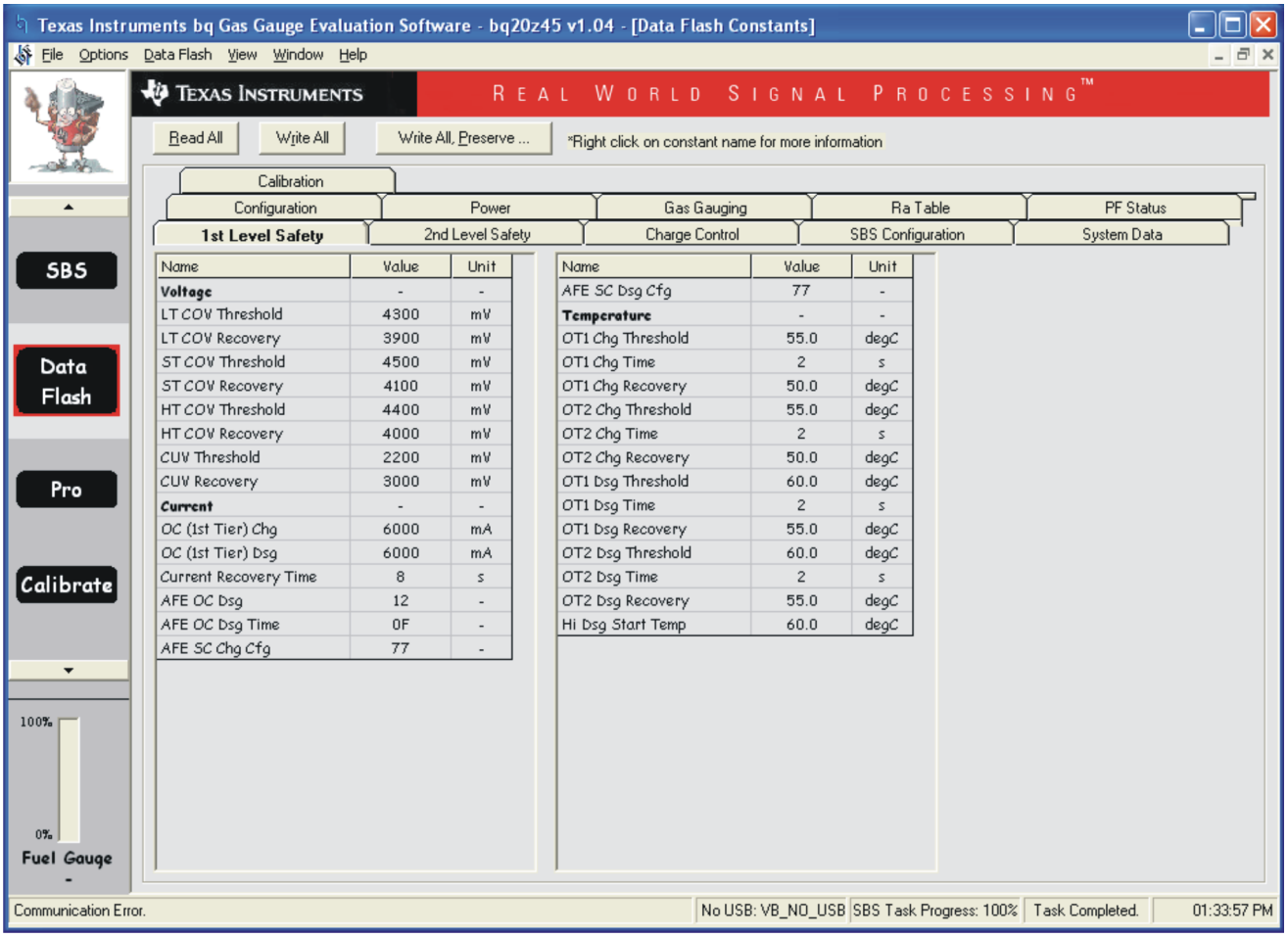
[brackets]: All words or letters in brackets represent bit/flag names exactly as they are shown in the SBS and Data Flash in the EV software.

(–): This is commonly used in this document to represent a minus sign. It is written this way to ensure that the sign is not lost in the translation of formulas in the text of this document.

2 Data Flash Descriptions

2.1 1st Level Safety

All 1st Level Safety functions are temporary. There should be no permanent failures or damage to the battery if any of the 1st Level Safety functions are triggered.



2.2 Voltage

LT COV Threshold

When the temperature is between *JT1* and *JT2*, and any cell voltage measured by Cell Voltage (Any) rises up to this threshold, then the Cell Over Voltage (COV) protection process is triggered, initiating a [COV] detection sequence for 2 seconds. If the COV condition clears prior to the expiration of the 2 second timer, then the [COV] detection sequence will be cleared and no [COV] flag will be set in **Safety Status**. If the COV condition does not clear then [COV] will be set in **Safety Status** and the Charge FET will be opened. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0.

Normal Setting: Default is 4300 mV. This cell is chemistry dependent.

LT COV Recovery

When the temperature is between *JT1* and *JT2*, and a [COV] is set in **Safety Status**, it can only be cleared when ALL cell voltages as measured by Cell Voltage(All) fall below this threshold.

Normal Setting: This defaults to 3900 mV. Set low enough that the hysteresis between *COV Threshold* fault and this recovery prevents oscillation of the Charge FET.

ST COV Threshold

When the temperature is between *JT2* and *JT3*, and any cell voltage measured by Cell Voltage (Any) rises up to this threshold, then the Cell Over Voltage (COV) protection process is triggered, initiating a [COV] detection sequence for 2 seconds. If the COV condition clears prior to the expiration of the 2 second timer, then the [COV] detection sequence will be cleared and no [COV] flag will be set in **Safety Status**. If the COV condition does not clear then [COV] will be set in **Safety Status** and the Charge FET will be opened. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0.

Normal Setting: Default is 4500 mV. This cell is chemistry dependent.

ST COV Recovery

When the temperature is between *JT2* and *JT3*, and a [COV] is set in **Safety Status**, it can only be cleared when ALL cell voltages as measured by Cell Voltage(All) fall below this threshold.

Normal Setting: This defaults to 4100 mV. Set low enough that the hysteresis between *COV Threshold* fault and this recovery prevents oscillation of the Charge FET.

HT COV Threshold

When the temperature is between *JT3* and *JT4*, and any cell voltage measured by Cell Voltage (Any) rises up to this threshold, then the Cell Over Voltage (COV) protection process is triggered, initiating a [COV] detection sequence for 2 seconds. If the COV condition clears prior to the expiration of the 2 second timer, then the [COV] detection sequence will be cleared and no [COV] flag will be set in **Safety Status**. If the COV condition does not clear then [COV] will be set in **Safety Status** and the Charge FET will be opened. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0.

Normal Setting: Default is 4400 mV. This cell is chemistry dependent.

HT COV Recovery

When the temperature is between *JT3* and *JT4*, and a [COV] is set in **Safety Status**, it can only be cleared when ALL cell voltages as measured by Cell Voltage(All) fall below this threshold.

Normal Setting: This defaults to 4000 mV. Set low enough that the hysteresis between *COV Threshold* fault and this recovery prevents oscillation of the Charge FET.

CUV Threshold

When any cell voltage measured by ***Cell Voltage(Any)*** falls below this threshold then the Cell Under Voltage (CUV) detection process is triggered. If the CUV condition clears within a 2 second timer window then the CUV detection process is cleared and no [CUV] is set in **Safety Status**. If the CUV condition does not clear then a [CUV] is set in **Safety Status** and the Discharge FET is opened. This fault condition causes [TDA] and [FD] in **Battery Status** to be set. It also causes [XDSG] in **Operation Status**.

Normal Setting: Default is 2200 mV. This is cell chemistry dependent by 2200 mV–2300 mV is the most common setting

CUV Recovery

When [CUV] is set in ***Safety Status***, it can only be cleared when **ALL** cell voltages as measured by ***Cell Voltage(All)*** rise above this threshold.

Normal Setting: The default for this register is 3000 mV. Set high enough that the hysteresis between *CUV Threshold* fault and this recovery prevents oscillation of the Discharge FET.

2.3 Current

There are 2 levels or tiers of current protection in the bq20z40/bq20z45. The first 2 levels, 1st Tier and 2nd Tier is slow responding (>1 second). The 2nd level (denoted by AFE in the labels of the data flash locations) is a very quick responding current protection controlled directly by the bq29330.

NOTE: IT is important to note that the AFE makes the triggering decision for any of the AFE fault conditions. This is to ensure quick response to dangerous faults that could not only cause damage but also hazards. It is also designed in such a way that the AFE can act completely autonomously in the event of damage to the gauge in the triggering of any AFE fault. The AFE cannot, however, clear the fault condition. It is cleared only by the gauge. The AFE data is transferred to the AFE on reset and (if enabled in the **AFE Verification** subclass) is continually monitored by the gauge to ensure no corruption has occurred at any time. If corruption has occurred the gauge will attempt to correct it and if after repeated attempts (as set in the **AFE Verification** subclass) it cannot correct the condition then it will set a permanent failure. If enabled in *Permanent Fail Cfg*, then the SAFE pin is driven high on the gauge. (See *Permanent Fail Cfg*)

OC (1st Tier) Chg

When current measured by ***Current*** reaches up to or above this threshold during charging then the 1st Tier Over Current in Charge [OCC] detection process is triggered. If the 1st Tier OCC condition clears prior to the expiration of a 2 second timer, then [OCC] detection process is cleared and no [OCC] is set in ***Safety Status***. If the 1st Tier OCC condition does not clear then a [OCC] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.

Normal Setting: This register is application dependent. It should be set above the absolute maximum expected discharge current. It should be set high enough that unexpected mild charge spikes or inaccuracies will not create a false over current trigger but low enough to force the Charge FET to open before damage can occur to the pack.

OC (1st Tier) Dsg

When current measured by ***Current*** falls down to or below this threshold during discharging then the 1st Tier Over Current in discharge (OCD) detection process is triggered. If the 1st Tier OCD condition clears prior to the expiration of 2 second timer, then no [OCD] is set is ***Safety Status***. If the 1st Tier OCD condition does not clear then [OCD] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [XDSG] and [XDSGI] in ***Operation Status*** to be set. It also causes ***Charging Current*** to be set to 0.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent. It should be set **below** the absolute maximum expected discharge current. It should be set **low** enough that unexpected mild discharge spikes or inaccuracies will not create a false over current trigger but **high** enough to force the Discharge FET open before damage can occur to the pack.

Current Recovery Timer

The *Current Recovery Timer* is used in the recovery process of any of the over current fault conditions. After a fault condition exists, depending on if enabled, the fault condition is cleared only after *Current Recovery Timer* time in seconds with ***AverageCurrent*** falling below the corresponding recovery threshold in the charge direction or rising above the corresponding recovery threshold in the discharge direction. The corresponding recovery does not happen immediately after the recovery condition exits. As soon as the recovery condition exists then the *Current Recovery Time* timer starts and the condition clears and the corresponding FET is enabled after the *Current Recovery Time* timer expires. This timer is associated with the following Fault Conditions as described in this section:

1. *OC (1st Tier) Dsg*
2. *OC (1st Tier) Chg*
3. *AFE OC Dsg*
4. *AFE SC Dsg*
5. *AFE SC Chg*

This Recovery method is enabled if [NR] is set in *Operation Cfg B*, or if ([NR] is cleared and the corresponding bits are set in the *Non-Removable Cfg* register:

1. *OC (1st Tier) Dsg* [OCD]
2. *OC (1st Tier) Chg* [OCC]
3. *AFE OC Dsg* [AOCD]
4. *AFE SC Dsg* [SCD]
5. *AFE SC Chg* [SCC]

Normal Setting: The default for this register is 8 seconds. This is a recommended number to prevent heating up in the corresponding FET.

AFE OC Dsg

See the important note about all AFE fault conditions at the beginning of the **Current** section.

This is the third level Over Current protection in the discharge direction. This is a last effort protection function before using the Permanent Fail Functions in the Second Level Safety Class. This register displays in HEX using the EV Software. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If the *AFE OC DSG* condition exists for *AFE OC Dsg Time* in milliseconds, then the discharge FET opens as controlled by the bq29330. This fault condition causes [AOCD] to be set in ***Safety Status*** and [XDSG], [XDSGI] is set in ***Operation Status***, and [TDA] is set in ***Battery Status***. It also causes ***Charging Current*** to be set to 0. See Table 1 for settings for this register.

Table 1. AFE OC Dsg Configuration

0X00	0.050 V	0x08	0.090 V	0x10	0.130 V	0x18	0.170 V
0x01	0.055 V	0x09	0.095 V	0x11	0.135 V	0x19	0.175 V
0x02	0.060 V	0x0a	0.100 V	0x12	0.140 V	0x1a	0.180 V
0x03	0.065 V	0x0b	0.105 V	0x13	0.145 V	0x1b	0.185 V
0x04	0.070 V	0x0c	0.110 V	0x14	0.150 V	0x1c	0.190 V
0x05	0.075 V	0x0d	0.115 V	0x15	0.155 V	0x1d	0.195 V
0x06	0.080 V	0x0e	0.120 V	0x16	0.160 V	0x1e	0.200 V
0x07	0.085 V	0x0f	0.125 V	0x17	0.165 V	0x1f	0.205 V

Normal Setting: Note that the maximum value for this register is 0x1F. Values above 0x1F cause unpredictable results. This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is **below** the *OC (2nd Tier) Dsg* given the application sense resistor value.

AFE OC Dsg Time

This is the time after detection of an *AFE OC Dsg* fault before the Discharge FET attempts to open. This trigger function is completely controlled by the bq29330. The setting of this register is in HEX, and it is in milliseconds (See *AFE OC Dsg*). See Table 2 for setting for this register.

Table 2. AFE OC Dsg Time Configuration

0x00	1 ms	0x04	9 ms	0x08	17 ms	0x0c	25 ms
0x01	3 ms	0x05	11 ms	0x09	19 ms	0x0d	27 ms
0x02	5 ms	0x06	13 ms	0x0a	21 ms	0x0e	29 ms
0x03	7 ms	0x07	15 ms	0x0b	23 ms	0x0f	31 ms

Normal Setting: Note that the maximum value for this register is 0x0F. Values above 0x0F will cause unpredictable results. This register is completely application specific. It should be set long enough to prevent false triggering of the [AOCD] in ***Safety Status***, but short enough to prevent damage to the battery pack.

AFE SC Chg Cfg

See the **NOTE** at the beginning of the Current section for an important note about all AFE fault conditions.

This register includes 2 settings. The registers are refered to as *AFE SC Chg* and *AFE SC Chg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4-7) sets the time for the AFE short circuit in the Charge direction fault detection time (*AFE SC Chg Time*). The least significant nibble (bits 0-3) set the threshold at which the bq29330 detects a AFE short circuit fault (*AFE SC Chg*). This is an extreme condition with settings for very large voltages and very short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Charge FET opens as controlled by the bq29330. This fault condition causes [SCC] to be set in ***Safety Status***, and [TCA] to be set in ***Battery Status***. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. See Table 4 for settings for this register.

Table 3. AFE SC Chg Cfg Bit Description

7	6	5	4	3	2	1	0
SCCT3	SCCT2	SCCT1	SCCT0	SCCV3	SCCV2	SCCV1	SCCV0
AFE SC Chg Time				*AFE SC Chg*			

Table 4. AFE SC Chg Cfg Least Significant Nibble (SCCV3-SCCV0)

0x00	0.100 V	0x04	0.200 V	0x08	0.300 V	0x0c	0.400 V
0x01	0.125 V	0x05	0.225 V	0x09	0.325 V	0x0d	0.425 V
0x02	0.150 V	0x06	0.250 V	0x0a	0.350 V	0x0e	0.450 V
0x03	0.175 V	0x07	0.275 V	0x0b	0.375 V	0x0f	0.475 V

Table 5. AFE SC Chg Cfg Most Significant Nibble (SCCT3-SCCT0)

0x00	0 µs	0x04	244 µs	0x08	488 µs	0x0c	732 µs
0x01	61 µs	0x05	305 µs	0x09	549 µs	0x0d	793 µs
0x02	122 µs	0x06	366 µs	0x0a	610 µs	0x0e	854 µs
0x03	183 µs	0x07	427 µs	0x0b	671 µs	0x0f	915 µs

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is sufficiently above *OC (2nd Tier) Chg*.

AFE SC Dsg Config

See the important note about all AFE fault conditions at the beginning of the Current section.

This register includes 2 settings. See these as *AFE SC Dsg* and *AFE SC Dsg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4–7) sets the time for the AFE short circuit in the discharge direction fault detection time (*AFE SC Dsg Time*). The least significant nibble (bits 0–3) sets the threshold at which the bq29330 detects an AFE short circuit fault in the discharge direction (*AFE SC Dsg*). This is an extreme condition with settings for very large voltages and very short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Discharge FET opens as controlled by the bq29330. This fault condition causes [SCD] to be set in ***Safety Status***, [XDSG] and [XDSGI] to be set in ***Operation Status***, and [TDA] to be set in ***Battery Status***. See Table 7 and Table 8 for settings for this register.

Table 6. AFE SC Dsg Cfg Bit Description

7	6	5	4	3	2	1	0
SCDT3	SCDT2	SCDT1	SCDT0	SCDV3	SCDV2	SCDV1	SCDV0
AFE SC Dsg Time				*AFE SC Dsg*			

Table 7. AFE SC Dsg Cfg Least Significant Nibble (SCDV3-SCDV0)

0x00	0.10 V	0x04	0.20 V	0x08	0.30 V	0x0c	0.40 V
0x01	0.125 V	0x05	0.225 V	0x09	0.325 V	0x0d	0.425 V
0x02	0.150 V	0x06	0.250 V	0x0a	0.350 V	0x0e	0.450 V
0x03	0.175 V	0x07	0.275 V	0x0b	0.375 V	0x0f	0.475 V

Table 8. AFE SC Dsg Cfg Most Significant Nibble (SCDT3-SCDT0)

0x00	0 µs	0x04	244 µs	0x08	488 µs	0x0c	732 µs
0x01	61 µs	0x05	305 µs	0x09	549 µs	0x0d	793 µs
0x02	122 µs	0x06	366 µs	0x0a	610 µs	0x0e	854 µs
0x03	183 µs	0x07	427 µs	0x0b	671 µs	0x0f	915 µs

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required to determine the proper setting for this register. Be sure that this value is **below** AFE OC Dsg.

2.4 Temperature

OT1 Chg Threshold

When the temperature measured by TS1 rises up to or above this threshold while charging (**Current** > *Chg Current Threshold*) then the TS1 Over Temperature in charge direction (OT1C) detection process is triggered. If the OT1C condition clears within *OT1 Chg Time* seconds, then no [OT1C] will be set in **Safety Status**. If the condition does not clear then [OT1C] will be set in **Safety Status** and if [OTFET] is set in *Operation Cfg B* the Charge FET will be opened. If [OTFET] is not set in *Operation Cfg B* then the Charge FET will not be opened by this fault. This fault condition causes [TCA] and [OTA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 55°C which should be sufficient for most LION applications.

OT1 Chg Time

See *OT1 Chg Threshold*. This is a buffer time allotted for TS1 Over Temperature in the charge direction condition. The timer starts every time the temperature breaches *OT1 Chg Threshold* while charging. When the timer expires, the bq20z40/bq20z45 forces an [OT1C] in **Safety Status** and opens the Charge FET, if enabled with [OTFET] in *Operation Cfg B*. If the OT1C condition clears within *OT1 Chg Time* seconds, then no [OT1C] will be set in **Safety Status**. Setting the *OT1 Chg Time* to 0 disables this function.

Normal Setting: This is usually set to 2 seconds which should be sufficient for most applications. Temperature is usually a slow acting condition that does not need high speed triggering. It should be set long enough to prevent false triggering of the [OT1C] in **Safety Status** but short enough to prevent damage to the battery pack.

OT1 Chg Recovery

OT1 Chg Recovery is the temperature at which the battery will recover from an *OT1 Chg Threshold* fault. This is the only recovery method for an *OT1 Chg Threshold* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Charge FET if it was opened with the fault. The default is 50°C which should be sufficient to protect against oscillation during the transition between conditions.

OT2 Chg Threshold

When the temperature measured by TS2 rises up to or above this threshold while charging (**Current** > *Chg Current Threshold*) then the TS2 Over Temperature in charge direction (OT2C) detection process is triggered. If the OT2C condition clears within *OT2 Chg Time* seconds, then no [OT2C] will be set in **Safety Status 2**. If the condition does not clear then [OT2C] will be set in **Safety Status 2** and if [OTFET] is set in *Operation Cfg B* the Charge FET will be opened. If [OTFET] is not set in *Operation Cfg B* then the Charge FET will not be opened by this fault. This fault condition causes [TCA] and [OTA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 55°C which should be sufficient for most LION applications.

OT2 Chg Time

See *OT2 Chg Threshold*. This is a buffer time allotted for TS2 Over Temperature in the charge direction condition. The timer starts every time the temperature breaches *OT2 Chg Threshold* while charging. When the timer expires, the bq20z40/bq20z45 forces an [OT2C] in **Safety Status 2** and opens the Charge FET, if enabled with [OTFET] in *Operation Cfg B*. If the OT2C condition clears within *OT2 Chg Time* seconds, then no [OT2C] will be set in **Safety Status 2**. Setting the *OT2 Chg Time* to 0 disables this function.

Normal Setting: This is usually set to 2 seconds which should be sufficient for most applications. Temperature is usually a slow acting condition that does not need high speed triggering. It should be set long enough to prevent false triggering of the [OT1C] in **Safety Status 2** but short enough to prevent damage to the battery pack.

OT2 Chg Recovery

OT2 Chg Recovery is the temperature at which the battery will recover from an *OT2 Chg Threshold* fault. This is the only recovery method for an *OT2 Chg Threshold* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Charge FET if it was opened with the fault. The default is 50°C which should be sufficient to protect against oscillation during the transition between conditions.

OT1 Dsg Threshold

When the temperature measured by TS1 rises up to or above this threshold while discharging (**Current** < (-)(*Dsg Current Threshold*)) then the TS1 Over Temperature in discharge direction (OT1D) detection process is triggered. If the OT1D condition clears within 2 seconds, then no [OT1D] will be set in **Safety Status**. If the condition does not clear then [OT1D] will be set in **Safety Status** and if [OTFET] is set in *Operation Cfg B* the Discharge FET will be opened. If [OTFET] is not set in *Operation Cfg B* then the Discharge FET will not be opened by this fault. This fault condition causes [TDA] and [OTA] in **Battery Status** to be set. It also causes **Charging Current** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these settings are sufficient for the application temperature. The default is 60°C which should be sufficient for most LION applications. The reason why the default *OT1 Dsg Threshold* setting is higher than the default *OT2 Chg Threshold* is because LION can handle a higher temperature in the discharge direction than in the charge direction.

OT1 Dsg Time

See *OT1 Dsg Threshold*. This is a buffer time allotted for TS1 Over Temperature in the discharge direction condition. The timer starts every time the temperature breaches *OT1 Dsg Threshold* while discharging. When the timer expires then the bq20z40/bq20z45 forces an [OT1D] in **Safety Status** and opens the Discharge FET if enabled with [OTFET] in *Operation Cfg B*. If the OT1D condition clears within *OT1 Dsg Time* seconds, then no [OT1D] will be set in **Safety Status**. Setting the *OT1 Dsg Time* to 0 disables this function.

Normal Setting: This is usually set to 2 seconds which should be sufficient for most applications. Temperature is usually a slow acting condition that does not need high speed triggering. It should be set long enough to prevent false triggering of the [OT1D] in **Safety Status** but short enough to prevent damage to the battery pack.

OT1 Dsg Recovery

OT1 Dsg Recovery is the temperature at which the battery recovers from an *OT1 Dsg Threshold* fault. This is the only recovery method for an *OT1 Dsg Threshold* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Discharge FET if it was opened with the fault. The default is 55°C which is sufficient to protect against this oscillation during the transition between conditions.

OT2 Dsg Threshold

When the temperature measured by TS2 rises up to or above this threshold while discharging (**Current** < (-)(*Dsg Current Threshold*)) then the TS2 Over Temperature in discharge direction (OT2D) detection process is triggered. If the OT2D condition clears within 2 seconds, then no [OT2D] will be set in **Safety Status 2**. If the condition does not clear then [OT2D] will be set in **Safety Status 2** and if [OTFET] is set in *Operation Cfg B* the Discharge FET will be opened. If [OTFET] is not set in *Operation Cfg B* then the Discharge FET will not be opened by this fault. This fault condition causes [TDA] and [OTA] in **Battery Status** to be set. It also causes **Charging Current** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these settings are sufficient for the application temperature. The default is 60°C which should be sufficient for most LION applications. The reason why the default *OT2 Dsg Threshold* setting is higher than the default *OT2 Chg Threshold* is because LION can handle a higher temperature in the discharge direction than in the charge direction.

OT2 Dsg Time

See *OT2 Dsg Threshold*. This is a buffer time allotted for TS2 Over Temperature in the discharge direction condition. The timer starts every time the temperature breaches *OT2 Dsg Threshold* while discharging. When the timer expires then the bq20z40/bq20z45 forces an [OT2D] in **Safety Status 2** and opens the Discharge FET if enabled with [OTFET] in *Operation Cfg B*. If the OT2D condition clears within *OT2 Dsg Time* seconds, then no [OT2D] will be set in **Safety Status 2**. Setting the *OT2 Dsg Time* to 0 disables this function.

Normal Setting: This is usually set to 2 seconds which should be sufficient for most applications. Temperature is usually a slow acting condition that does not need high speed triggering. It should be set long enough to prevent false triggering of the [OT2D] in **Safety Status 2** but short enough to prevent damage to the battery pack.

OT2 Dsg Recovery

OT2 Dsg Recovery is the temperature at which the battery recovers from an *OT2 Dsg Threshold* fault. This is the only recovery method for an *OT2 Dsg Threshold* fault.

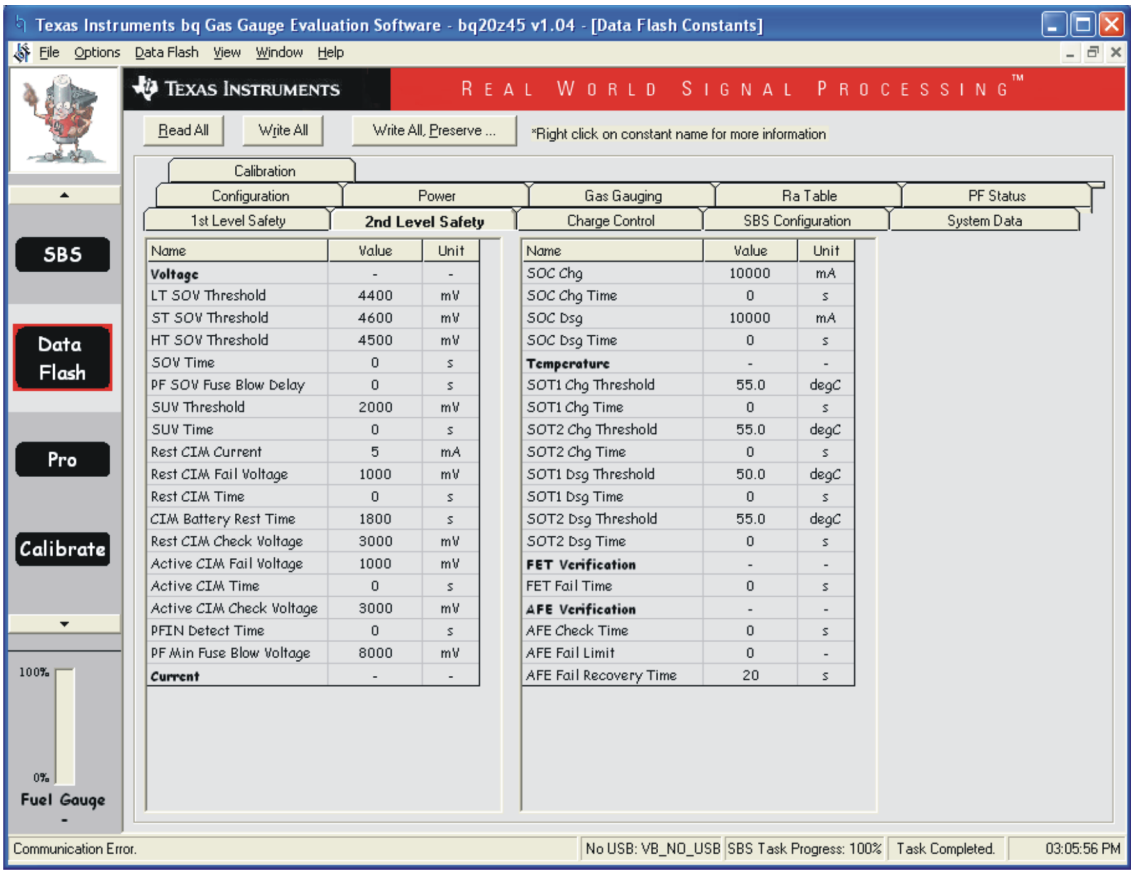
Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Discharge FET if it was opened with the fault. The default is 55°C which is sufficient to protect against this oscillation during the transition between conditions.

Hi Dsg Start Temp

When **Temperature** is above this threshold and there is an attempt at discharging the bq20z40/bq20z45 enters discharge inhibit mode. In this mode, the Discharge FET is opened, [XDSG] and [DSGIN] in **Operation Status** are set, and [TDA] in **Battery Status** is set. The bq20z40/bq20z45 will return to normal mode and allow discharging when **Temperature** becomes equal to or less than *Hi Dsg Start Temp*.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while discharging and verify these settings are sufficient for the application temperature. The default is 60 degrees C which should be sufficient for most LION applications. This threshold should not be set higher than *OT1 Dsg Threshold* or *OT2 Dsg Threshold* in most applications.

3 2nd Level Safety



3.1 Voltage

LT SOV Threshold

This is a final level of protection. It is permanent. When the bq20z40/bq20z45 is operating in the low temperature charging range ([TR2] in **Temperature Range** is set) and the highest cell voltage rises up to this threshold, then the Safety Over Voltage (SOV) detection process is triggered. If the SOV condition clears within *SOV Time*, then no [SOV] will be set in **PF Status**. If the SOV condition does not clear then [SOV] will be set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET, Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled
5. If [XSOV] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a voltage above the *LT COV Threshold*. This is meant to be a permanent condition and it is recommended that [XSOV] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

ST SOV Threshold

This is a final level of protection. It is permanent. When the bq20z40/bq20z45 is operating in the standard temperature charging range (either [TR2a] or [TR3] in **Temperature Range** are set) and the highest cell voltage rises up to this threshold, then the Safety Over Voltage (SOV) detection process is triggered. If the SOV condition clears within *SOV Time*, then no [SOV] will be set in **PF Status**. If the SOV condition does not clear then [SOV] will be set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET, Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled
5. If [XSOV] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a voltage above the *ST COV Threshold*. This is meant to be a permanent condition and it is recommended that [XSOV] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

HT SOV Threshold

This is a final level of protection. It is permanent. When the bq20z40/bq20z45 is operating in the high temperature charging range ([TR4] in **Temperature Range** is set) and the highest cell voltage rises up to this threshold, then the Safety Over Voltage (SOV) detection process is triggered. If the SOV condition clears within *SOV Time*, then no [SOV] will be set in **PF Status**. If the SOV condition does not clear then [SOV] will be set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET, Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled
5. If [XSOV] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a voltage above the *HT COV Threshold*. This is meant to be a permanent condition and it is recommended that [XSOV] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

SOV Time

See *LT SOV Threshold*, *ST SOV Threshold*, or *HT SOV Threshold*. This is a buffer time allotted for an SOV condition. The timer starts when the Safety Over Voltage (SOV) detection process is triggered. When it expires then the bq20z40/bq20z45 forces an [SOV] in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOV Time* timer then the *SOV Time* timer resets without setting [SOV] in **PF Status**. If *SOV Time* is 0 then the SOV Threshold functions are disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. It is highly recommended to enable this function in the final application. The most common values for this register are between 2–5 seconds.

PF SOV Fuse Blow Delay

In case of a safety over voltage permanent failure condition, the assertion of the SAFE output (to blow the fuse) can be delayed to allow the battery to discharge to a safe level before blowing the fuse. A PF timer is started once an SOV PF event occurs. The SAFE output will be driven high (thus blowing the fuse) once this time reaches *PF SOV Fuse Blow Delay*, or as soon as all cell voltages go below the COV recovery threshold for the current temperature range, whichever comes first. If *PF SOV Fuse Blow Delay* is set to 0, the SAFE output will be driven high (to blow the fuse) immediately after the *SOV Time* timer expires, following the detection of a safety over voltage condition.

Normal Setting: This register defaults to 0. This disables the function. If this function is enabled, this timer should be set high enough to allow the battery voltage to drop below a safe level. Since the discharge time is also limited to all cell voltages falling below the relevant COV recovery threshold, there is no risk of over discharging due to setting the timer too high.

SUV Threshold

This is a final level of protection. It is permanent. When the lowest cell voltage falls to this threshold then the Safety Under Voltage (SUV) detection process is triggered. If the SUV condition clears within *SUV Time*, then no [SUV] will be set in **PF Status**. If the SUV condition does not clear then [SUV] will be set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET, Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled
5. If [XSUV] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a voltage below the *CUV Threshold*. This is meant to be a permanent condition and it is recommended that [XSUV] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

SUV Time

See *SUV Threshold*. This is a buffer time allotted for an SUV condition. The timer starts when the Safety Under Voltage (SUV) detection process is triggered. When it expires then the bq20z40/bq20z45 forces an [SUV] in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SUV Time* timer then the SUV Time timer resets without setting [SUV] in **PF Status**. If *SUV Time* is 0 then the *SUV Threshold* functions are disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. It is highly recommended to enable this function in the final application. The most common values for this register are between 2-5 seconds.

Rest CIM Current

This is part of the safety cell imbalance at rest detection algorithm. There are 5 registers that go together to make up this algorithm. *Rest CIM Current* is the value that **Current** must be below for the entire *CIM Battery Rest Time* before cell imbalance at rest detection is enabled. In other words, the bq20z40/bq20z45 will not start trying to detect a cell imbalance at rest until the battery **Current** has been below this *Rest CIM Current* for at least *CIM Battery Rest Time*.

Normal Setting: This register should be set relatively low to ensure the battery is completely relaxed when this algorithm is enabled. This Safety algorithm, if triggered, is permanent and renders the battery useless, so it is imperative that all data is valid prior to activation. The default setting is 5mA which should be sufficient for most applications.

Rest CIM Fail Voltage

This is part of the safety cell imbalance at rest detection algorithm. For the purpose of this description:

Cell Voltage H = the highest SBS cell voltage

Cell Voltage L = the lowest SBS cell voltage

Delta Cell Voltage = ***Cell Voltage H*** – ***Cell Voltage L***

There are 5 registers that go together to make up this algorithm. If any cell voltage is greater than *Rest CIM Check Voltage* and after the *CIM Battery Rest Time* portion of the cell imbalance at rest algorithm has passed the test criteria (see *CIM Battery Rest Time* and *Rest CIM Current*) then, if **Delta Cell Voltage** is greater than the *Rest CIM Fail Voltage* in millivolts the *Rest CIM Fail Voltage* detection process is triggered. If the cell imbalance at rest condition clears prior to the expiration of the *Rest CIM Time* timer, then no [CIM_R] will be set in **PF Status**. If the cell imbalance at rest condition does not clear then [CIM_R] will be set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in **Battery Status** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If [XCIM_R] in *Permanent Fail Cfg* is set then the Safety Output pins will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a voltage high enough to prevent any possibility of false triggering because in application this is irreversible. This is meant to be a permanent condition and it is recommended that [XCIM_R] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

Rest CIM Time

See *Rest CIM Fail Voltage*. This is a buffer time allotted for a cell imbalance at rest safety condition. The timer starts after the *CIM Battery Rest Time* has expired with **Current** below the *Rest CIM Current* and **Delta Cell Voltage** (see *Rest CIM Fail Voltage*) is above the *Rest CIM Fail Voltage*. When the *Rest CIM Time* timer expires then the bq20z40/bq20z45 forces a [CIM_R] in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Rest CIM Time* timer then the *Rest CIM Time* timer resets without setting [CIM_R] in **PF Status**. The *Rest CIM Fail Voltage* function is disabled with *Rest CIM Time* equal to 0 or *CIM Battery Rest Time* set to 0.

Normal Setting: This register defaults to 0. This disables the function. It is recommended that this function be enabled and the [XCIM_R] bit be enabled in *Permanent Fail Cfg* to protect against a potentially dangerous condition. *CIM Battery Rest Time* will help prevent false triggering of this condition so a good setting for *Rest CIM Time* is 5 seconds. This gives several readings to ensure that the condition does exist.

CIM Battery Rest Time

See *Rest CIM Current*. *CIM Battery Rest Time* is the time in seconds that the battery **Current** must be below the *Rest CIM Current* before cell imbalance at rest detection is enabled. In other words, the bq20z40/bq20z45 will not start trying to detect a cell imbalance at rest for this safety algorithm until the battery **Current** has been below *Rest CIM Current* for at least *CIM Battery Rest Time*. The *Rest CIM Fail Voltage* function is disabled with *Rest CIM Time* or *CIM Battery Rest Time* set to 0.

Normal Setting: This register should be set for a relatively long time period to ensure the battery is completely relaxed when this algorithm is enabled. This safety algorithm, if triggered, is permanent and renders the battery useless so it is imperative that all data is valid prior to activation. The default setting is 1800 seconds which should be sufficient for most applications.

Rest CIM Check Voltage

See *Rest CIM Current* and *Rest CIM Fail Voltage*. This is part of the safety cell imbalance at rest detection algorithm. If any of the cell voltages are greater than this threshold, then the safety cell imbalance at rest detection algorithm will be enabled.

Normal Setting: The default value of *Rest CIM Check Voltage* is 3000mV. It is not recommended to set the value any lower. Voltage differences at very low capacities are not necessarily due to cell imbalance and can trigger inadvertent permanent failures, which will blow the fuse and render the pack inoperable.

Active CIM Fail Voltage

This is part of the safety cell imbalance while active detection algorithm. For the purpose of this description:

Cell Voltage H = the highest SBS cell voltage

Cell Voltage L = the lowest SBS cell voltage

Delta Cell Voltage = ***Cell Voltage H*** – ***Cell Voltage L***

There are 3 registers that go together to make up this algorithm. If any cell voltage is greater than *Active CIM Check Voltage* and **Current** is at least *Charge Detection Current* then, if **Delta Cell Voltage** is greater than the *Active CIM Fail Voltage* in millivolts the *Active CIM Fail Voltage* detection process is triggered. If the cell imbalance while active condition clears prior to the expiration of the *Active CIM Time* timer, then no [CIM_A] will be set in **PF Status 2**. If the cell imbalance while active condition does not clear then [CIM_A] will be set in **PF Status 2**. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in **Battery Status** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If [XCIM_A] in *Permanent Fail Cfg 2* is set then the Safety Output pins will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a voltage high enough to prevent any possibility of false triggering because in application this is irreversible. This is meant to be a permanent condition and it is recommended that [XCIM_A] be set in *Permanent Fail Cfg 2* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

Active CIM Time

See *Active CIM Fail Voltage*. This is a buffer time allotted for a cell imbalance while active safety condition. The timer starts after the **Current** has reached *Charge Detection Current* and **Delta Cell Voltage** (see *Active CIM Fail Voltage*) is above the *Active CIM Fail Voltage*. When the *Active CIM Time* timer expires then the bq20z40/bq20z45 forces a [CIM_A] in **PF Status 2** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Active CIM Time* timer then the *Active CIM Time* timer resets without setting [CIM_A] in **PF Status 2**. The *Active CIM Fail Voltage* function is disabled with *Active CIM Time* equal to 0.

Normal Setting: This register defaults to 0. This disables the function. It is recommended that this function be enabled and the [XCIM_A] bit be enabled in *Permanent Fail Cfg 2* to protect against a potentially dangerous condition. A good setting for *Active CIM Time* is 5 seconds. This gives several readings to ensure that the condition does exist.

Active CIM Check Voltage

See *Active CIM Fail Voltage*. This is part of the safety cell imbalance while active detection algorithm. If any of the cell voltages are greater than this threshold, then the safety cell imbalance while active detection algorithm will be enabled.

Normal Setting: The default value of *Active CIM Check Voltage* is 3000mV. It is not recommended to set the value any lower. Voltage differences at very low capacities are not necessarily due to cell imbalance and can trigger inadvertent permanent failures, which will blow the fuse and render the pack inoperable.

PFIN Detect Time

This is a buffer time allotted for an $\overline{\text{PFIN}}$ safety condition. The timer *PFIN Detect Time* timer starts after the $\overline{\text{PFIN}}$ input pin has been set logic low by some external device (normally an external protector). When the *PFIN Detect Time* timer expires then the bq20z40/bq20z45 forces an {PFIN} in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *PFIN Detect Time* timer then the *PFIN Detect Time* timer resets without setting {PFIN} in ***PF Status***. If *PFIN Detect Time* is 0 then this function is disabled. This fault condition triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If [XPFIN] in *Permanent Fail Cfg* is set then the Safety Output pins will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: If this fault condition occurs then it is because an external device has already triggered a fault that should be non recoverable. This is meant to be a permanent condition and it is recommended that [XPFIN] be set in *Permanent Fail Cfg*. Then if a fault happens and and external device sets the /PFIN input low, if for some reason the fuse does not blow then the bq20z40/bq20z45 will also attempt to blow the fuse (SAFE pin is set high). There is a clear function for this condition but it is only intended to be used during the development process. The default for this function is 0. If the /PFIN input is not used then this should be disabled. It is highly recommended that this be used and that [XPFIN] be set to ensure safe operation.

PF Min Fuse Blow Voltage

In case of a safety permanent failure condition other than Charge FET or Discharge FET faults ([CFETF] or [DFETF]), the assertion of the SAFE output is conditional on pack voltage being greater than *PF Min Fuse Blow Voltage*. The purpose of the feature is to ensure that there is sufficient battery power for a reliable fuse blow.

Normal Setting: This register defaults to 8000mV and can be effectively disabled by setting the value to 0mV.

3.2 Current

SOC Chg

SOC Chg is a final level of current protection from the bq20z40/bq20z45. This is not related to the 2nd level (AFE) protection which is a fast acting protection. It is also intended to be permanent. When the charge current as measured by ***Current*** rises to or above this threshold, then the Safety Over Current in the Charge direction (SOCC) protection process is triggered. This process starts by setting [SOCC] in ***PF Alert*** for *SOC Chg Time*. If the SOCC condition clears prior to the expiration of the *SOC Chg Time* timer, then the [SOCC] is cleared in ***PF Alert*** and with no [SOCC] being set in ***PF Status***. If the SOC condition does not clear, then [SOCC] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If [XSOCC] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a current above *OC(1stTier) Chg*. It is not necessarily required to set above *AFE OC Chg* which is a fast acting fault condition meant for high current spike detection. This function is meant to be a permanent condition, and it is recommended that [XSOCC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Chg Time

See *SOC Chg*. This is a buffer time allotted for an SOCC condition. The timer starts after [SOCC] is set in ***PF Alert***. When it expires, then the bq20z40/bq20z45 forces an [SOCC] in ***PF Status***, and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Chg Time* timer, then the *SOC Chg Time* timer resets without setting [SOCC] in ***PF Status***. If *SOC Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

SOC Dsg

SOC Dsg is a final level of current protection from the bq20z40/bq20z45. This is not related to the 2nd level (AFE) protection because that is a fast acting protection. This is very slow relatively speaking. It is also intended to be permanent. When the discharge current as measured by ***Current*** falls **down** to or **below** a negative of this threshold (– (*SOC Dsg*)) then the Safety Over Current in the discharge direction (SOCD) detection process is triggered. If the SOCC condition clears prior to the expiration of the *SOC Dsg Time* timer, then no [SOCC] is set in ***PF Status***. If the SOC condition does not clear then [SOCD] is set in PF Status. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed..
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If [XSOCD] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: Care must taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This is the last level of protection and must be set to a current below *OC(1stTier) Dsg*. It is not required to set above *AFE OC Dsg* which is a fast acting fault condition meant for high current spike detection. This is meant to be a permanent condition and it is recommended that [XSOCD] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Dsg Time

See *SOC Dsg*. This is a buffer time allotted for an SOCD condition. The timer starts after the Safety Over Current in the discharge direction (SOCD) detection process is triggered. When it expires then the bq20z40/bq20z45 forces an [SOCD] in ***PF Status*** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Dsg Time* timer then the *SOC Dsg Time* timer resets without setting [SOCD] in ***PF Status***. If *SOC Dsg Time* is 0 then this function is disabled

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

3.3 Temperature

SOT1 Chg Threshold

SOT1 Chg Threshold is a final level of temperature protection from the bq20z40/bq20z45. This fault condition is intended to be permanent. When the temperature as measured by **TS1 Temperature** rises up to or above this threshold while charging ([DSG] cleared in **Battery Status**) then the TS1 Safety Over Temperature in the Charge direction (SOT1C) detection process is triggered. If the SOT1C condition clears prior to the expiration of the *SOT1 Chg Time* timer, then [SOT1C] will not be set in **PF Status**. If the SOT1C condition does not clear then [SOT1C] will be set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.

4. Data Flash Writes will be disabled.
5. If [XSOT1C] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a temperature above *OT1 Chg Threshold*. This is meant to be a permanent condition and it is recommended that [XSOT1C] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

SOT1 Chg Time

See *SOT1 Chg Threshold*. This is a buffer time allotted for a TS1 Safety Over Temperature Condition. The timer starts after the TS1 Safety Over Temperature in the Charge direction (SOT1C) detection process is triggered. When it expires then the bq20z40/bq20z45 forces an [SOT1C] in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were closed. If the condition clears prior to the expiration of the *SOT1 Chg Time* timer then the *SOT1 Chg Time* timer resets without setting [SOT1C] in **PF Status**. If *SOT1 Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. It is highly recommended to enable this function in the final application. The most common values for this register are between 2-5 seconds.

SOT2 Chg Threshold

SOT2 Chg Threshold is a final level of temperature protection from the bq20z40/bq20z45. This fault condition is intended to be permanent. When the temperature as measured by **TS2 Temperature** rises up to or above this threshold while charging ([DSG] cleared in **Battery Status**) then the TS2 Safety Over Temperature in the Charge direction (SOT2C) detection process is triggered. If the SOT2C condition clears prior to the expiration of the *SOT2 Chg Time* timer, then [SOT2C] will not be set in **PF Status 2**. If the SOT2C condition does not clear then [SOT2C] will be set in **PF Status 2**. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If [XSOT2C] in *Permanent Fail Cfg 2* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a temperature above *OT2 Chg Threshold*. This is meant to be a permanent condition and it is recommended that [XSOT2C] be set in *Permanent Fail Cfg 2* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

SOT2 Chg Time

See *SOT2 Chg Threshold*. This is a buffer time allotted for a TS2 Safety Over Temperature Condition. The timer starts after the TS2 Safety Over Temperature in the Charge direction (SOT2C) detection process is triggered. When it expires then the bq20z40/bq20z45 forces an [SOT2C] in **PF Status 2** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were closed. If the condition clears prior to the expiration of the *SOT2 Chg Time* timer then the *SOT2 Chg Time* timer resets without setting [SOT2C] in **PF Status 2**. If *SOT2 Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. It is highly recommended to enable this function in the final application. The most common values for this register are between 2-5 seconds.

SOT1 Dsg Threshold

SOT1 Dsg Threshold is a final level of temperature protection from the bq20z40/bq20z45. This fault condition is intended to be permanent. When the temperature as measured by **TS1 Temperature** rises up to or above this threshold while discharging ([DSG] set in **Battery Status**) then the TS1 Safety Over Temperature in the discharge direction (SOT1D) detection process is triggered. If the SOT1D condition clears prior to the expiration of the *SOT1 Dsg Time* timer, then no [SOT1D] will be set in **PF Status**. If the SOT1D condition does not clear then [SOT1D] will be set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If [XSOT1D] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a temperature above *OT1 Dsg Threshold*. This is meant to be a permanent condition and it is recommended that [XSOT1D] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

SOT1 Dsg Time

See *SOT1 Dsg Threshold*. This is a buffer time allotted for a TS1 Safety Over Temperature Condition. The timer starts after the TS1 Safety Over Temperature in the discharge direction (SOT1D) detection process is triggered. When it expires then the bq20z40/bq20z45 forces an [SOT1D] in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOT1 Dsg Time* timer then the *SOT1 Dsg Time* timer resets without setting [SOT1D] in **PF Status**. If *SOT1 Dsg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. It is highly recommended to enable this function in the final application. The most common values for this register are between 2-5 seconds.

SOT2 Dsg Threshold

SOT2 Dsg Threshold is a final level of temperature protection from the bq20z40/bq20z45. This fault condition is intended to be permanent. When the temperature as measured by **TS2 Temperature** rises up to or above this threshold while discharging ([DSG] set in **Battery Status**) then the TS2 Safety Over Temperature in the discharge direction (SOT2D) detection process is triggered. If the SOT2D condition clears prior to the expiration of the *SOT2 Dsg Time* timer, then no [SOT2D] will be set in **PF Status 2**. If the SOT2D condition does not clear then [SOT2D] will be set in **PF Status 2**. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If [XSOT2D] in *Permanent Fail Cfg* 2 is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

Normal Setting: This is the last level of protection and should be set to a temperature above *OT2 Dsg Threshold*. This is meant to be a permanent condition and it is recommended that [XSOT2D] be set in *Permanent Fail Cfg 2* with a fuse designed into the application. There is a clear function for this condition but it is only intended to be used during the development process.

SOT2 Dsg Time

See *SOT2 Dsg Threshold*. This is a buffer time allotted for a TS2 Safety Over Temperature Condition. The timer starts after the TS2 Safety Over Temperature in the discharge direction (SOT2D) detection process is triggered. When it expires then the bq20z40/bq20z45 forces an [SOT2D] in **PF Status 2** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOT2 Dsg Time* timer then the *SOT2 Dsg Time* timer resets without setting [SOT2D] in **PF Status 2**. If *SOT2 Dsg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. It is highly recommended to enable this function in the final application. The most common values for this register are between 2-5 seconds.

3.4 FET Verification

FET Fail Limit

The *FET Fail Time* register is a buffer time allotted for a FET circuit fault protection algorithm in the bq20z40/bq20z45 that detects potentially hazardous FET circuit damage. In the bq20z40/bq20z45 this is set to ±50 milliAmps and is not adjustable. This fault condition is intended to be permanent and has 2 possible trigger functions that are listed separately here to help prevent confusion.

(A) If the Charge and Pre-Charge FET (if enabled) have been commanded to be off for any reason by either the gauge or the AFE (any AFE fault condition) and charge current as measured by ***Current*** still exists which is more than 50 milliAmps, then the FET Fault detection process is triggered. If the [CFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then the no [CFETF] is set in ***PF Status***. If the [CFETF] condition does not clear, then [CFETF] is set in ***PF Status***. This triggers many permanent protection features as listed below::

(B) If the discharge FET has been commanded to be off for any reason by either the gauge or the AFE (any AFE fault condition) and discharge current as measured by ***Current*** still exists which is less than or equal to –50 milliAmps then the *FET Fail Limit* protection process is triggered. If the [DFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then no [DFETF] is set in ***PF Status***. If the [DFETF] condition does not clear then [DFETF] is set in ***PF Status***. This triggers many permanent protection features as listed below:

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If A) and [XCFETF] or B) and [XDFETF] in *Permanent Fail Cfg* is set then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

If *FET Fail Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application, is recommended. The most common values for this register are between 2–5 seconds. The Charge and Discharge FETs arguably have more stress than any other component on the gas gauge PCB. This function is an excellent safety feature to help protect against the possibility of a shorted FET that could be potentially hazardous. This is meant to be a permanent condition and it is recommended that [XCFETF] and [XDFETF] both be set in *Permanent Fail Cfg* with a fuse designed into the application.

3.5 AFE Verification

AFE Check Time

Every *AFE Check Time* in seconds the gauge will read all the AFE registers through the I2C port that is shared between the 2 parts and compare the static register read results to the AFE data in the gauge's Data Flash. If they do not match then the gauge will attempt to repair the corruption and then increment an internal counter (for the sake of this document this will be referred to as AFE_P Fail Counter) which triggers the periodic AFE_P Fail protection process. See *AFE Fail Recovery Time* for a recovery description. If *AFE Check Time* is set to 0 then the periodic AFE verification (AFE_P) is completely disabled.

Normal Setting: Setting *AFE Check Time* to 0 only disables the AFE_P verification function. It does not disable the AFE_C verification function as described in *AFE Fail Limit*. *AFE Check Time* set to 0 is acceptable because there is still the AFE_C verification process. If, however, *AFE Check Time* is used, set above 20 seconds since the periodic test does not need to be done very often to ensure correct function.

AFE Fail Limit

Anytime a communication with the bq29330 is performed over the I^2C bus then an internal counter (for the sake of this document this is referred to as AFE_C Fail Counter) will increment. When the AFE_C Fail Counter increments, the AFE_C Fail detection process is triggered. As long as the AFE_C Fail Counter stays below the *AFE Fail Limit* and above 0, then this detection process is active. During this process, every 20 seconds AFE_C Fail Counter is decremented by 1 until it reaches 0 which will turn off the detection process. If the AFE_C Fail Counter reaches the *AFE Fail Limit*, then [AFE_C] is set in ***PF Status***. Setting *AFE Fail Limit* to 0 disables the AFE_C Fail protection process.

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET , Discharge FET, and Pre-Charge FET will all be opened if they were closed.
2. [TCA] and [TDA] in ***Battery Status*** will be set.
3. ***Charging Current*** and ***Charging Voltage*** will be set to 0.
4. Data Flash Writes will be disabled.
5. If A. and [XAFE_P] or B) and [XAFE_C] in *Permanent Fail Cfg* is set, then the Safety Output pin will be activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class will be filled with all past and current permanent failure causes.

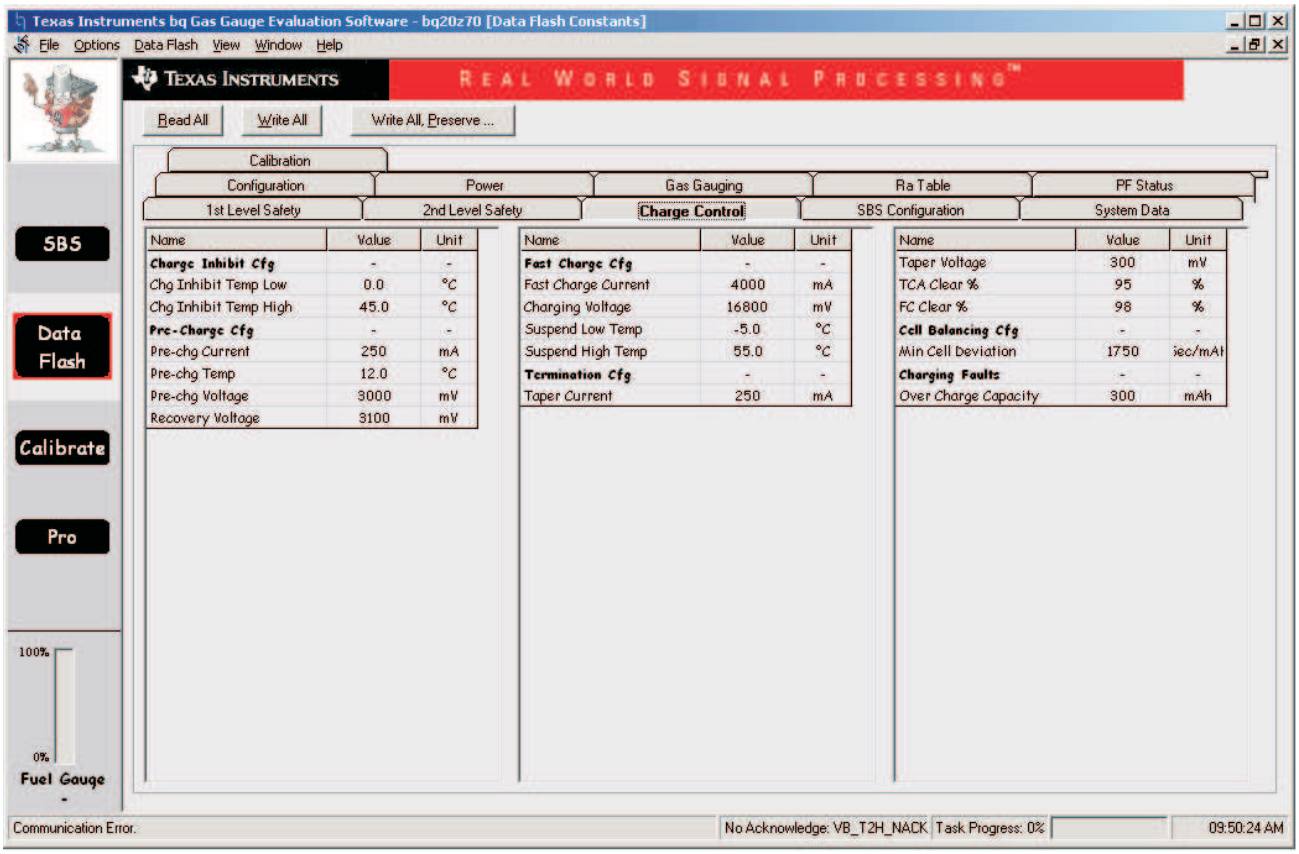
Normal Setting: *AFE Fail Limit* defaults to 10. It is very important to note that setting *AFE Fail Limit* to 0 only disables the AFE_C functions. The default of 10 should be appropriate for most applications. This gives sufficient buffer for ESD, resets and other unknown failures that should be recoverable.

AFE Fail Recovery Time

See *AFE Check Time* and *AFE Fail Limit*. *AFE Fail Recovery Time* function works independently with each of the AFE counters described above (AFE_C Fail Counter and AFE_P Fail Counter). While the AFE protection process is active, every *AFE Fail Recovery Time* period in seconds AFE_C Fail Counter and/or AFE_P Fail Counter will be decremented by 1 until each reaches 0. As soon as they are decremented back to 0 the AFE protection process is reversed.

Normal Setting: It is recommended to set this register less than *AFE Check Time* so that at least one recovery process can occur between periodic checks.

4 Charge Control



4.1 Charge Inhibit Config

JT1

JT1 is the lower bound of the low temperature charging range. If **Temperature** is below the *JT1* threshold, then the [TR1] flag in **Temperature Range** is set and charging is inhibited from starting. If the bq20z40/bq20z45 is in charge mode ([DSG] set in **Battery Status**), then charging is suspended, the [CHGSUSP] flag in **Charging Status** is set, and **Charging Current** and **Charging Voltage** are set to 0.

Normal Setting: The purpose of this low inhibit temperature is to suspend or inhibit charging prevent damage to the pack when the temperature is too low. The default for this is 0°C and can be modified to fit the application. This threshold is also the lower bound of the low temperature charging range for the JEITA specification.

JT2

JT2 is the upper bound of the low temperature charging range and the lower bound of the standard temperature charging range 1. If **Temperature** is between *JT1* and *JT2*, then the [TR2] flag in **Temperature Range** is set, **Charging Voltage** is set to *LT Chg Voltage*, and **Charging Current** is set to *LT Chg Current 1*, *LT Chg Current 2*, or *LT Chg Current 3*, depending on the maximum cell voltage.

Normal Setting: The default for this is 12°C and can be modified to fit the application. This threshold is also the upper bound of the low temperature charging range and the lower bound of the normal temperature charging range for the JEITA specification.

JT2a

JT2a is the upper bound of the standard temperature charging range 1 and the lower bound of the standard temperature charging range 2. If **Temperature** is between *JT2* and *JT2a*, then the [TR2A] flag in **Temperature Range** is set, **Charging Voltage** is set to *ST1 Chg Voltage*, and **Charging Current** is set to *ST1 Chg Current 1*, *ST1 Chg Current 2*, or *ST1 Chg Current 3*, depending on the maximum cell voltage.

Normal Setting: The default for this is 30°C and can be modified to fit the application. This threshold marks the upper bound of the standard temperature charging range 1 and the lower bound of the standard charging range 2. This is not a JEITA defined threshold, but it adds additional charge control flexibility.

JT3

JT3 is the upper bound of the standard temperature charging range 2 and the lower bound of the high temperature charging range. If **Temperature** is between *JT2a* and *JT3*, then the [TR3] flag in **Temperature Range** is set, **Charging Voltage** is set to *ST2 Chg Voltage*, and **Charging Current** is set to *ST2 Chg Current 1*, *ST2 Chg Current 2*, or *ST2 Chg Current 3*, depending on the maximum cell voltage.

Normal Setting: The default for this is 45°C and can be modified to fit the application. This threshold is also the upper bound of the standard temperature charging range and the lower bound of the high temperature charging range for the JEITA specification.

JT4

JT4 is the upper bound of the high temperature charging range. If **Temperature** is between *JT3* and *JT4*, then the [TR4] flag in **Temperature Range** is set, **Charging Voltage** is set to *HT Chg Voltage*, and **Charging Current** is set to *HT Chg Current 1*, *HT Chg Current 2*, or *HT Chg Current 3*, depending on the maximum cell voltage. If temperature is greater than *JT4*, then the [TR5] flag in **Temperature Range** is set. If the bq20z40/bq20z45 is in charge mode ([DSG] set in **Battery Status**), then charging is suspended, the [CHGSUSP] flag in **Charging Status** is set, and **Charging Current** and **Charging Voltage** are set to 0.

Normal Setting: The default for this is 55°C and can be modified to fit the application. This threshold is also the upper bound of the high temperature charging range for the JEITA specification.

Temp Hys

Temp Hys is used to make sure that transitions between temperature ranges are not affected by small transients on the temperature reading. For example, if the current temperature range is the standard temperature range 2 ([TR3] in **Temperature Range** is set) and **Temperature** goes above *JT3*, then the high temperature range is entered ([TR3] is cleared and [TR4] is set). **Temperature** has to fall below *JT3* - *Temp Hys* for the bq20z40/bq20z45 to go back to the standard temperature range 2.

Normal Setting: The default setting for this threshold is 1 degree Celsius. This setting depends on the application.

4.2 Pre-Charge Config

Pre-chg Voltage Threshold

The bq20z40/bq20z45 enters Pre-Charge mode and sets the [PCHG] flag in **Charging Status** if Cell Voltage (Any) drops below the *Pre-chg Voltage Threshold*. In this mode, **Charging Voltage** is set to *LT Chg Voltage* and **Charging Current** is set to *LT Chg Current 1*.

Normal Setting: Ensure that this voltage is set per the battey cell specifications. Setting this value too high hurts nothing (except slower charging from empty) but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage to bring them up to normal charging voltage slowly before hitting them with a fast current. It is always recommended to use a Pre-Charge FET or smart charger that supports low Pre-Charge currents.

Pre-chg Recovery Voltage

If the battery pack is in Pre-Charge mode due to Cell Voltage (Any) falling to or below *Pre-chg Voltage Threshold* then it will exit Pre-Charge mode when Cell Voltage (All) rises above *Pre-Chg Recovery Voltage*. This will clear the [PCHG] flag in **Charging Status**.

Normal Setting: This is battery cell dependent. Ensure that this is set per the battery cell specifications. Setting this value too high hurts nothing (except slower charging from empty) but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage to bring them up to normal charging voltage slowly before hitting them with a fast current. It is always recommended to use a Pre-Charge FET or smart charger that supports low Pre-Charge currents.

Pre-Charge Current

This is the current that the bq20z40/bq20z45 will report in the **Charging Current** register when the bq20z40/bq20z45 is in Pre-Charge mode (see *Pre-chg Voltage Threshold*). This current is also broadcast to a smart charger when bq20z40/bq20z45 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Pre-Charge Mode (**Charging Current** = *Pre-chg Current*), [PCHG] will be set in **Charging Status** and then the appropriate charging FET is enabled as set with [ZVCHG1] and [ZVCHG0] in *Operation Cfg A*.

Table 9. FET Control Bits in *Operation Cfg A*

ZVCHG1	ZVCHG0	FET Used
0	0	ZVCHG
0	1	CHG
1	0	OD
1	1	No Action

There are three primary recoveries from Pre-Charge mode:

1. Cell Voltage (All) must be above *Pre-chg Recovery Voltage*.

   Either of these conditions cause the bq20z40/bq20z45 to enter Fast Charge Mode:

2. Pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated.
3. This is considered a recovery, but it is really a transition from one mode to another. A charge suspend condition (see *JT5* and *JT1*) which forces the bq20z40/bq20z45 to transition from Pre-Charge Mode to Charge Suspend Mode.

Normal Setting: This register is application dependent. If a Pre-Charge FET and a current limiting resistor is used to control the current allowed into the battery during Pre-Charge Mode ([ZVCHG1] and [ZVCHG1] both equal 0) then this register accuracy is not as important as if it were used for a smart charger that will initiate a current equal to the requested Pre-Charge current. It is important to note that use of the OD pin is not recommended because it does not have limiting circuitry to ensure “hard” on control for a Zero Volt charging condition. It is always recommended to use a Pre-Charge FET or smart charger that supports low Pre-Charge currents.

4.3 Fast Charge Config

LT Chg Voltage

The bq20z40/bq20z45 sets **Charging Voltage** to the *LT Chg Voltage* value when **Temperature** is in the low temperature charging range ([TR2] in **Temperature Range** is set).

Normal Setting: Charger tolerances and battery specifications should be considered when setting this register.

LT Chg Current 1

The bq20z40/bq20z45 sets **Charging Current** to the *LT Chg Current 1* value when **Temperature** is in the low temperature charging range ([TR2] in **Temperature Range** is set) and Cell Voltage (Max) is below *Cell Voltage Threshold 1* (see *Cell Voltage Threshold 1*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

LT Chg Current 2

The bq20z40/bq20z45 sets **Charging Current** to the *LT Chg Current 2* value when **Temperature** is in the low temperature charging range ([TR2] in **Temperature Range** is set) and Cell Voltage (Max) is between *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2* (see *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

LT Chg Current 3

The bq20z40/bq20z45 sets **Charging Current** to the *LT Chg Current 3* value when **Temperature** is in the low temperature charging range ([TR2] in **Temperature Range** is set) and Cell Voltage (Max) is above *Cell Voltage Threshold 2* (see *Cell Voltage Threshold 2*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

ST1 Chg Voltage

The bq20z40/bq20z45 sets **Charging Voltage** to the *ST1 Chg Voltage* value when **Temperature** is in the standard temperature charging range 1 ([TR2A] in **Temperature Range** is set).

Normal Setting: Charger tolerances and battery specifications should be considered when setting this register.

ST1 Chg Current 1

The bq20z40/bq20z45 sets **Charging Current** to the *ST1 Chg Current 1* value when **Temperature** is in the standard temperature charging range 1 ([TR2A] in **Temperature Range** is set) and Cell Voltage (Max) is below *Cell Voltage Threshold 1* (see *Cell Voltage Threshold 1*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

ST1 Chg Current 2

The bq20z40/bq20z45 sets **Charging Current** to the *ST1 Chg Current 2* value when **Temperature** is in the standard temperature charging range 1 ([TR2A] in **Temperature Range** is set) and Cell Voltage (Max) is between *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2* (see *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

ST1 Chg Current 3

The bq20z40/bq20z45 sets **Charging Current** to the *ST1 Chg Current 3* value when **Temperature** is in the standard temperature charging range 1 ([TR2A] in **Temperature Range** is set) and Cell Voltage (Max) is above *Cell Voltage Threshold 2* (see *Cell Voltage Threshold 2*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

ST2 Chg Voltage

The bq20z40/bq20z45 sets **Charging Voltage** to the *ST2 Chg Voltage* value when **Temperature** is in the standard temperature charging range 2 ([TR3] in **Temperature Range** is set).

Normal Setting: Charger tolerances and battery specifications should be considered when setting this register.

ST2 Chg Current 1

The bq20z40/bq20z45 sets **Charging Current** to the *ST2 Chg Current 1* value when **Temperature** is in the standard temperature charging range 2 ([TR3] in **Temperature Range** is set) and Cell Voltage (Max) is below *Cell Voltage Threshold 1* (see *Cell Voltage Threshold 1*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

ST2 Chg Current 2

The bq20z40/bq20z45 sets **Charging Current** to the *ST2 Chg Current 2* value when **Temperature** is in the standard temperature charging range 2 ([TR3] in **Temperature Range** is set) and Cell Voltage (Max) is between *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2* (see *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

ST2 Chg Current 3

The bq20z40/bq20z45 sets **Charging Current** to the *ST2 Chg Current 3* value when **Temperature** is in the standard temperature charging range 2 ([TR3] in **Temperature Range** is set) and Cell Voltage (Max) is above *Cell Voltage Threshold 2* (see *Cell Voltage Threshold 2*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

HT Chg Voltage

The bq20z40/bq20z45 sets **Charging Voltage** to the *HT Chg Voltage* value when **Temperature** is in the high temperature charging range ([TR4] in **Temperature Range** is set).

Normal Setting: Charger tolerances and battery specifications should be considered when setting this register.

HT Chg Current 1

The bq20z40/bq20z45 sets **Charging Current** to the *HT Chg Current 1* value when **Temperature** is in the high temperature charging range ([TR4] in **Temperature Range** is set) and Cell Voltage (Max) is below *Cell Voltage Threshold 1* (see *Cell Voltage Threshold 1*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

HT Chg Current 2

The bq20z40/bq20z45 sets **Charging Current** to the *HT Chg Current 2* value when **Temperature** is in the high temperature charging range ([TR4] in **Temperature Range** is set) and Cell Voltage (Max) is between *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2* (see *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

HT Chg Current 3

The bq20z40/bq20z45 sets **Charging Current** to the *HT Chg Current 3* value when **Temperature** is in the high temperature charging range ([TR4] in **Temperature Range** is set) and Cell Voltage (Max) is above *Cell Voltage Threshold 2* (see *Cell Voltage Threshold 2*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

Cell Voltage Threshold 1

The bq20z40/bq20z45 is in cell voltage range 1 (CVR1) when Cell Voltage (Max) is lower than *Cell Voltage Threshold 1*. This threshold affects **Charging Voltage** and **Charging Current** settings in the different temperature modes (see also *Cell Voltage Threshold 2* and *Cell Voltage Thresh Hys*).

Normal Setting: Charger tolerances and battery specifications should be considered when setting this register.

Cell Voltage Threshold 2

The bq20z40/bq20z45 is in cell voltage range 2 (CVR2) when Cell Voltage (Max) is between *Cell Voltage Threshold 1* and *Cell Voltage Threshold 2*. The bq20z40/bq20z45 enters cell voltage range 3 (CVR3) when Cell Voltage (Max) is greater than *Cell Voltage Threshold 2*. This threshold affects **Charging Voltage** and **Charging Current** settings in the different temperature modes (see also *Cell Voltage Threshold 1* and *Cell Voltage Thresh Hys*).

Normal Setting: Charger tolerances and battery specifications should be considered when setting this register.

Cell Voltage Thresh Hys

Cell Voltage Thresh Hys is used to make sure that transitions between cell voltage ranges are not affected by small transients on the temperature reading. For example, if the current cell voltage range is CVR2 and Cell Voltage (Max) rises above *Cell Voltage Threshold 2*, then CVR3 is entered. Cell Voltage (All) has to fall below *Cell Voltage Threshold 2 - Cell Voltage Thresh Hys* for the bq20z40/bq20z45 to go back to the CVR2 range.

Normal Setting: The default setting for this threshold is 10 mV. This setting depends on the application.

4.4 Termination Config

Taper Current

Taper Current is used in the Primary Charge Termination algorithm. ***Current*** is integrated over each of the two consecutive periods of 40 seconds each separately and then they are averaged separately to give 2 averages. Both of these averages must be below the *Taper Current* to qualify for a Primary Charge Termination. In total, a primary charge termination has the following requirements:

1. ***Voltage*** must be above (*Charging Voltage – Taper Voltage*) for the bq20z40/bq20z45 to start trying to qualify a termination. It must be above this voltage before bq20z40/bq20z45 starts trying to detect a primary charge termination.
2. An average of all ***Current*** measurements must be below *Taper Current* for two consecutive periods of 40 seconds from beginning to end of each window.
3. An average of all ***Current*** measurements during each of two consecutive periods of 40 seconds from beginning to end of each window must be above 0.25mAh as integrated and averaged over the two consecutive 40 second windows.

When these conditions are met, the primary charge termination has occurred and the following happens:

1. [TCA] is set in ***Battery Status*** and either of the following happens:
   (a) if [CHGFET] set in *Operation Cfg B* then and ***Charging Current*** is set to 0, and the Charge FET is opened.
   (b) if [CHGFET] is cleared in *Operation Cfg B* then and ***Charging Current*** is set to 0.
2. [FC] is set in ***Battery Status***
3. If [CSYNC] is set in *Operation Cfg B*, then ***Remaining Capacity*** is written to ***Full Charge Capacity***.

The primary charge termination mode has two clearing methods:

1. It is cleared when ***RSOC*** falls below *FC Clear %*
2. if [CHGTERM] in *Operation Cfg B* set, and ***Current*** is less than *Chg Current Threshold* for two consecutive periods of 40 seconds.

Normal Settings: This register is dependent on battery cell characteristics and charger specifications. ***Average Current*** is not used for this qualification because its time constant is not long enough which is why we use 2 consecutive 40 second windows. The reason for making 2 Current Taper qualifications is to prevent false current taper qualifications. False primary terminations can happen with pulse charging and with random starting and stopping of the charge current. This is particularly critical at the beginning or end of the qualification period. .

Taper Voltage

During Primary Charge Termination detection, one of the 3 requirements is that ***Voltage*** must be above (*Charging Voltage – Taper Voltage*) for the bq20z40/bq20z45 to start trying to qualify a termination. It must be above this voltage before bq20z40/bq20z45 starts trying to detect a primary charge termination.

Normal Setting: This value is dependent on charger characteristics. It needs to be set so that ripple voltage, noise, and charger tolerances are taken into account. A value selected too low can cause early termination. If the value selected is too high, then it can cause no or late termination detection. A good example value is 200mV (see *Taper Current*).

TCA Clear %

If during discharge ([DSG] set in ***Battery Status***), ***RSOC*** falls below this value, then [TCA] is cleared.

Normal Setting: Application dependant.

FC Clear %

If during discharge ([DSG] set in ***Battery Status***), ***RSOC*** falls below this value, then [FC] is cleared.

Normal Setting: Application dependant.

4.5 Cell Balancing Config

Min Cell Deviation

The cell balancing algorithm with be active only during charging ([DSG] cleared in ***Battery Status***). The function is disabled completely if *Min Cell Deviation* is set to 0. With impedance track, the bq20z40/bq20z45 knows the Full Charge Capacity for each cell independently. Each cell input in the bq29330 has an internal FET that shorts the cell filtering resistors, and an internal 500-Ω resistor across the cells that need reduced charging to help balance the cells. The bq20z40/bq20z45 use impedance track information along with the value for *Min Cell Deviation* to know how long to turn on the shorting FET. The algorithm works based on the formula:

Min Cell Deviation = dQ × R / (V × duty cycle)

Where:

dQ = correction factor = 3600 seconds/hour

V = nominal cell voltage = 3600 mV

duty cycle = 40% = 0.4

R = Total resistance from cell top to cell bottom (2 filter resistors and internal 500-Ω resistor), so for the bq20z40/bq20z45 EVM, the filter resistors are 100 Ω; therefore, R = 100 × 2 + 500 = 700 Ω

So for 700 Ω in resistance *Min Cell Deviation* = 1750 sec/mAh

Normal Setting: The bq20z40/bq20z45 default value for this register is 1750s/mAH. The only values that is needed to be changed in the formula are R (Resistance), and V (nominal cell voltage). (See SLUA340 for more information)

4.6 Charging Faults

Over Charge Capacity

Over Charge Capacity is detected in a two-step process. First the battery must be charged to the point where Remaining Capacity reaches ***FCC*** (***Full Charge Capacity***). Then any charge applied after this point is still measured but not displayed by the bq20z40/bq20z45. When this charge as measured by the bq20z40/bq20z45 reaches a threshold as defined by ***FCC*** + *Over Charge Capacity*, then the bq20z40/bq20z45 goes into a charging fault condition. The [OC] in ***Charging Status*** is set. ***Charging Voltage*** and ***Charging Current*** are both set to 0. If [OC] set in *Charge Fault Cfg*, then the Charge FET is turned off.

There are three recovery methods for the bq20z40/bq20z45.

1. The first only happens if [NR] in *Operation Cfg B* is set. With this setting the bq20z40/bq20z45 will recover from an overcharged condition with a continuous discharge of 2 mAHs.
2. With [NR] cleared in *Operation Cfg B*, the bq20z40/bq20z45 recovers from the overcharge fault with a pack removal and reinsertion ($\overline{\text{PRES}}$ transition).
3. The third recovery happens when ***RSOC*** falls below the *FC Clear %*. This recovery also is the only one that returns ***Charging Voltage*** and ***Charging Current*** to normal.

Normal Setting: This register is application dependent but a good example is 100 to 300 mAh for each cell in parallel. To small of a value could force false detections, and to large a value could damage the cells if normal charge termination methods fail.

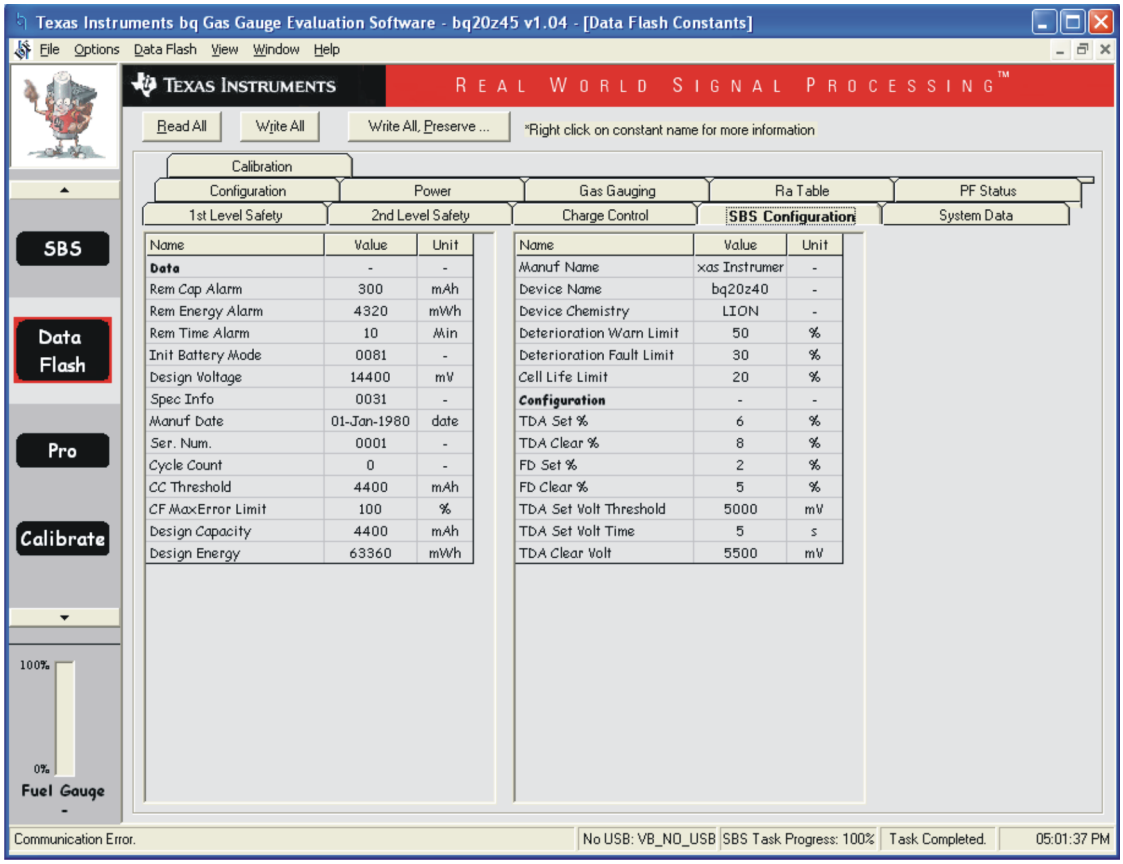
Charge Fault Cfg

This register sets the behavior of the Charge, Discharge, and Pre-Charge FETs in fault conditions.

—	—	—	—	—	—	—	—
—	—	—	—	—	—	OC	—

- OC [1]: If this bit is set, the Charge FET and Pre-Charge FET (if used) are turned off when an overcharge fault occurs (see *Over Charge Capacity*). If cleared, an overcharge fault does not cause any FET action.

5 SBS Configuration



5.1 SBS Data

Rem Cap Alarm

When the ***Remaining Capacity*** falls below this value, [RTA] is set in ***Battery Status***.

Normal Setting: About 10% of the *Full Charge Capacity*. This value is programmed into ***RemainingCapacityAlarm*** on device initialization

Rem Energy Alarm

When the bq20z40/bq20z45 is in milliwatt mode ([CapM] set in ***Battery Mode***), the value in *Rem Energy Alarm* is written to the ***Rem Cap Alarm***. Once this value is written to ***Rem Cap Alarm***, then the function acts the same as *Rem Cap Alarm* except units are in milliwatts. (See *Rem Cap Alarm*)

Normal Setting: About 10% of the *Full Charge Capacity* but units have to be converted to milliwatts. This data flash value is only used when in milliwatt mode. This value is programmed into *RemainingCapacityAlarm* on device initialization if in milliwatt mode.

Rem Time Alarm

When the average time to empty falls below this value, then the [RTA] flag is set in ***Battery Status***.

Normal Setting: Approximately 10 minutes. This value is programmed into ***RemainingTimeAlarm*** on device initialization.

Init Battery Mode

This is the default value loaded into ***Battery Mode*** on all resets, and when the bq20z40/bq20z45 wakes from sleep. The primary purpose of having an initial value for this register is to enable milliwatt mode whenever the bq20z40/bq20z45 resets or wakes up from sleep.

Normal Setting: In most applications, this register should be 0x0081. If the application requires the bq20z40/bq20z45 to wake in mW mode, then this value can be set to 0x8081. Care should be taken with this setting; however, because the ***Battery Mode*** register is writable even when the bq20z40/bq20z45 is sealed. The mW mode bit can be accidentally written to a 0.

Design Voltage

This is the theoretical nominal voltage of the battery pack. This value is used in ***ATRATE*** calculations and milliWatt mode (***Battery Mode*** MSByte bit 7).

Normal Setting: This varies by cell manufacturer, but Li-Ion is normally about 3.6-V per cell. See the cell manufacturer data sheet for the exact numbers. This value is programmed into ***Design Voltage*** on device initialization.

Spec Info

This performs two purposes. The high byte has the current and voltage multipliers. The bq20z40/bq20z45 does not require any multiplier, so use 0x00. The low byte is the SBS specification revision. See the SBS Implementers Forum web page for more information (http://www.sbs-forum.org/specs/index.html).

Normal Setting: 0x0031 for SBS specification v1.1 with PEC error checking, or 0x0021 for SBS specification V1.1 without PEC error checking.

Manuf Date

This is the date of manufacture. It is stored in the Data Flash in packed format. All bqEV Software and bqMTester both accept input of this date in standard date format so the packed format does not need to be used input. It is then translated by the software to packed format. This data does not affect the operation, nor is it used by the part in any way.

Ser. Num.

This is a 16 bit serial number that does not affect the operation nor is it used by the part in any way. It is normally used for battery identification.

Cycle Count(CC)

CC Threshold is used to increment *Cycle Count*. When the bq20z40/bq20z45 accumulates enough discharge capacity equal to the *CC Threshold* then it increments *Cycle Count* by 1. This discharge capacity does not have to be consecutive. In other words the internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *CC Threshold*. Then *Cycle Count* is incremented. Every increment of *Cycle Count* between QMAX updates will increment **Max Error** by 0.05%. It takes 20 increments of *Cycle Count* to increment **Max Error** by 1% so that it is visible in the SBS register.

Normal Setting: This should be set to 0.

CC Threshold

CC Threshold is used to increment *Cycle Count*. When the bq20z40/bq20z45 accumulates enough discharge capacity equal to the *CC Threshold*, then it increments *Cycle Count* by 1. This discharge capacity does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *CC Threshold* and increments *Cycle Count*.

Normal Setting: This is normally set to about 80% of the *Design Capacity*.

CF Max Error Limit

The bq20z40/bq20z45 forces [CF] to be set in ***Battery Mode*** if ***MaxErr*** goes above the value stored in this register. This value is used to give an alternate method for setting the [CF] flag in ***Battery Mode***, other than the impedance track algorithm. The [CF] flag is a condition request flag indicating the battery would like a full charge/discharge cycle, and rarely is set by impedance track because accurate capacity measurements are always updated.

Normal Setting: This register is normally set to 100 and is in units of %.

Design Capacity

Design Capacity is the data flash location that is reported in the ***Design Capacity*** register when [CapM] is clear in ***Battery Mode***. If [CapM] is set in ***Battery Mode***, then *Design Energy* is reported in ***Design Capacity***. This value is used also for the ***ASOC*** calculation by the bq20z40/bq20z45 if [CapM] is cleared in ***Battery Mode***.

Normal Setting: This value should be set based on the application battery specification. See the battery manufacturer data sheet.

Design Energy

Design Energy is the data flash location that is reported in the ***Design Capacity*** register if [CapM] is set in ***Battery Mode***. If [CapM] is clear in ***Battery Mode***, then *Design Capacity* is reported in *Design Capacity*. This value is used also for the ASOC calculation by the bq20z40/bq20z45 if [CapM] is set in ***Battery Mode***.

Normal Setting: This value is be set based on the application battery specification. See the battery manufacturer data sheet. At higher rates of discharge, energy is less, so referring to discharge data similar to the typical rate of the user's application is important to obtain a meaningful value.

Manuf Name

String data that can be a maximum of 11 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x20.

Device Name

String data that can be a maximum of 7 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x21.

Device Chemistry

String data that can be a maximum of 4 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x22.

Deterioration Warn Limit

The *Deterioration Warn Limit* is a warning that indicates the battery capacity has degraded significantly from it's original design capacity. If the absolute battery capacity, as indicated by **State Of Health** (low byte), falls below the *Deterioration Warn Limit*, the bq20z40/bq20z45 sets the [DetW] flag in **State Of Health** (high byte).

Deterioration Fault Limit

The *Deterioration Fault Limit* is a warning that indicates the battery capacity has degraded significantly from it's original design capacity and the battery is approaching the end of it's useful life. If the absolute battery capacity, as indicated by **State Of Health** (low byte), falls below the *Deterioration Fault Limit*, the bq20z40/bq20z45 sets the [DetF] flag in **State Of Health** (high byte).

Cell Life Limit

The *Cell Life Limit* is a warning that indicates the battery capacity has degraded significantly from it's original design capacity and the battery, for all practical purposes, has reached the end of it's useful life. If the absolute battery capacity, as indicated by **State Of Health** (low byte), falls below the *Cell Life Limit*, the bq20z40/bq20z45 sets the [CLL] flag in **State Of Health** (high byte).

5.2 Configuration

These are alternative methods for setting and clearing [TDA] and [FD] in ***Battery Status***. They are in addition to traditional methods or fault conditions explained in other areas of this document.

TDA Set %

If set to a value between 0 and 100 then when ***RSOC*** falls to or below this value, then [TDA] in ***Battery Status*** is set. If set to (–)1, then this function is disabled. *TDA Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference. This is the threshold that the bq20z40/bq20z45 requests that discharge be halted because the battery is nearing depletion. If used, it is normally set around 6%. Be sure that if *TDA Clear %* is used, then this should be used as well. They only work together.

TDA Clear %

If set to a value between 0 and 100 then when ***RSOC*** rises to or above this value after being set by *TDA Set %*, then [TDA] in ***Battery Status*** is cleared. This register can only be used to clear [TDA] if it was set by TDA Set %. If set to (–)1, then this function is disabled. *TDA Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 8%. Be sure that if *TDA Set %* is used then this should be used as well. They only work together.

FD Set %

If set to a value between 0 and 100 then when ***RSOC*** falls to or below this value then [FD] in ***Battery Status*** is set. If set to (–)1 then this function is disabled. *FD Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [FD] is completely unaffected by this register.

Normal Setting: This is user preference. This is a stronger request than TDA. The battery is presumed dead at this point. If used it is normally set around 2%. Be sure that if FD *Clear %* is used then this should be used as well.

FD Clear %

If set to a value between 0 and 100 then when ***RSOC*** rises to or above this value after being set by *FD Set %*, then [FD] in ***Battery Status*** is cleared. If set to (–)1, then this function is disabled. *FD Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 5%. If FD Set % is used, then this should be used as well. They only work together.

TDA Set Volt Threshold

When battery voltage as measured by ***Voltage*** falls to or below the *TDA Set Volt Threshold* value for *TDA Set Volt Time* seconds, then [TDA] in ***Battery Status*** is set. This works completely independent of *TDA Set %*. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 6% ***RSOC***.

TDA Set Volt Time

See *TDA Set Volt*. This is the time that the battery voltage must be equal to or below *TDA Set Volt Threshold* before [TDA] is set in ***Battery Status***.

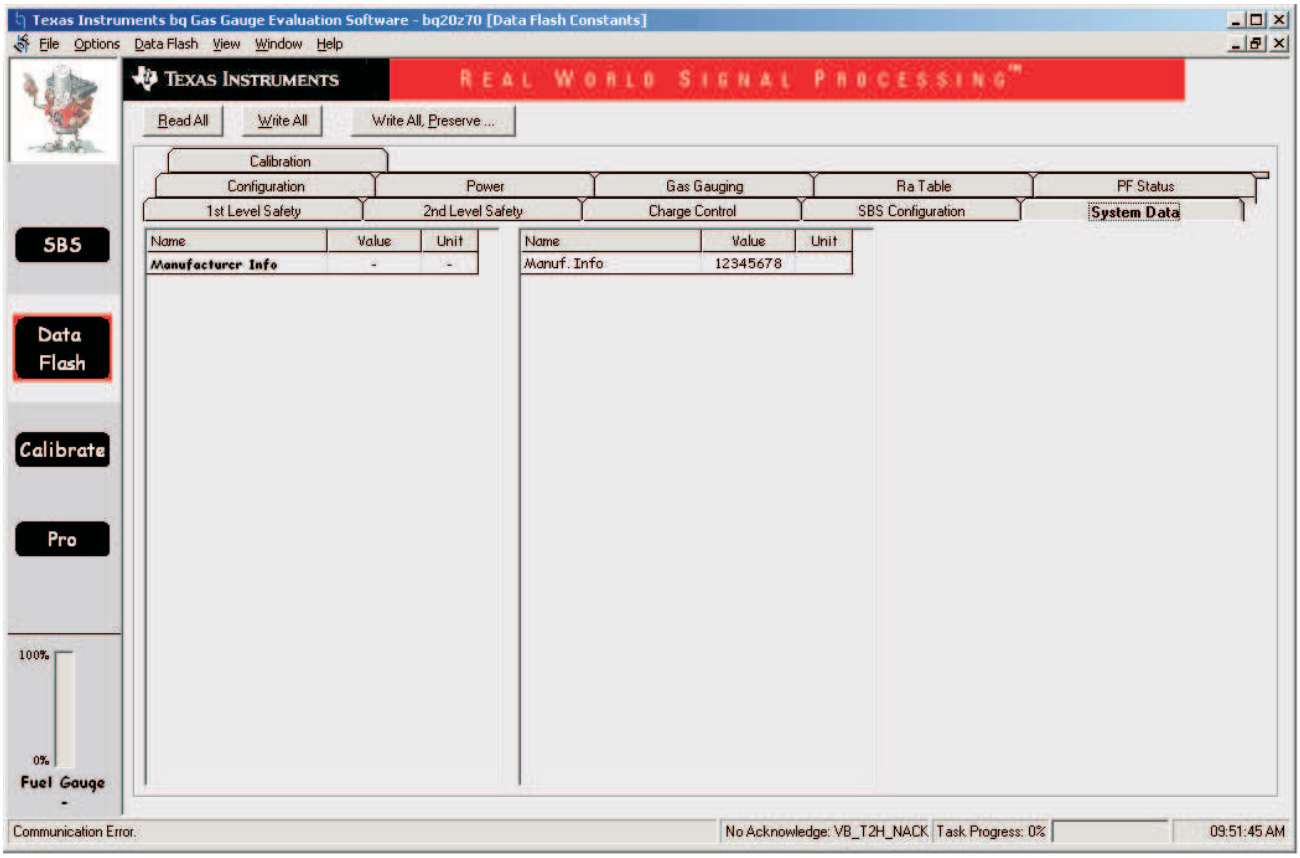
Normal Setting: This is normally set to 5 seconds but depends on the application.

TDA Clear Volt

When battery voltage (as measured by ***Voltage***) rises to or above this value, then [TDA] in ***Battery Status*** is cleared. [TDA] is only cleared with this threshold if it was set by *TDA Set Volt Threshold* criteria. It is not cleared if it was set by any other methods.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 8% ***RSOC***.

6 System Data



6.1 Manufacturer Info

Manuf. Info 0

This is string data that can be any user data. It can be a maximum of 31 characters.
Normal Setting: Can be used for any user data.

Manuf. Info 1

This is string data that can be any user data. It can be a maximum of 20 characters.
Normal Setting: Can be used for any user data.

Manuf. Info 2

This is string data that can be any user data. It can be a maximum of 20 characters.
Normal Setting: Can be used for any user data.

Manuf. Info 3

This is string data that can be any user data. It can be a maximum of 20 characters.
Normal Setting: Can be used for any user data.

Manuf. Info 4

This is string data that can be any user data. It can be a maximum of 20 characters.
Normal Setting: Can be used for any user data.

6.2 Lifetime Data

Lifetime Max Temp

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the maximum temperature as measured by **Temperature** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM location only updates *Lifetime Max Temp* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Temp* for 60 seconds.
2. If the internal RAM location is greater than *Lifetime Max Temp* by at least 1°C.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Temp

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the minimum temperature as measured by **Temperature** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM location only updates *Lifetime Min Temp* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is less than *Lifetime Min Temp* for 60 seconds.
2. If the internal RAM location is less than *Lifetime Min Temp* by at least 1°C.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Cell Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the maximum cell voltage as measured by Cell Voltage (Max) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM location only updates *Lifetime Max Cell Voltage* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Cell Voltage* for 60 seconds.
2. If the internal RAM location is greater than *Lifetime Max Cell Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Cell Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the minimum cell voltage as measured by Cell Voltage (Min) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM location only updates *Lifetime Min Cell Voltage* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is less than *Lifetime Min Cell Voltage* for 60 seconds.
2. If the internal RAM location is less than *Lifetime Min Cell Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Pack Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the maximum pack voltage as measured by **Voltage** is updated continuously in a reserved RAM location. To prevent flash wear out, this RAM location only updates with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Pack Voltage* for 60 seconds.
2. If the internal RAM location is greater than *Lifetime Max Pack Voltage* by at least 100 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Pack Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the minimum pack voltage as measured by **Voltage** is updated continuously in a reserved RAM location. To prevent flash wear out, this RAM location only updates with any one of the following 3 conditions:

1. Whenever the internal RAM location is less than *Lifetime Min Pack Voltage* for 60 seconds.
2. If the internal RAM location is less than *Lifetime Min Pack Voltage* by at least 100 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Chg Current

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the maximum current in the charge direction as measured by **Average Current** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Chg Current* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Chg Current* for 60 seconds.
2. If the internal RAM location is greater than *Lifetime Max Chg Current* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Dsg Current

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the maximum current in the discharge direction as measured by **Average Current** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Dsg Current* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than (-) *Lifetime Max Dsg Current* for 60 seconds.
2. If the internal RAM location is greater than (-) *Lifetime Max Dsg Current* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Chg Power

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the maximum power in the charge direction as measured by a reserved continually updated average power register (uses **Voltage** * **Current** in an internal averaging algorithm) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Chg Power* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Chg Power* for 60 seconds.
2. If the internal RAM location is greater than *Lifetime Max Chg Power* by at least 100 in units of 10 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Dsg Power

When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the maximum power in the charge direction as measured by a reserved continually updated average power register (uses **Voltage** * **Current** in an internal averaging algorithm) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Dsg Power* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than (-) *Lifetime Max Dsg Power* for 60 seconds.
2. If the internal RAM location is greater than (-) *Lifetime Max Dsg Power* by at least 100 in units of 10 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Avg Dsg Cur

Current is averaged over every discharge cycle. Every discharge cycle an internal unaccessible RAM Register (LastAverageCurrent) is updated with this average current. The maximum current in the discharge direction as measured by this last average discharge current register is updated continuously in a lifetime data reserved RAM location. When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the *Life Max Avg Dsg Cur* data flash register is updated from this RAM location but only with any one of the following 3 conditions:

1. Whenever the internal RAM location is **less** than (-) *Life Max Avg Dsg Cur* for 60 seconds..
2. If the internal RAM location is **less** than (-) *Life Max Avg Dsg Cur* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Avg Dsg Pow

Power is averaged over every discharge cycle. Every discharge cycle an internal unaccessible RAM Register (LastAveragePower) is updated with this average power. The maximum power in the discharge direction as measured by this last average discharge power register (uses **Voltage** * **Current** in an internal averaging algorithm) is updated continuously in a lifetime data reserved RAM location. When the Impedance Track Algorithm is enabled ([QEN] set in **Operation Status**), the *Life Max Avg Dsg Pow* data flash register is updated from this RAM location but only with any one of the following 3 conditions:

1. Whenever the internal RAM location is **less** than (-) *Life Max Avg Dsg Pow* for 60 seconds..
2. If the internal RAM location is **less** than (-) *Life Max Avg Dsg Pow* by at least 100 in units of 10 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Life Avg Temp

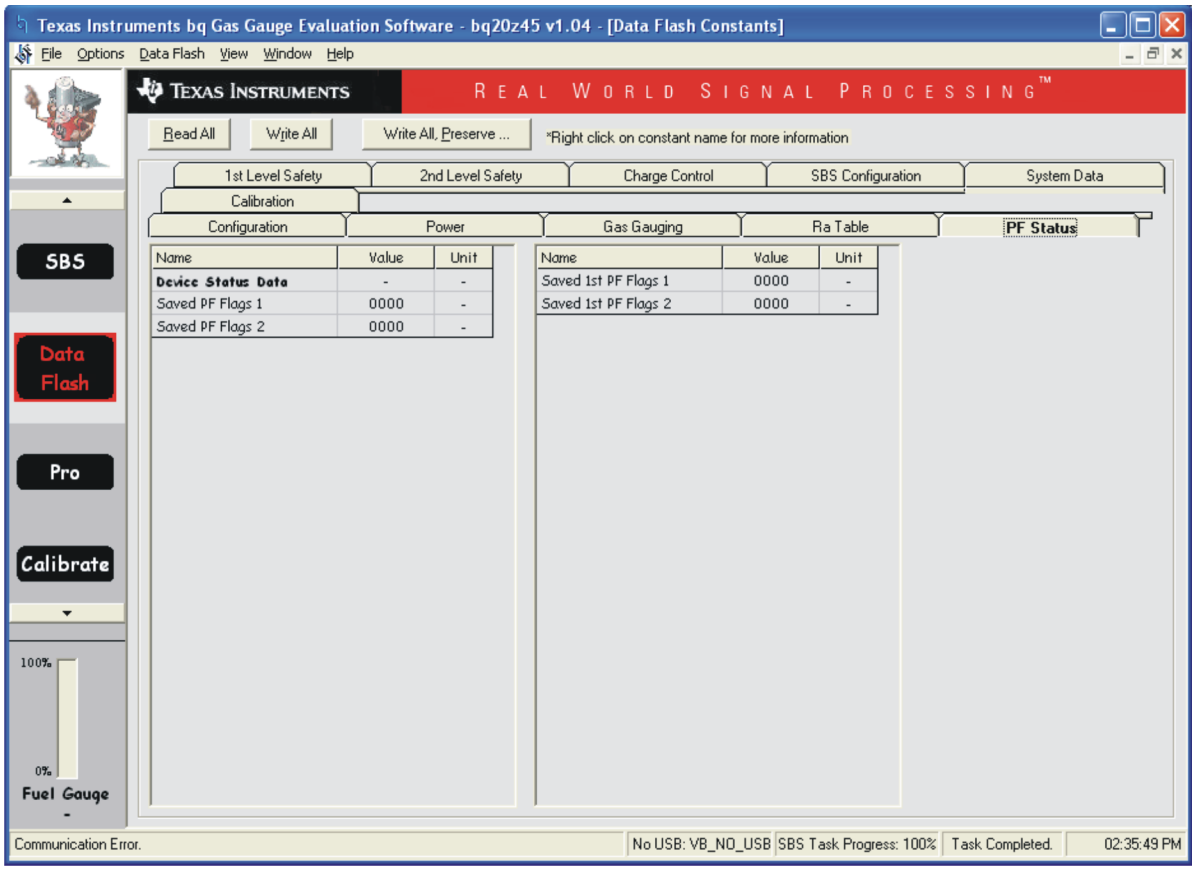
Temperature is averaged over the entire life of the battery. The temperature is sampled from the **Temperature** register every 1/16th of an hour. Then, it is added to the last Temperature Sum (**Temperature** + Previous Temperature Sum) as updated in the previous 1/16th of an hour sample. Finally, the value is divided by *LT Temp Samples*. This is then updated continuously in a lifetime data reserved RAM location. To prevent flash wear out, this RAM only updates to data flash when any other Lifetime Data locations update to data flash after meeting their update criteria. Impedance Track must be enabled ([QEN] set in **Operation Status**) for this data flash update to occur.

6.3 Lifetime Temp Samples

LT Temp Samples

LT Temp Samples is used to compute the *Lifetime Avg Temp*. Temperature is averaged over the entire life of the battery. The temperature is sampled from the **Temperature** register every 1/16th of an hour. Then, it is added to the last Temperature Sum (**Temperature** + Previous Temperature Sum) as updated in the previous 1/16th of an hour sample. Finally, the value is divided by *LT Temp Samples*. *LT Temp Samples* is then incremented by 1. *LT Temp Samples* is updated continuously in a lifetime data reserved RAM location. To prevent flash wear out, this RAM location only updates when any other Lifetime Data location updates to data flash after meeting their update criteria. Impedance Track must be enabled ([QEN] set in **Operation Status**) for this data flash update to occur.

7 PF Status



There is no configuration or settings required for the PF Status Class. The entire PF Status class should all be zeros for every register. This class is intended only for reporting failure information to the factory and Texas Instruments. In fact, it only reports any information with catastrophic failures or during development time as a tool to help with configuration or layout issues.

7.1 Device Status Data

Saved PF Flags 1

This location, along with *Saved PF Flags 2*, indicates all the causes of permanent failures that have occurred from the time the bq20z40/bq20z45 was last programmed with new firmware or the last time this register was cleared. It is important to understand that more than one fault can be recorded here if multiple faults have occurred. *Saved PF Flags 1* bit locations and definitions correspond to **PF Status**. If the corresponding bit in *Saved PF Flags 1* is enabled in the *Permanent Fail Cfg* register then the bq20z40/bq20z45 will attempt to blow the fuse in addition to record the permanent failure in the *Saved PF Flags 1* register. This register will be cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z40/bq20z45 (See the bq20z40/bq20z45 data sheet). This is the only register in the data flash which will ignore the disabled data flash writing setting when a permanent failure occurs. (See *Permanent Fail Cfg*).

—	PFVSHUT	SUV	—	SOCD	SOCC	AFE_P	AFE_C
DFF	DFETF	CFETF	CIM_R	SOT1D	SOT1C	SOV	PFIN

- PFVSHUT [14]: This bit causes much confusion for customers. At first, the attempt was to label it reserved, but there were many questions on its function. It serves no purpose in the operation of the bq20z40/bq20z45 but it does get set periodically. It does not function like any of the other PF Flags in that it there does not necessarily have to be a permanent failure for this flag to be set. It is basically a “shutdown” process monitor bit. When the bq20z40/bq20z45 starts the shutdown process, then it sets this bit. When it wakes, this bit is cleared. If this bit is set and then a real permanent failure occurs

during the shutdown process, then this bit is set along with the bit that indicates the actual permanent failure.

- SUV [13]: Set if a Safety Under Voltage Threshold Fault has occurred and the function is enabled. If *SUV Time* is set to 0 then this function is disabled. If [XSUV] is set in *Permanent Fail Cfg* then the SAFE pin will be driven high. (See *SUV Threshold*).
- SOCD [12]: Set if a Safety Over Current Discharge Fault has occurred and the function is enabled. If *SOC Dsg Time* is set to 0, then this function is disabled. If [XSOCD] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high. (See *SOC Dsg*).
- SOCC [11]: Set if a Safety Over Current Charge Fault has occurred, and the function is enabled. If *SOC Chg Time* is set to 0, then this function is disabled. If [XSOCC] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high (See *SOC Chg*).
- AFE_P [10]: Set if a Periodic AFE Check Fault has occurred and the function is enabled. If *AFE Check Time* is set to 0 then this function is disabled. If [XAFE_P] is set in *Permanent Fail Cfg* then the SAFE pin will be driven high. (See *AFE Check Time*).
- AFE_C [9]: Set if an AFE Communication Fault has occurred. If *AFE Fail Limit* is set to 0, then this function is disabled. If [XAFE_C] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high (See *AFE Fail Limit*).
- DFF [8]: The bq20z40/bq20z45 verifies all data flash writes and will set [DFF] if a Data Flash Verify Fault has occurred Only the setting of [DFF] can be disabled. If [XDFF] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high.
- DFETF [7]: Set if a Discharge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XDFETF] is set in *Permanent Fail Cfg* then the SAFE pin is driven high. (See *FET Fail Time*).
- CFETF [6]: Set if a Charge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XCFETF] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high. (See *FET Fail Time*).
- CIM_R [4]: Set if a Cell Imbalance at Rest Fault has occurred and the function is enabled. If *Rest CIM Time* or *Battery Rest Time* are set to 0 then that function is disabled. If [XCIM_R] is set in *Permanent Fail Cfg* then the SAFE pin will be driven high. (See *Rest CIM Time* and *Battery Rest Time*).
- SOT1D [3]: Set if a TS1 Safety Over Temperature Discharge Fault has occurred and the function is enabled. If *SOT1 Dsg Time* is set to 0 then this function is disabled. if [XSOT1D] is set in *Permanent Fail Cfg* then the SAFE pin will be driven high. (See *SOT1 Dsg Threshold*).
- SOT1C [2]: Set if a TS1 Safety Over Temperature Charge Fault has occurred and the function is enabled. If *SOT1 Chg Time* is set to 0 then this function is disabled. If [XSOT1C] is set in *Permanent Fail Cfg* then the SAFE pin will be driven high. (See *SOT1 Chg Threshold*).
- SOV [1]: Set if a Safety Over Voltage Threshold Fault has occurred and the function is enabled. If *SOV Time* is set to 0 then this function is disabled. If [XSOV] is set in *Permanent Fail Cfg* then the SAFE pin will be driven high. (See *LT SOV Threshold*, *ST SOV Threshold*, or *HT SOV Threshold*).
- PFIN [0]: The bq20z40/bq20z45 monitors the PFIN line. When the PFIN line goes low for *PFIN Detect Time*, then the bq20z40/bq20z45 attempts to report a PFIN Fault if the function is enabled. If *PFIN Detect Time* is set to 0, then this function is disabled. If [XPFIN] is set in *Permanent Fail Cfg*, then the SAFE pin is driven. (See *PFIN Detect Time*)

Saved PF Flags 2

This location *Saved PF Flags 1*, indicates all the causes of permanent failures that have occurred from the time the bq20z40/bq20z45 was last programmed with new firmware or the last time this register was cleared. It is important to understand that more than one fault can be recorded here if multiple faults have occurred. *Saved PF Flags 2* bit locations and definitions correspond to **PF Status 2**. If the corresponding bit in *Saved PF Flags 2* is enabled in the *Permanent Fail Cfg 2* register then the bq20z40/bq20z45 will attempt to blow the fuse in addition to record the permanent failure in the *Saved PF Flags 2* register. This register will be cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z40/bq20z45 (See the bq20z40/bq20z45 data sheet). This is the only register in the data flash which will ignore the disabled data flash writing setting when a permanent failure occurs. (See *Permanent Fail Cfg 2*).

—	—	—	—	—	—	—	—
—	—	—	—	—	SOT2D	SOT2C	CIM_A

- SOT2D [2]: Set if a TS2 Safety Over Temperature Discharge Fault has occurred and the function is enabled. If *SOT2 Dsg Time* is set to 0 then this function is disabled. if [XSOT2D] is set in *Permanent Fail Cfg 2* then the SAFE pin will be driven high. (See *SOT2 Dsg Threshold*)
- SOT2C [1]: Set if a TS2 Safety Over Temperature Charge Fault has occurred and the function is enabled. If *SOT2 Chg Time* is set to 0 then this function is disabled. If [XSOT2C] is set in *Permanent Fail Cfg 2* then the SAFE pin will be driven high. (See *SOT2 Chg Threshold*)
- CIM_A [0]: Set if a Cell Imbalance while Active Fault has occurred and the function is enabled. If *Active CIM Time* is set to 0 then that function is disabled. If [XCIM_A] is set in *Permanent Fail Cfg 2* then the SAFE pin will be driven high. (See *Active CIM Time*)

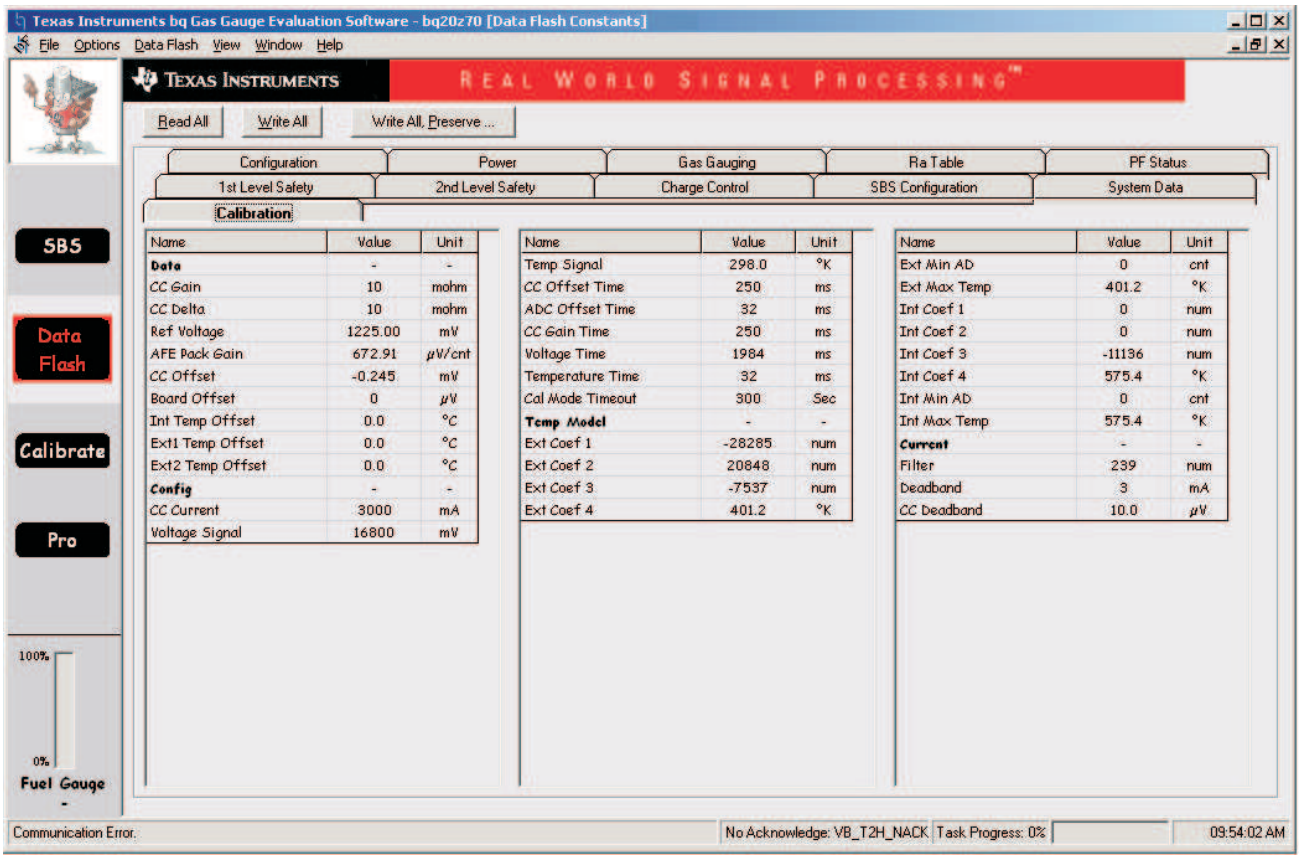
Saved 1st PF Flags 1

This register and *Saved 1st PF Flags 2* reports the first permanent failure that occurred from the time the bq20z40/bq20z45 was last programmed with new firmware. The difference between this register and *Saved PF Flags 1* is that this register only records one failure and it is the first one in a possible series of failures. This method gives a better chance to learn what could have caused a whole series of failures by knowing what the first failure was.

Saved 1st PF Flags 2

This register and *Saved 1st PF Flags 1* reports the first permanent failure that occurred from the time the bq20z40/bq20z45 was last programmed with new firmware. The difference between this register and *Saved PF Flags 2* is that this register only records one failure and it is the first one in a possible series of failures. This method gives a better chance to learn what could have caused a whole series of failures by knowing what the first failure was.

8 Calibration



8.1 Data

Most of these values should never need to be modified by the user. They should only be modified by the Calibration commands in Calibration mode as explained in the *Callibration Application Note* SLUA379A.

CC Gain

This is the gain factor for calibrating out Sense Resistor, Trace, and Internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports ***Current***. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports Current cancels out the time base since ***Current*** does not have a time component (it reports in mA) and *CC Delta* requires a time base for reporting ***Remaining Capacity*** (it reports in mAh).

Normal Setting: *CC Gain* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the latest calibration application note for the bq20z40/bq20z45 (SLUA379A: *Data Flash Programming and Calibrating the bq20zxx Family of Gas Gauges*) for more information on calibration.CC Gain

CC Delta

This is the gain factor for calibrating out Sense Resistor, Trace, and internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports charge and discharge in and out of the battery through the ***Remaining Capacity*** register. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports ***Current*** cancels out the time base since ***Current*** does not have a time component (it reports in mA) and *CC Delta* requires a time base for reporting ***Remaining Capacity*** (it reports in mAh).

Normal Setting: *CC Delta* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the latest calibration application note for the bq20z40/bq20z45 (SLUA379A: *Data Flash Programming and Calibrating the bq20zxx Family of Gas Gauges*) for more information on calibration.

Ref Voltage

The *Ref Voltage* is based on the actual reference voltage that the AFE uses for reference when sending voltage readings to the gauge. Therefore, this is a required constant in all the bq20z40/bq20z45 voltage computation formulas for displaying individual cell voltages (***Cell Voltage 1-4***) and the computed battery voltage (***Voltage***) in millivolts. By tweaking this value before it is used in the voltage computation formulas, the errors introduced by the gauge ADC and AFE reference are canceled out before they affect the reported voltages.

Normal Setting: *Ref Voltage* should never need to be modified by the user. It is modified by the voltage calibration command in Calibration mode. See the latest calibration application note for the bq20z40/bq20z45 (SLUA379A: *Data Flash Programming and Calibrating the bq20zxx Family of Gas Gauges*) for more information on calibration.

AFE Pack Gain

The *AFE Pack Gain* is used for calibrating out errors in the AFE reference and gauge ADC. It is used for reporting the ***Pack Voltage*** as measured on the PACK pin of the bq29330. Therefore, this is a required constant in all the bq20z40/bq20z45 voltage computation formulas for displaying ***Pack Voltage*** in millivolts. By tweaking this value before it is used in the voltage computation formulas, it changes the gain of the reported voltage which gives a method for calibrating this reported voltage.

Normal Setting: AFE Pack Gain may not need to be calibrated depending on the application. Unless ***Pack Voltage*** is used for display by the application then it is only used for charger detection, and it does not need to be accurate for function. *AFE Pack Gain* should never need to be modified by the user. It is modified by the pack voltage calibration command in Calibration mode. See the latest calibration application note for the bq20z40/bq20z45 (SLUA379A: *Data Flash Programming and Calibrating the bq20zxx Family of Gas Gauges*) for more information on calibration.

CC Offset

There are 2 offsets for calibrating the offset of the internal Coulomb Counter, board layout, sense resistor, copper traces and other offsets from the Coulomb Counter readings. *CC Offset* is the calibration value that primarily corrects for the offset error of the bq20z40/bq20z45 Coulomb Counter circuitry. The other offset calibration is *Board Offset* described below. To minimize external influences when doing *CC Offset* calibration either by either automatic *CC Offset* calibration or by the *CC Offset* calibration function in Calibration Mode an internal short is places across the SR1 and SR2 pins inside the bq20z40/bq20z45. *CC Offset* is a correction for very small noise/errors; therefore, to maximize accuracy, it takes about 20 seconds to calibrate out the offset. Since it is not practical to do a 20 second offset during production, 2 different methods for calibrating CC Offset were developed.

(A) The first method is to calibrate CC Offset by the putting the bq20z40/bq20z45 in Calibration Mode and initiating the CC Offset function as part of the entire bq20z40/bq20z45 calibration suite. See the SLUA379A for more information on Calibration Mode. This is a short calibration that is not as accurate as the second method described below. Its primary purpose is to calibrate CC Offset so that it will not affect any other Coulomb Counter calibrations. This is only intended as a temporary calibration because the automatic calibration described below is done the first time SMBus is low for more than 20 seconds which is a more accurate calibration.

(B) During normal Gas Gauge Operation (***Temperature*** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*) when the SMBus clock and data lines are low for more than *Bus Low Time* seconds and ***Current*** is less than *Sleep Current* in milliAmps then an automatic *CC Offset* calibration is performed. This takes around 16 seconds and is much more accurate than the method in Calibration mode.

Normal Setting: *CC Offset* should never be modified directly by the user. It is modified by the current calibration function from Calibration Mode or by Automatic Calibration. See the latest calibration application note for the bq20z40/bq20z45 (SLUA379A: *Data Flash Programming and Calibrating the bq20zxx Family of Gas Gauges*) for more information on calibration.

Board Offset

Board Offset is the second offset register. Its primary purpose is to calibrate all that the *CC Offset* does not calibrate out. This includes board layout, sense resistor and copper trace and other offsets that are external to the bq20z40/bq20z45 IC. The simplified ground circuit design in the bq20z40/bq20z45 requires a separate board offset for each tested device. The bq20z40/bq20z45 board offset calibration is explained in the SLUA379A application note.

Normal Setting: This value needs to be modified for each device being tested unlike the bq20z80. See the latest calibration application note for the bq20z40/bq20z45 (SLUA379A: *Data Flash Programming and Calibrating the bq20zxx Family of Gas Gauges*) for more information on calibration.

Int Temp Offset

The bq20z40/bq20z45 has a temperature sensor built into the IC. The *Int Temp Offset* is used for calibrating out offset errors in the measurement of the reported ***Temperature*** if the internal temperature sensor is used. The gain of the internal temperature sensor is accurate enough that a calibration for Gain is not required.

Normal Setting: *Int Temp Offset* should never need to be modified by the user. It is modified by the internal temperature sensor calibration command in Calibration mode. *Int Temp Offset* should only be calibrated if the internal temperature sensor is used. See the *Data Flash Programming/Calibrating the bq20zxx Family of Gas Gauges* application note SLUA379A for more information on calibration.

Ext1 Temp Offset

Ext1 Temp Offset is for calibrating the offset of the thermistor connected to the TS1 pin of the bq20z40/bq20z45 as reported by ***Temperature***. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting: *Ext1 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext1 Temp Offset* should only be calibrated if a thermistor is connected to the TS1 pin of the bq20z40/bq20z45. See the *Data Flash Programming/Calibrating the bq20zxx Family of Gas Gauges* application note SLUA379A for more information on calibration.

Ext2 Temp Offset

Ext2 Temp Offset is for calibrating the offset of the thermistor connected to the TS2 pin of the bq20z40/bq20z45 as reported by ***Temperature***. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting: *Ext2 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext2 Temp Offset* should only be calibrated if the a thermistor is connected to the TS1 pin of the bq20z40/bq20z45. See the *Data Flash Programming/Calibrating the bq20zxx Family of Gas Gauges* application note SLUA379A for more information on calibration.

8.2 Config

These are all setting for adjusting Calibration Mode applied voltage, current, and temperature as well as the times associated with these calibrations. The Times should not need to be modified with normal applications. The values in Data Flash for these registers are defaults for Calibration Mode. If no other values are assigned to the calibration commands associated with each of these registers when in Calibration Mode, then these default values are used. See the *Data Flash Programming/Calibrating the bq20zxx Family of Gas Gauges* application note SLUA379A for more information on calibration.

CC Current

This register holds the default current that is applied during the calibration process while in Calibration mode. While in calibration mode, if the *CC Current* is not modified by calibration command, then this value is what is used to calibrate *CC Gain* and *CC Delta*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z40/bq20z45.

Normal Setting: This depends on the sense resistor used. Higher currents increase the voltage across the SR1 and SR2 pins which decreases noise and offset errors. It also increases the calibration accuracy because the granularity has less effect on the measurements. Good numbers for a 10 milliohm sense resistor are 2 to 3 amps.

Voltage Signal

This register holds the default voltage that is applied during the calibration process while in Calibration Mode. While in calibration mode, if the *Voltage Signal* is not modified by calibration command, then this value is what is used to calibrate *Reference Voltage* and *AFE Pack Gain*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z40/bq20z45. This value is a pack voltage, not a cell voltage.

Normal Setting: This depends on the number of cells, but it is good idea to use a voltage that is within the normal operating voltages of the cells used in the application times the number of cells.

Temp Signal

This register holds the default Temperature that is applied during the calibration process while in Calibration Mode. If, while in calibration mode, the *Temp Signal* is not modified by calibration command then this value is what is used to calibrate all the Temperature inputs that are used in this application. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z40/bq20z45.
Normal Setting: This value more than any of the others must be modified using the calibration commands in Calibration Mode instead of using this Data Flash location because temperature is continually changing.

CC Offset Time

CC Offset Time is the time that the calibration command for initiating a *CC Offset* calibration takes to do a *CC Offset* calibration. This is also used in Board Offset calibration in the bq20z40/bq20z45 EV software.

Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function rounds the *CC Offset Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Remember that this is only a temporary calibration to minimize offset effects on other CC calibrations. The Automatic Offset calibration that happens during normal Gas Gauging mode does a more accurate calibration. It is important to note that this is also used by the bq20z40/bq20z45 EV software to do Board Offset calibration. It is a good idea to increase this number to 20,000 to get a very accurate board offset measurement for production testing (see *Board Offset*) .

ADC Offset Time

ADC Offset Time is the time that the calibration command for initiating an ADC Offset calibration takes for an ADC Offset calibration. *ADC Offset* is not associated with a Data Flash location, but it is done every time Automatic *ADC Offset* is done in Gas Gauging mode and should be initiated at the same time as *ADC Offset* when in Calibration Mode.

Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the *ADC Offset Time* down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It reports a calibration error if a value less than 32 is used. Remember that this is only a temporary calibration. The Automatic Offset calibration that happens during normal Gas Gauging mode keeps this value accurate.

CC Gain Time

CC Gain Time is the time that the calibration command for initiating a CC Gain calibration takes for a *CC Gain Time* calibration. It uses the value in *CC Current* over *CC Gain Time* to do the calibration.
Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function will round the *CC Gain Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Depending on the current used, it is possible that 250 ms not enough time for a good calibration. It is recommended that 500 ms to 1000 ms be used for best results.

Voltage Time

Voltage Time is the time that the calibration commands for initiating a *Reference Voltage* or *AFE Pack Gain* calibration takes for a *Reference Voltage* or *AFE Pack Gain* calibration. These commands use the value in *Voltage Signal* over *Voltage Time* to do the calibration.
Normal Setting: The default is 1984 and the units are in milliseconds. Only use values in multiples of 1984ms. The calibration function will round the *Voltage Time* down to the next lower multiple of 1984ms if an exact multiple of 1984 is not used. It will report a calibration error if a value less than 1984 is used.

Temperature Time

Temperature Time is the time that the calibration commands for initiating any of the *3 temperature* calibrations takes for the respective calibrations. These commands uses the value in *Temperature Signal* over *Temperature Time* to do the calibration.

Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the *Temperature Time* down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It reports a calibration error if a value less than 32 is used.

Cal Mode Timeout

Cal Mode Timeout is the maximum amount of time allowed for all calibrations to complete before the bq20z40/bq20z45 reverts to Gas Gauge mode automatically. The timer for this function starts when the ***Call Mode*** command is initiated.
Normal Setting: The purpose of this function is ensure that the bq20z40/bq20z45 has the ability to get out of Calibration Mode on its own if it was accidentally put into Calibration Mode for any reason. The default for this register is 300 which is in units of seconds. This translates to 5 minutes. It is unlikely that this register will need to be modified.

8.3 Temp Model

None of these registers must not be changed for any reason. The only reason these values are listed is for the purpose of using a different thermistor; however, this is not recommended, and has not been tested with the bq20z40/bq20z45 at the time this was written.

Ext Coef 1, Ext Coef 2, Ext Coef 3, Ext Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Ext Min AD

This is the minimum ADC value allowed for the Temperature conversion formula.
Normal Setting: This value is 0 and should not be changed.

Ext Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.
Normal Setting: This value is 4012 and should not be changed.

Int Coef 1, Int Coef 2, Int Coef 3, Int Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Int Min AD

This is the minimum ADC value allowed for the Temperature conversion formula.
Normal Setting: This value is 0 and should not be changed.

Int Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.
Normal Setting: This value is 4012 and should not be changed.

8.4 Current

Filter

This constant defines the filter constant used in the ***Average Current*** formula. This is a very common question how this is calculated. The formula used to compute ***Average Current*** is :

New (***Average Current***) = A × *Old* (***Average Current***) + (1-A) × ***Current***

A = *Filter*/256. Default value is 239

The time constant = 1 sec/ln(1/a) (default 14.5 sec)
Normal Setting: It is unlikely that this value should ever need to be changed.

Deadband

The purpose of the *Deadband* is to create a filter window to the reported ***Current*** register where the current is reported as 0. Any negative current above this value or any positive current below this value is displayed as 0.
Normal Setting: This defaults to 3 mA. There are not many reasons to change this value. Here are a few.

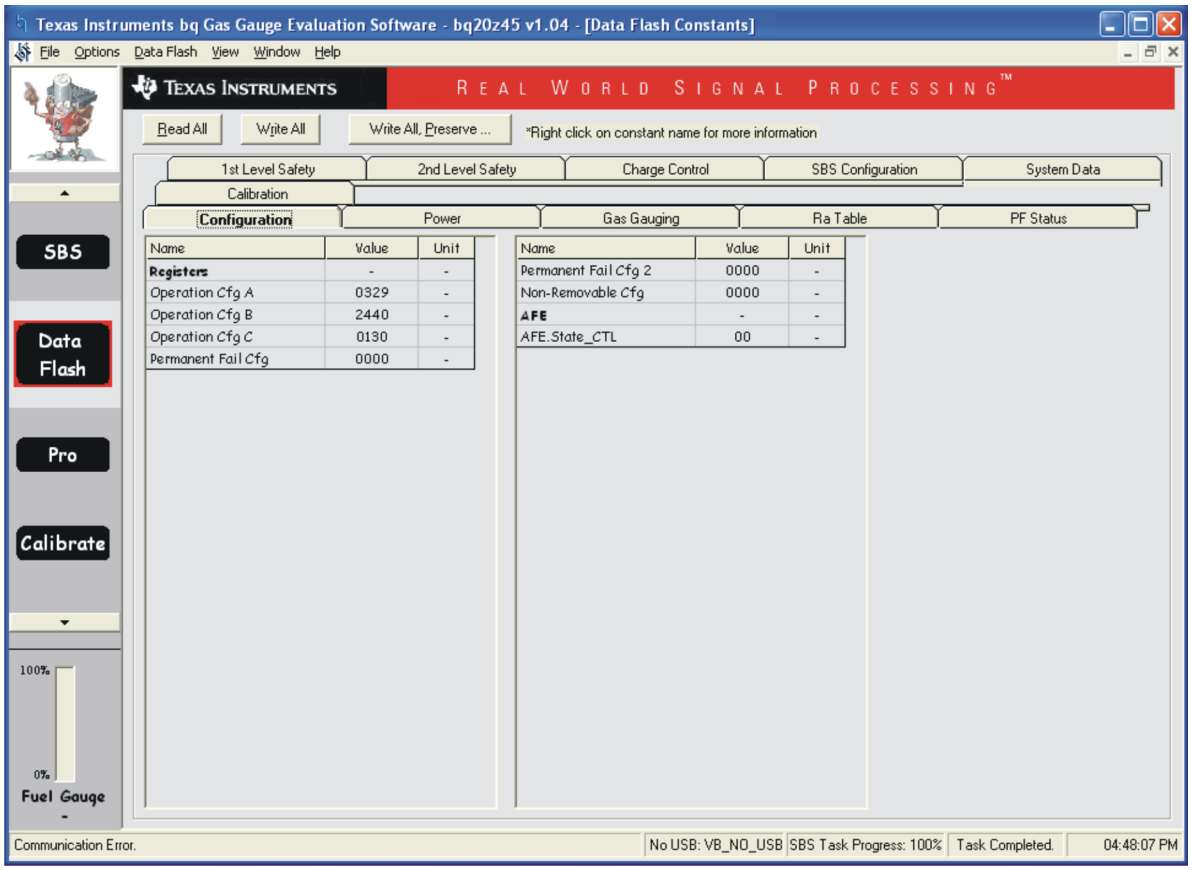
1. If the bq20z40/bq20z45 is not calibrated.
2. *Board Offset* has not been characterized.
3. If the PCB layout has issues that cause inconsistent board offsets from board to board.
4. An extra noisy environment in conjunction with number 3.
5. If the sense resistor is changed. *Deadband* is inversely proportional to the value of the sense resistor. For example, the default of 3mA corresponds to 30µV for a 10mOhm sense resistor. If the sense resistor is changed to 5mOhm, then the *Deadband* should be changed to 6mA (30µV) to be able to provide the same noise floor.

If this value must be modified be sure and verify the *CC Deadband* as well.

CC Deadband

This is also referred to as Digital Filter. This works much in the same way as the *Deadband* except it works for capacity counting on the ***Remaining Capacity*** register. Any absolute voltage between SR1 and SR2 below this value does not contribute to capacity measurement. The purpose of this is to minimize the possibility of unwanted noise from being counted towards capacity.
Normal Setting: The default for this register is 10 microvolts. This value is most likely too small for most applications. A better value would be 2 or 3 times this default. Unlike *Deadband* this value is not influenced by what value of sense resistor is used since this value is stored in microvolts and not milliamps.

9 Configuration



9.1 Registers

Operation Cfg A

This register is used to enable or disable various functions on the bq20z40/bq20z45. These bits are continued in *Operation Cfg B*.

—	—	—	—	—	—	CC1	CC0
—	—	SLEEP	TEMP1	TEMP0	—	ZVCHG1	ZVCHG0

- RESERVED [15-10]: These bits are reserved.
- CC1,0 [9,8]: These bits are used to tell the bq20z40/bq20z45 the number of LION battery cells in series the application has. This setting is critical for every aspect of the Data Flash configuration with regards to voltage based functions.
  - 1,1 = 4 series cell application
  - 1,0 = 3 series cell application
  - 0,1 = 2 series cell application
  - 0,0 = Reserved (Not Valid)

  Normal Setting: The default value for these bits are both set for a 4 series cell application. These bits are application and user dependant.
- RESERVED [7,6]:These bits are reserved
- SLEEP [5]: This bit enables or disables the ability to go to sleep when SMBus Clock and Data lines go low for *Bus Low Time* and ***Current*** is below *Sleep Current* (See *Sleep Current* and *Bus Low Time*)
  - 0: bq20z40/bq20z45 will not go to sleep with the above criteria
  - 1: bq20z40/bq20z45 will go to sleep when the sleep criteria is set

Normal Setting: This bit defaults to a 1 which should be used in most applications. There are very few reasons why this should be set to 0.

- Temp1,0 [4,3]: These bits are used to tell the bq20z40/bq20z45 the temperature sensor configuration. The bq20z40/bq20z45 can use up to 2 external sensors and there is also an internal sensor available if needed. All of these sensors are able to use various configurations to report temperature in the ***Temperature*** register.
  - 1,1 = The Average of TS1 and TS2 external inputs are used to generate ***Temperature***
  - 1,0 = Only Temperature sensor TS2 is used to generate ***Temperature***
  - 0,1 = Only Temperature sensor TS1 is used to generate ***Temperature***
  - 0,0 = 0,0 = Only internal temperature sensor is used to generate ***Temperature***.

  Normal Setting: The default setting for these bits is [Temp1] cleared and [Temp0] set. This requires one external temperature sensor on TS1. The bq20z40/bq20z45 default configuration is for a Semitec 103AT thermistor as briefly described in the ***Temp Model*** subclass (See ***Temp Model***). The internal temperature sensor is slightly less accurate than using a Semitc 103AT and is not recommended. It also is not as accurate because it cannot be put as close to the battery cells in the application as can be done with an external thermistor.
- RESERVED [2]: This bit is reserved
- ZVCHG1,0 [1,0]: These bits are also known as Pre-Charge 1,0. These bits are used to tell the bq20z40/bq20z45 how the Pre-Charge circuit is configured in the application. It tells the gauge what pin on the AFE to use for Pre-Charge functions when required.
  - 1,1 = No action is taken in Pre-Charge functions with this setting.
  - 1,0 = OD pin is used for Pre-Charge functions.
  - 0,1 = Charge FET is used for Pre-Charge functions.
  - 0,0 = ZVCHG FET is being used for Pre-Charge functions.

  Normal Setting: If using a separate Pre-Charge FET it is recommended not to use the OD pin for this function because it does not have good “zero volt charging” capabilities when a battery is completely dead. Therefore, the ZVCHG pin should be used because it has excellent clamping abilities. The default is for using the Charge FET pin on the bq29330.

Operation Cfg B

This register is used to enable or disable various functions on the bq20z40/bq20z45. This is a continuation of *Operation Cfg A*.

—	—	RESCAP	NCSMB	NRCHG	CSYNC	CHGTERM	—
CHGSUP	OTFET	CHGFET	CHGIN	NR	CPE	HPE	BCAST

- RESCAP [13]: The bq20z40/bq20z45 reports ***Remaining Capacity*** and ***Full Charge Capacity*** that is falsely lower than the actual capacity of the battery as defined by the *Reserve Cap-mAh* in mAh mode or *Reserve Cap-mW* in mWh mode (configured by [CAPM] in ***Battery Mode***). RESCAP sets a load compensation for this function.
  - 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
  - 1: If set to a 1, then a more normal rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See **IT Cfg** class)

  Normal Setting: This bit defaults to a 1. For most applications, this along with *Load Select* should be left at the default values.
- NCSMB [12]: This bit is used to enable a special mode for the SMBus engine in the bq20z40/bq20z45 where it allows for unlimited timeouts for SMBus communications more like I^2C. This mode was made for customers that were using older legacy parts that had longer timeouts and were not SMBus compliant.
  - 0: Timeout extension is disabled.
  - 1: Unlimited Timeout extension enabled.

  Normal Setting: The default for this register is 0. It is recommended that this always be set to 0. There have been many complications with customers using this function in the past. When set to a 1, it is

important to note that if clocking in data with a SMBus read command and the communication gets interrupted with data low then data can be stuck low until more clocks are sent to finish the communication.

- NRCHG [11]: This bit is used to configure whether or not the bq20z40/bq20z45 turns off the Charge FET when it goes to Sleep if [NR] bit is set in *Operation Cfg B*. If [NR] cleared then this bit is not used.
  - 0: Charge FET turns off in sleep mode as long as the bq20z40/bq20z45 is setup with [NR] set.
  - 1: Charge FET remains on in sleep mode with the [NR} bit set.

  Normal Setting: This bit defaults to a 0 which should be used for most applications with [NR] set. This could be a problem for some applications that expect the battery to start charging immediately when charge is applied when asleep.
- CSYNC [10]: This bit is used in the Primary Charge Termination Algorithm (See *Maintenance Current*). When this bit is set, then with a Primary Charge Termination the bq20z40/bq20z45 writes the ***Remaining Capacity*** to ***Full Charge Capacity***
  - 0: ***Remaining Capacity*** is not written up to ***Full Charge Capacity*** on Primary Charge Termination.
  - 1: ***Remaining Capacity*** is written up to ***Full Charge Capacity*** on Primary Charge Termination.

  Normal Setting: The default setting for this bit is 1. This should be used for most applications to ensure that the Remaining Capacity starts from ***Full Charge Capacity*** when the charger terminates charging. This is a synchronization function to ensure the bq20z40/bq20z45 discharges from full when it has been determined that the battery is full.
- CHGTERM [9]: This bit enables the ability for the bq20z40/bq20z45 to turn off [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination is detected and then ***Current*** falls below the *Chg Current Threshold* for 2 consecutive periods of *Taper Current Window*.
  - 0: bq20z40/bq20z45 does not clear [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination.
  - 1: bq20z40/bq20z45 does clear [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination.

  Normal Setting: This bit defaults to 0. This should be acceptable for most applications.
- CHGSUSP [7]: This bit enables the ability to turn off the Charge FET and/or Pre-Charge FET in charge suspend mode (See **Charge Control** Class).
  - 0 = The Charge FET is unaffected by any type of charge suspension.
  - 1 = The Charge FET and/or Pre-Charge FET are opened with any charge suspension.

  Normal Setting: The default setting for this bit is 0. It is common for this to be set to 1 to give the bq20z40/bq20z45 the control for additional protection.
- OTFET [6]: This bit is used to configure how the bq20z40/bq20z45 controls the current FETs (Charge or Discharge) during *Over Temp Chg* or *Over Temp Dsg* faults. (See *Over Temp Chg* and *Over Temp Dsg*)
  - 0: FET control is unaffected by any *Over Temp Chg* or *Over Temp Dsg* faults.
  - 1: During a *Over Temp Chg* fault the Charge FET is opened. During a *Over Temp Dsg* fault the Discharge FET is opened.

  Normal Setting: This bit defaults to a 1 which should be used in production for most applications. Over temperature conditions can be dangerous and every level of protection possible should be used.
- CHGFET [5]: This bit is used to configure how the bq20z40/bq20z45 controls the Charge FETs when [TCA] gets set in ***Battery Status***. (See *TCA Set* % for an explanation for when [TCA] gets set).
  - 0: Charge FET is unaffected anytime [TCA] gets set.
  - 1: Charge FET is turned off anytime [TCA] gets set.

  Normal Setting: This bit defaults to a 0 which should be used in production for most applications. Setting it to a 1 turns the Charge FET off is only if *Maintenance Current* is set to 0.
- CHGIN [4]: This bit is used to configure how the bq20z40/bq20z45 controls the Charge FETs when in charge inhibit mode. (See *Chg Inhibit Temp Low* and *Chg Inhibit Temp High*).
  - 0: Charge FET is unaffected when in charge inhibit mode.
  - 1: Charge FET is turned off when in charge inhibit mode.

Normal Setting: This bit defaults to a 0 which should be acceptable for most applications. It is important to note that this is different than charge suspend mode because this inhibits the charge cycle from occurring. This function acts while discharging.

- NR [3]: Use this bit to configure the bq20z40/bq20z45 for either a removable or a nonremovable battery pack. A removable pack uses the System Present pin (PRES) and a nonremovable pack does not. This affects many functions in the bq20z40/bq20z45. Primarily it affects the way it handles recovery methods of most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register is used to enable many nonremovable pack fault recovery methods for use with a removable pack. (See *NR Config* and **Current** subclass in **1st Level Safety** class)
  - 0: Configures battery for removable mode. Transition on System Present pin (PRES) triggers certain recovery functions. *NR Config* can be used to enable nonremovable functions for this mode as well
  - 1: Configures battery for nonremovable mode.

  Normal Setting: Default for this bit is application specific. Set to 0 for batteries that are removed, and use the PRES pin. Set to 1 for packs that do not use the PRES pin.
- CPE [2]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z40/bq20z45 broadcasts to the SMBus Device Address 0x12 (SMBus charger device address) (See SBS and SMBus specification that can be downloaded from the web).
  - 0: No PEC byte is sent to SMBus Device Address 0x12.
  - 1: Every broadcast from the bq20z40/bq20z45 to SMBus Device Address 0x12 includes a PEC byte as the last byte sent.

  Normal Setting: If a smart charger (SMBus Device Address 0x12) is used that is PEC capable, then this should be set to a 1. It is always recommended to use PEC when possible.
- HPE [1]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z40/bq20z45 broadcasts to the SMBus Device Address 0x14 (SMBus Host device address)
  - 0: No PEC byte is set to SMBus Device Address 0x14. (See SBS and SMBus specification that can be downloaded from the web)
  - 1: Every broadcast from the bq20z40/bq20z45 to SMBus Device Address 0x14 includes a PEC byte as the last byte sent.

  Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.
- BCAST [0]: This bit enables or disables Master Mode Message broadcasting periodically to a smart charger or host. The bq20z40/bq20z45 broadcasts are completely disabled (See SBS and SMBus specification that can be downloaded from the web)
  - 0: The bq20z40/bq20z45 never masters the SMBus for any reason.
  - 1: The bq20z40/bq20z45 is enabled to Master the bus periodically to inform a host or charger of critical information

  Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.

Operation Cfg C

This register is used to enable or disable various functions on the bq20z40/bq20z45. This is a continuation of Operation Cfg B.

—	—	—	—	—	—	CHGOCV_DIS	CELL_TAPER
—	—	OCV_WGHT	LOCK_0	SUV_MODE	SHUTV	PRE_ZT_PF_En	RSOCL

- RESERVED [15-10, 7, 6]: These bits are reserved.
- CHGOCV_DIS [9]: This bit prevents OCV readings from being taken when the battery voltage is less than the voltage that defines the upper bound of the OCV flat region and after having undergone a period of charging. OCV readings are still taken if the battery voltage is above the flat region or if the current rest period did not follow a charge period.
  - 1 = OCV reading is taken when under the flat volt max and having come from charge..
  - 0 = OCV reading is not taken when under the flat volt max and having come from charge.

  Normal Setting: This function is application specific. Some battery chemistries cause a jump in

Relative State of Charge in the situation described above after the OCV reading is taken. Default setting for this bit is a 0.

- CELL_TAPER[8]: Taper voltage (used for primary charge termination) is either cell voltage-based or pack voltage-based depending on this bit.
  - 1 = When set to 1 then taper voltage is cell voltage-based. (Cell Voltage (Max) + *Taper Voltage*) must be greater than (**Charging Voltage** / number of cells) in order for taper to occur.
  - 0 = When set to 0 then taper voltage is pack voltage-based. (**Voltage** + *Taper Voltage*) must be greater than **Charging Voltage** in order for taper to occur.

  Normal Setting: This function is application specific. Some customers like the option of being able to base taper on the maximum cell voltage rather than on the pack voltage. Default setting for this bit is a 1.
- OCV_WGHT[5]: This bit enables evaluation of the accuracy of each state of charge reading from OCV during relaxation. It is used to take into account both previous and new state of charge estimates weighed according to their respective accuracy. This results in improved accuracy and in reduction of **Relative State Of Charge** jumps after relaxation.
  - 1 = Evaluation of the accuracy of each state of charge reading from OCV during relaxation is enabled.
  - 0 = Evaluation of the accuracy of each state of charge reading from OCV during relaxation is disabled.

  Normal Setting: This function is application specific. In some situations after a relaxation **Relative State Of Charge** can jump up or down a few percent, depending on previous load variations and magnitudes. This function can prevent these jumps from occurring if the bit is set to 1.
- LOCK_0[4]: This bit prevents **Remaining Capacity** and **Relative State Of Charge** from increasing during relaxation after 0mAh/0% was reached during discharge.
  - 1 = **Remaining Capacity** and **Relative State Of Charge** are prevented from increasing during relaxation after 0mAh/0% was reached during discharge.
  - 0 = **Remaining Capacity** and **Relative State Of Charge** are NOT prevented from increasing during relaxation after 0mAh/0% was reached during discharge.

  Normal Setting: This function is application specific. In some situations after a relaxation at the end of discharge **Remaining Capacity** and **Relative State Of Charge** can jump up few percent, depending on previous load variations and magnitudes. This function can prevent these jumps from occurring if the bit is set to 1.
- SUV_MODE[3]: This bit controls the operation of the Safety Under Voltage Permanent Failure feature.
  - 1 = Cell voltage is checked only upon wakeup from Shutdown mode. Upon wakeup, the Charge and Pre-Charge FETs are turned off and the cell voltage is checked. If any cell voltage is below *SUV Threshold* then the Safety Under Voltage mechanism starts.
  - 0 = If, at any time, any cell voltage goes below the *SUV Threshold*, then the Safety Under Voltage Permanent Failure mechanism starts.

  Normal Setting: This function is application specific. It provides the option to only check for a Safety Under Voltage condition when exiting Shutdown mode. If a pack never enters Shutdown mode, then the pack most likely will not be damaged by a low voltage situation. This default mode for this function is to check for SUV at all times, so the bit is set to 0.
- SHUTV[2]: This bit configure the voltage threshold used when entering Shutdown mode.
  - 1 = Shutdown occurs when Cell Voltage (Min) falls below *Cell Shutdown Voltage* and **Current** is 0 mA or less for a period greater than 10s.
  - 0 = Shutdown occurs when **Voltage** falls below *Shutdown Voltage* and **Current** is 0 mA or less for a period greater than 10s.

  Normal Setting: This function is application specific. Some customers prefer cell based shutdown over pack based shutdown. Cell imbalances can cause issues with premature or late shutdown. This bit gives a bit more flexibility in controlling when the pack shuts down. This bit defaults to pack based shutdown.
- PRE_ZT_PF_En[1]: This bit enables or disables permanent failures from occurring before the Impedance Track algorithm is enabled.
  - 1 = All Permanent Failures are allowed regardless of whether the Impedance Track algorithm has been enabled or not.

– 0 = All Permanent Failures (except DFF) are prevented from occurring until the Impedance Track algorithm is enabled. Shutdown is also disabled.

Normal Setting: This is a very useful function. Customers have reported problems in the past with Permanent Failures occurring on the production line due to cell attachment and other tests. Setting this bit to 0 will prevent these failures from happening until the Impedance Track algorithm is enabled. Since enabling the algorithm is usually done at the end of the production line, Permanent Failures can be completely avoided during production.

- RSOCL[0]: This bit is used to modify the functionality of RSOC at 100%.
  - 1 = When set to 1, then ***RSOC*** is only written to 100% if there is a primary charge termination (see *Taper Current* for more information on primary charge termination).
  - 0 = When set to 0, then ***RSOC*** at 100% functions like every other percentage for RSOC. When it reaches 99%, then any fraction above 99% in the ***RSOC*** computation will force ***RSOC*** to be written to 100%

  Normal Setting: This function is very application specific. Some customers have requested that they do not want ***RSOC*** to be 100% under any circumstances unless the bq20z40/bq20z45 detects a full condition. If this is a requirement, then consider setting this to a 1.

Permanent Fail Cfg

This enables or disables the various permanent failure protection functions ability to activate the SAFE output or not when the function is triggered.

—	XVSHUT	XSUV	—	XSOCD	XSOCC	XAFE_P	XAFE_C
XDFF	XDFETF	XCFETF	XCIM_R	XSOT1D	XSOT1C	XSOV	XPFIN

- RESERVED [15–12]: These bits are reserved. Even XVSHUT serves no purpose. These bits should always be set to 0.
- XSUV [13]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Under Voltage condition. (See *SUV Threshold*)
  - 0: The SAFE pin is not activated for a Safety Under Voltage Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a Safety Under Voltage Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is highly recommended that [XSUV] be set for production packs to protect against hazardous failures.
- XSOCD [11]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an Safety Over Current in the discharge direction condition. (See *SOC Dsg*)
  - 0: The SAFE pin is not activated for a Safety Over Current in the discharge direction Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a Safety Over Current in the discharge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOCD] be set for production packs to protect against hazardous failures.
- XSOCC [10]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Current in the charge direction condition. (See *SOC Chg*).
  - 0: The SAFE pins are not activated for a Safety Over Current in the charge direction Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a Safety Over Current in the charge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOCC] be set for production packs to protect against hazardous failures.

- XAFE_P [9]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a periodic AFE verification failure. (See *AFE Check Time*)
  - 0: The SAFE pin is not activated for a periodic AFE verification failure.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a periodic AFE verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is highly recommended that [XAFE_P] be set for production packs to protect against hazardous failures.
- XAFE_C [8]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an AFE communication verification failure. (See *AFE Fail Limit*)
  - 0: The SAFE pin are not activated for an AFE communication verification failure.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for an AFE communication verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XAFE_C] be set for production packs to protect against hazardous failures.
- XDFF [7]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Data Flash verification failure. (See *PF Flags 1*)
  - 0: The SAFE pin is not activated and the *Fuse Flag* is not written to 0x3672 for a Data Flash verification failure.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a Data Flash verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFF] be set for production packs to protect against hazardous failures.
- XDFETF [6]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Discharge FET Failure condition. (See *FET Fail Limit*)
  - 0: The SAFE pin is not activated for a Discharge FET Failure Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a Discharge FET Failure Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFETF] be set for production packs to protect against hazardous failures.
- XCFETF [5]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Charge FET Failure condition . (See *FET Fail Limit*)
  - 0: The SAFE pin is not activated for a Charge FET Failure Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a Charge FET Failure Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCFETF] be set for production packs to protect against hazardous failures.

- XCIM_R [4]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a extreme Cell Imbalance at Rest condition. (See *Rest CIM Fail Voltage*)
  - 0: The SAFE pin is not activated for an extreme Cell Imbalance at Rest Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for an extreme Cell Imbalance at Rest Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is highly recommended that [XCIM_R] be set for production packs to protect against hazardous failures.
- XSOT1D [3]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a TS1 Safety Over Temperature in the discharge direction condition. (See *SOT1 Dsg Threshold*)
  - 0: The SAFE pin is not activated for a TS1 Safety Over Temperature in the discharge direction Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a TS1 Safety Over Temperature in the discharge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is highly recommended that [XSOT1D] be set for production packs to protect against hazardous failures.
- XSOT1C [2]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a TS1 Safety Over Temperature in the charge direction condition. (See *SOT1 Chg Threshold*)
  - 0: The SAFE pin are not activated for a TS1 Safety Over Temperature in the charge direction Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a TS1 Safety Over Temperature in the charge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is highly recommended that [XSOT1C] be set for production packs to protect against hazardous failures.
- XSOV [1]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Voltage condition. (See *SOV Threshold*).
  - 0: The SAFE pin are not activated for a Safety Over Voltage Condition.
  - 1: The SAFE pin is driven high for a Safety Over Voltage Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOV] be set for production packs to protect against hazardous failures.

- XPFIN [0]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a PFIN input low condition. (See *PFIN Detect Time*)
  - 0: The SAFE pin is not activated for a PFIN input low Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a PFIN input low Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XPFIN] be set for production packs to protect against hazardous failures.

Permanent Fail Cfg 2

This enables or disables various permanent failure protection functions ability to activate the SAFE output or not when the function is triggered.

—	—	—	—	—	—	—	—
—	—	—	—	—	XSOT2D	XSOT2C	XCIM_A

- RESERVED [15-3]: These bits are reserved.
- XSOT2D [2]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a TS2 Safety Over Temperature in the discharge direction condition. (See *SOT2 Dsg Threshold*)
  - 0: The SAFE pin is not activated for a TS2 Safety Over Temperature in the discharge direction Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a TS2 Safety Over Temperature in the discharge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is highly recommended that [XSOT2D] be set for production packs to protect against hazardous failures.
- XSOT2C [1]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a TS2 Safety Over Temperature in the charge direction condition. (See *SOT2 Chg Threshold*)
  - 0: The SAFE pin is not activated for a TS2 Safety Over Temperature in the charge direction Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for a TS2 Safety Over Temperature in the charge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is highly recommended that [XSOT2C] be set for production packs to protect against hazardous failures.
- XCIM_A [0]: This bit enables the ability for the bq20z40/bq20z45 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a extreme Cell Imbalance while Active condition. (See *Active CIM Fail Voltage*)
  - 0: The SAFE pin is not activated for an extreme Cell Imbalance while Active Condition.
  - 1: The SAFE pin is driven high on the bq20z40/bq20z45 for an extreme Cell Imbalance while Active Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is highly recommended that [XCIM_A] be set for production packs to protect against hazardous failures.

Non-Removable Cfg

This register affects the way the bq20z40/bq20z45 handles recovery methods for most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register can be used to enable many nonremovable pack fault recovery methods for use with a removable pack. NR Config can be used to enable nonremovable fault recovery functions for a battery pack that is configured as removable.

—	—	OCD	OCC	—	—	—	—
—	—	—	—	—	AOCD	ASCC	ASCD

- RESERVED [15, 14]: These bits are reserved.
- OCD [13]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z40/bq20z45. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the discharge direction fault (See (OC*1st Tier) Dsg*).
  - 0: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is not enabled.
  - 1: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- OCC [12]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z40/bq20z45. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the charge direction fault (See *OC (1st Tier) Chg*).
  - 0: The nonremovable recovery option associated with *OC (1st Tier) Chg* is not enabled
  - 1: The nonremovable recovery option associated with *OC (1st Tier) Chg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- RESERVED [11-3]: These bits are reserved.
- AOCD [2]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z40/bq20z45. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE Over Current in the discharge direction fault (*AFE OC Dsg*).
  - 0: The nonremovable recovery option associated with *AFE OC Dsg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE OC Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- ASCC [1]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z40/bq20z45. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the charge direction fault (*AFE SC Chg*).
  - 0: The nonremovable recovery option associated with *AFE SC Chg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE SC Chg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- ASCD [0]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z40/bq20z45. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the discharge direction fault (*AFE SC Dsg*).
  - 0: The nonremovable recovery option associated with *AFE SC Dsg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE SC Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

AFE.State_CTL

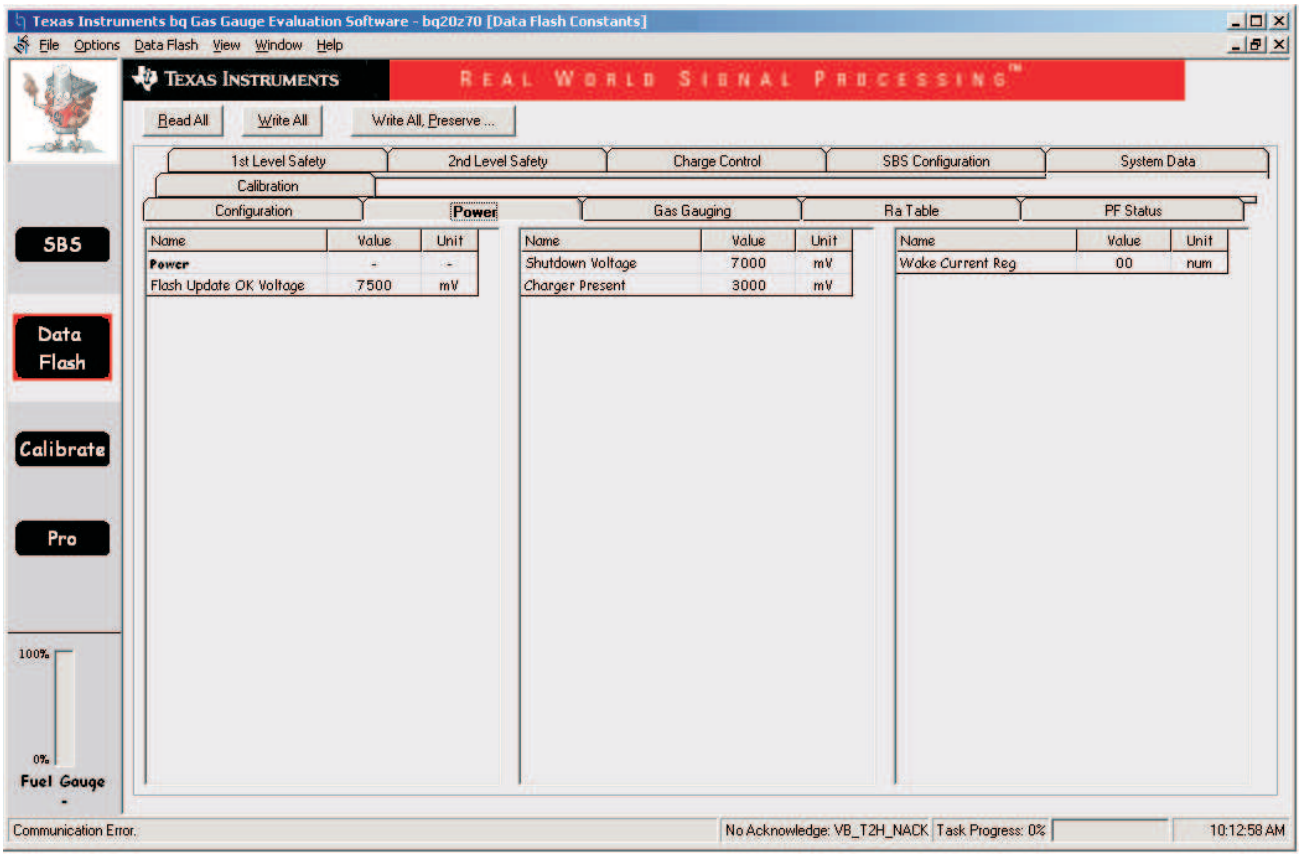
This register implements the STATE_CONTROL register for the AFE.

—	—	—	RSNS	—	—	—	—

- RESERVED [7-5, 3-0]: These bits are reserved.
- RSNS [4]: If this bit is set to 1, then the *AFE OC Dsg*, *AFE SC Chg Cfg*, and *AFE SC Dsg Cfg* voltage thresholds are divided by 2, which is suitable for low sense resistor values.

  Normal Setting: This bit defaults to 0. This is application specific. If using a small value sense resistor (<5 milliOhms) setting this bit will lower the voltage thresholds required to trigger the AFE current protection mechanisms. If this bit is not set when using a small value sense resistor, the lowest voltage setting may be too high for the application.

10 Power



10.1 Power

Flash Update OK Voltage

This register controls one of several data flash protection features. It is critical that data flash is not updated when the battery voltage is low. Data Flash programming takes much more current than normal operation of the gauge/AFE chipset and with a depleted battery this current can cause the battery voltage to crater (drop dramatically) forcing the bq20z40/bq20z45 into reset before completing a data flash write. The effects of an incomplete Data Flash write can corrupt the memory resulting in unpredictable and extremely undesirable results. The voltage setting in *Flash Update OK Voltage* is used to prevent any writes to the data flash below this value. If a charger is detected then this register is ignored.

Normal Setting: The default for this register is 7500 millivolts. For 2-cell applications, this can cause production issues with writing to the data flash because at nominal cell voltages, 2-cell applications can easily be below 7500 millivolts. The way to solve this problem is to connect a charger voltage to the battery which overrides this register while connected. Ensure that this register is set to a voltage where the battery has plenty of capacity to support data flash writes but below any normal battery operation conditions.

Shutdown Voltage

The bq20z40/bq20z45 goes into shutdown mode when ***Voltage*** falls below the *Shutdown Voltage* for at least Shutdown Time seconds. Also ***Current*** must be less than 0 and the ***Pack Voltage*** must be less than *Charger Present* for the entire time. So when the following conditions are met:

1. ***Voltage*** is below *Shutdown Voltage*
2. ***Current*** is less than 0
3. ***Pack Voltage*** less than *Charger Present*

Then a 10 second timer is initiated. If the above conditions remain until the timer expires, then the bq20z40/bq20z45 goes into shutdown mode. Every time the bq20z40/bq20z45 wakes up from shutdown mode, the 10 second timer is reset. It is not possible for the bq20z40/bq20z45 to go back into shutdown mode for 10 seconds after waking. When in shutdown mode, VCC is completely removed from the gauge by the AFE.
Normal Setting: This voltage should be far below any normal operating voltage but above any threshold that can cause damage to the cells. This threshold is met after the Charge and Discharge FETs are turned off from an under voltage fault condition.

Cell Shutdown Voltage

The bq20z40/bq20z45 will go into shutdown mode when the lowest **Cell Voltage** falls below the *Cell Shutdown Voltage* for at least 10 seconds. Also **Current** must be less than 0 and the **Pack Voltage** must be less than *Charger Present* for the entire time. So when the following conditions are met:

1. ***Cell voltage*** is below *Cell Shutdown Voltage*
2. ***Current*** is less than 0
3. ***Pack Voltage*** less than *Charger Present*

Then a 10 second timer is initiated. If the above conditions remain until the timer expires, then the bq20z40/bq20z45 goes into shutdown mode. Every time the bq20z40/bq20z45 wakes up from shutdown mode, the 10 second timer is reset. It is not possible for the bq20z40/bq20z45 to go back into shutdown mode for 10 seconds after waking. When in shutdown mode, VCC is completely removed from the gauge by the AFE.
Normal Setting: This voltage should be far below any normal operating voltage but above any threshold that can cause damage to the cells. This threshold is met after the Charge and Discharge FETs are turned off from an under voltage fault condition.

Charger Present

A charger is deemed present when ***Pack Voltage*** is at or above this level.
Normal Setting: It is important to note that a charger detection because this function prevents shutdown by either a ***Manufacture Access*** command or *Shutdown Voltage*. Some applications with external voltage sources can confuse the shutdown detection which prevents the bq20z40/bq20z45 shutdown mode from functioning properly. The AFE wakes up with a voltage above the “Start-up” voltage which is a wake up feature built into the AFE (see the bq29330 data sheet: SLUS673). If there is an external voltage source that has a voltage above the “Start-up” voltage threshold, but below the *Charger Present* threshold, then the gauge oscillates between awake and shutdown. This causes abnormal operational side effects. Therefore, it is recommended that *Charger Present* be set to 3000-4000 mV if there are any external voltage sources. Otherwise, this voltage can be set to between (3000–4000 mV per cell) × (number of cells).

Sleep Current

When **Current** is less than *Sleep Current* or greater than (-)*Sleep Current* in mA and the following conditions are met:

1. **Temperature** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*
2. SMBus clock and data lines are low for more than *Bus Low Time* seconds
3. [Sleep] is set in *Operation Cfg A*

Then the bq20z40/bq20z45 will do a CC Offset calibration and go to sleep.
Normal Setting: This setting should be below any normal application currents. The default is 10 mA which should be sufficient for most applications.

Wake Current Reg

This is one option for waking the bq20z40/bq20z45 from sleep. When the ***Current*** becomes more than what is set in *Wake Current Reg*, then the bq20z40/bq20z45 wakes from sleep.
Normal Setting: The default for this register is 0x00. This means that the function is disabled. The function is based on current; therefore, a sense resistor value must be selected as part of the option in (RSNS1, RSNS0).

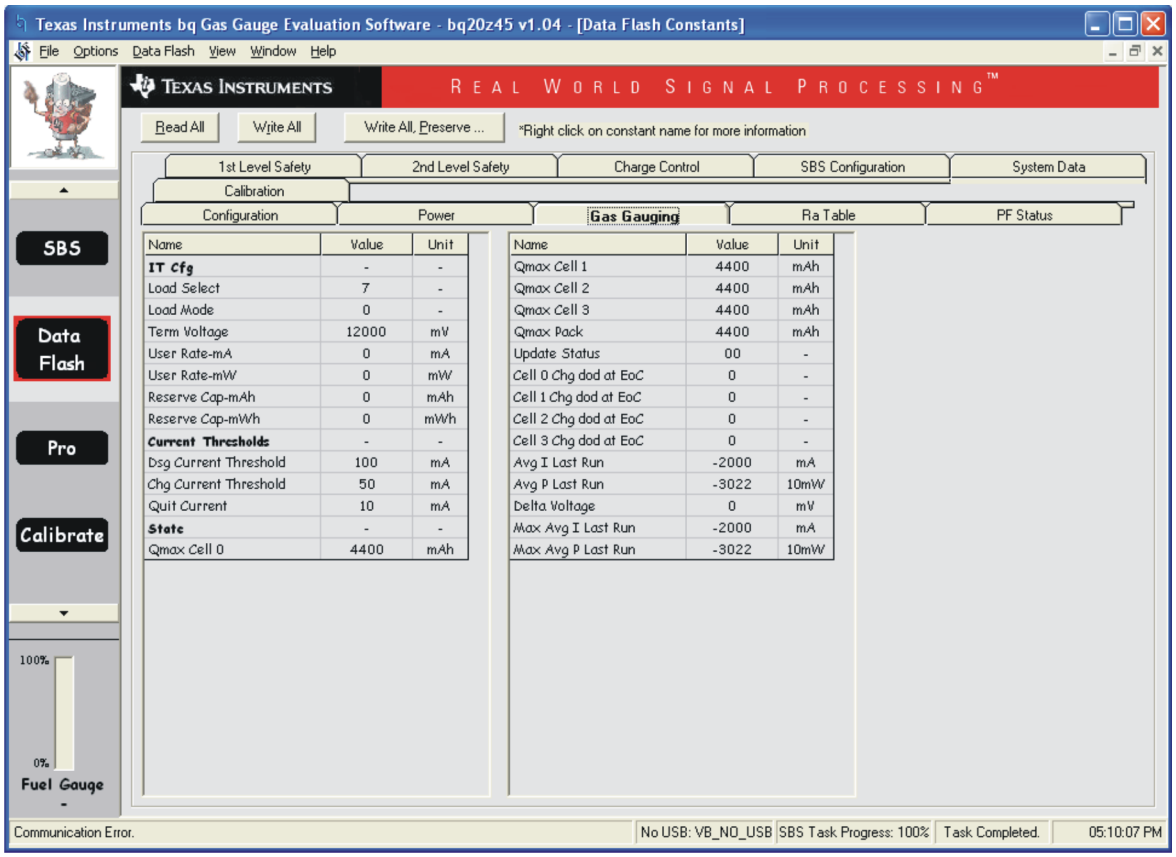
—	—	—	—	—	—	—	—
—	—	—	—	—	IWAKE	RSNS1	RSNS0

IWAKE	RSNS1	RSNS0	Current	Sense Resistor Value
0	0	0	Disabled	Disabled
0	0	1	0.5 A	2.5 mΩ
0	1	0	0.5 A	5 mΩ
0	1	1	0.5 A	10 mΩ
1	0	0	Disabled	Disabled
1	0	1	1 A	2.5 mΩ
1	1	0	1 A	5 mΩ
1	1	1	1 A	10 mΩ

Sealed Ship Delay

After the bq20z40/bq20z45 receives the 2 consecutive MAC (0x0010) commands in sealed mode, the CHG, DSG, and ZVCHG FETs are turned off after *Sealed Ship Delay* time period. After the passage of another *Sealed Ship Delay* period the bq20z60/bq20z65 enters ship mode (i. e . 2 times *Sealed Ship Delay* after the 2 MAC commands).
Normal Setting: The default for this register is 5 seconds. This feature is used specifically for production.

11 Gas Gauging



11.1 IT Config

Load Select

Load Select defines the type of power or current model to be used for *Remaining Capacity* computation in the Impedance Track™ algorithm. If *Load Mode* = Constant Current, then the following options are available:

0 = Average discharge current from previous cycle: There is an internal register that records the average discharge current through each entire discharge cycle. The previous average is stored in this register.

1 = Present average discharge current: This is the average discharge current from the beginning of this discharge cycle till present time.

2 = ***Current***: based off of ***Current***

3 = ***Average Current*** (default): based off the ***Average Current***

4 = ***Design Capacity*** / 5: C Rate based off of ***Design Capacity*** /5 or a C / 5 rate in mA.

5 = ***AtRate*** (mA): Use whatever current is in ***AtRate***

6 = *User_Rate-mA*: Use the value in *User_Rate-mA*. This gives a completely user configurable method.

7 = Maximum of **Average Current** from the previous discharge cycle.

If *Load Mode* = Constant Power then the following options are available:

0 = Average discharge power from previous cycle: There is an internal register that records the average discharge power through each entire discharge cycle. The previous average is stored in this register.

1 = Present average discharge power: This is the average discharge power from the beginning of this discharge cycle till present time.

2 = ***Current* × *Voltage***: based off of ***Current*** and ***Voltage***

3 = ***Average Current*** × ***Voltage*** (default): based off the ***Average Current*** and ***Voltage***

4 = ***Design Energy*** / 5: C Rate based off of ***Design Energy*** /5 or a C / 5 rate in mA

5 = ***AtRate*** (10 mW): Use whatever value is in ***AtRate***.

6 = *User_Rate-10mW*: Use the value in *User_Rate-mW*. This gives a completely user configurable method.

7 = Maximum of the average power from the previous discharge cycle.

Normal Setting: The default for this register is 7 which should be acceptable for most applications. This is application dependent.

Load Mode

Load Mode is used to select either the constant current or constant power model for the Impedance Track™ algorithm as used in *Load Select*. (See *Load Select*)

- 0: Constant Current Model
- 1: Constant Power Model

Normal Setting: This is normally set to Current Model but It is application specific. If the application load profile more closely matches a constant power model, then set to 1.

Term Voltage

Term Voltage is used in the Impedance Track™ algorithm to help compute ***Remaining Capacity***. This is the absolute minimum voltage for end of discharge.
Normal Setting: This register is application dependent. It should be set based on battery cell specifications to prevent damage to the cells or the absolute minimum system input voltage taking into account impedance drop from the PCB traces, FETs, and wires.

User Rate-mA

User Rate-mA is only used if *Load Select* is set to 6 and *Load Mode* = 0. If these criteria are met then the current stored in this register is used for the ***Remaining Capacity*** computation in the Impedance Track™ algorithm. This is the only function that uses this register.
Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined current at the end of discharge. With this type of discharge, it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment *Term Voltage* is reached.

User Rate-mW

User Rate-mW is only used if *Load Select* is set to 6 and *Load Mode* = 1. If these criteria are met, then the power stored in this register is used for the ***Remaining Capacity*** computation in the Impedance Track™ algorithm. This is the only function that uses this register.
Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined power at the end of discharge. With this application. it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment *Term Voltage* is reached.

Reserve Cap-mAh

Reserve Cap-mAh determines how much actual remaining capacity exists after reaching SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 0. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- [RESCAP]=0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity

- [RESCAP]=1: If set to a 1, then a higher rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mA mode (configured by [CAPM] in ***Battery Mode***).
Normal Setting: This register defaults to 0 which disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarmlike remaining* or *Remaining Capacity Alarm*.

Reserve Cap-mWh

Reserve Cap-mWh determines how much actual remaining capacity exists after reaching SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 1. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
- 1: If set to a 1, then a more normal rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mW mode (configured by [CAPM] in ***Battery Mode***).
Normal Setting: This register defaults to 0 which basically disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarm* or *Remaining Capacity Alarm*.

11.2 Current Thresholds

Dsg Current Threshold

This register is used as a threshold by many functions in the bq20z40/bq20z45 to determine if actual discharge current is flowing into and out of the part. This is independent from [DSG] in ***Battery Status*** which indicates whether the bq20z40/bq20z45 is in discharge mode or charge mode.
Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. If the bq20z40/bq20z45 is charging, then [DSG] is 0 and any other time (***Current*** less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z40/bq20z45 require more definitive information about whether current is flowing in either the charge or discharge direction. *Dsg Current Threshold* is used for this purpose. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Chg Current Threshold

This register is used as a threshold by many functions in the bq20z40/bq20z45 to determine if actual charge current is flowing into and out of the part. This is independent from [DSG] in ***Battery Status*** which indicates whether the bq20z40/bq20z45 is in discharge mode.
Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. Basically, if the bq20z40/bq20z45 is charging then [DSG] is 0 and any other time (***Current*** less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z40/bq20z45 require more definitive information about whether current is flowing in either the charge or discharge direction. This is what *Dsg Current Threshold* is used for. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Quit Current

The *Quit Current* is used as part of the Impedance Track™ algorithm to determine when the bq20z40/bq20z45 goes into relaxation mode from a current flowing mode in either the charge direction or the discharge direction. Either of the following criteria must be met to enter relaxation mode:

1. ***Current*** is **less than** (–)*Quit Current* and then goes within (±)*Quit Current* for 1 second.
2. ***Current*** is **greater than** *Quit Current* and then goes within (±)*Quit Current* for 60 seconds.

After about 30 minutes in relaxation mode, the bq20z40/bq20z45 attempts to take accurate OCV and Qmax updates which are used in the Impedance Track™ algorithm.

Normal Setting: It is critical that the battery voltage be relaxed during OCV readings to get the most accurate results. This current must not be higher than C/20 when attempting to go into relaxation mode; however, it should not be so low as to prevent going into relaxation mode due to noise. This should always be less than *Chg Current Threshold* or *Dsg Current Threshold*.

11.3 State

Qmax Cell 0

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z40/bq20z45 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 1

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z40/bq20z45 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 2

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z40/bq20z45 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 3

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z40/bq20z45 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Pack

This is the maximum capacity of the entire battery pack. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated to the lowest chemical capacity of all the cells (*Qmax Cell 0* – *Qmax Cell 3*) by the bq20z40/bq20z45 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity. It is updated with the capacity of the lowest cell during use. This is because the capacity of the entire battery is only as much as the capacity of the lowest cell. When that cell is empty, it does not matter if any other cells have capacity.

Update Status

There are 2 bits in this register that are important.

- Bit 1 (0x02) indicates that the bq20z40/bq20z45 has learned new Qmax parameters and is accurate.
- Bit 2 (0x04) indicates whether Impedance Track™ algorithm is enabled.

The remaining bits are reserved.
Normal Setting: These bits are user configurable; however, bit 1 is also a status flag that can be set by the bq20z40/bq20z45. These bits should never be modified except when creating a golden image file as explained in the application note *Preparing Optimized Default Flash Constants for specific Battery Types* (see SLUA334.pdf). Bit 1 is updated as needed by the bq20z40/bq20z45 and Bit 2 is set with ***Manufacturers Access*** command 0x0021.

Cell 0 Chg dod at EoC

This value is the calculated depth of discharge (DOD) for cell 0 at the end of charging. It is used for QMax calculations.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

Cell 1 Chg dod at EoC

This value is the calculated depth of discharge (DOD) for cell 1 at the end of charging. It is used for QMax calculations.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

Cell 2 Chg dod at EoC

This value is the calculated depth of discharge (DOD) for cell 2 at the end of charging. It is used for QMax calculations.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

Cell 3 Chg dod at EoC

This value is the calculated depth of discharge (DOD) for cell 3 at the end of charging. It is used for QMax calculations.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

Avg I Last Run

The bq20z40/bq20z45 logs the **Current** averaged from the beginning to the end of each discharge cycle. It stores this average current from the previous discharge cycle in this register.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

Avg P Last Run

The bq20z40/bq20z45 logs the power averaged from the beginning to the end of each discharge cycle. It stores this average power from the previous discharge cycle in this register. To get a correct average power reading the bq20z40/bq20z45 continuously multiplies **Current** times **Voltage** to get power. It then logs this data to derive the average power.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

Delta Voltage

The exact computation of this register is very complex so this description, while not exact, gives the general formula. Delta Voltage is derived as a function average Voltage versus immediate ***Voltage***. The average ***Voltage*** is a localized average over the most recent few seconds. The *Delta Voltage* is the maximum (average ***Voltage*** – ***Voltage***) at any given time. This register is only updated whenever the algorithm computes a value greater than the previous. Every SOC gridpoint (see *Cell0 R_a0*) causes a sort of reset of this computation. To prevent a 0 value in this register and to give more meaning, the reset algorithm uses a percentage of the previous SOC gridpoint *Delta Voltage* to compute a reset value and then starts the process of computing maximum *Delta Voltage* values again.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

Max Avg I Last Run

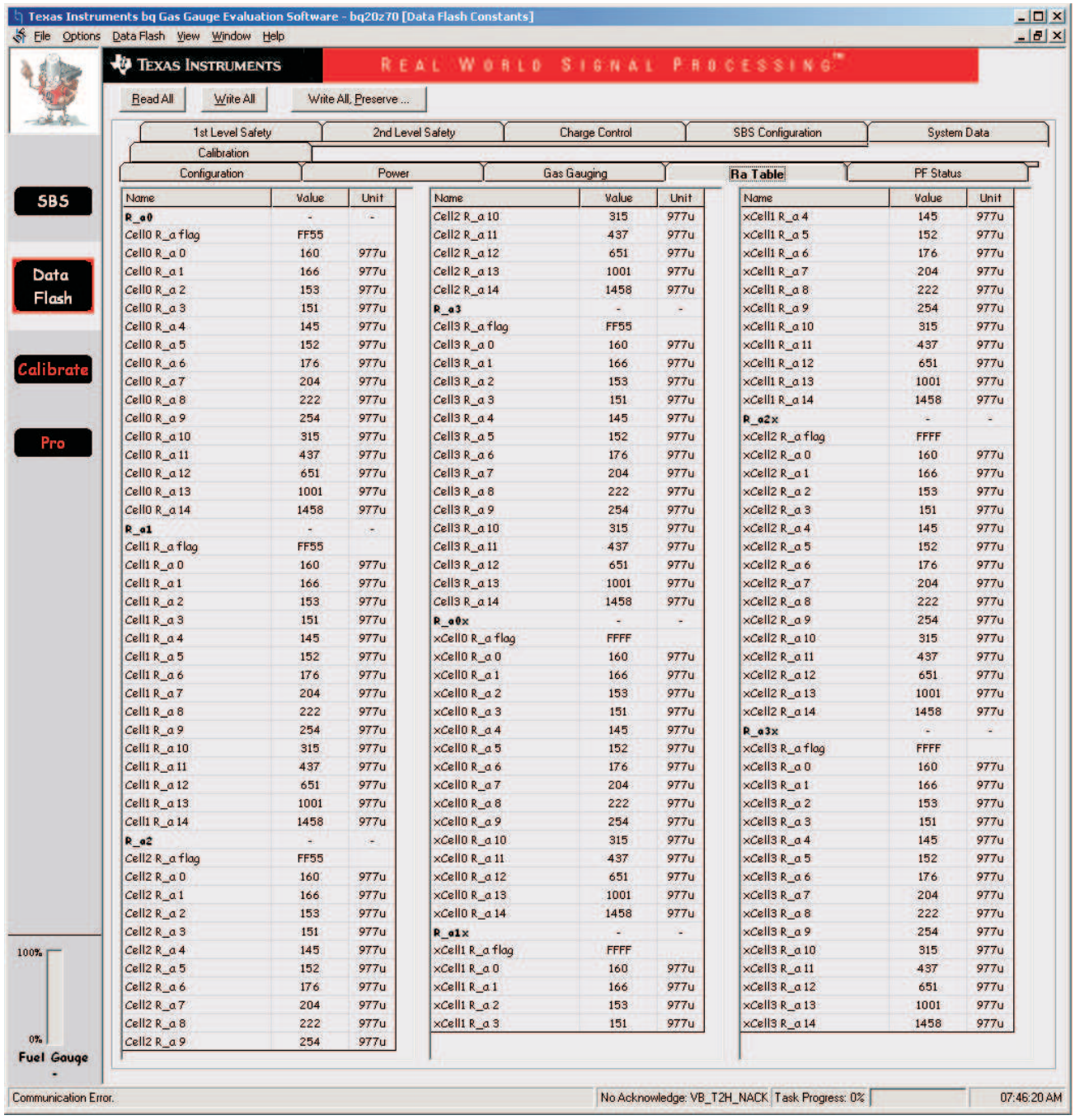
This value is the maximum of the **Average Current** values from the last discharge cycle. It is used by the Impedance Track algorithm as an initial value for rate compensation if Load Select 7 is selected and Load Mode 0 (current) is selected.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

Max Avg P Last Run

This value is the maximum average power from the last discharge cycle. It is used by the Impedance Track algorithm as an initial value for rate compensation if Load Select 7 is selected and Load Mode 1 (power) is selected.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z40/bq20z45 when required.

12 Ra Table

This data is automatically updated during device operation. No user changes should be made except for reading the values from another pre-learned pack for creating “Golden Image Files”. See the application note *Preparation of optimized default flash constants for specific type of battery* (SLUA334). Profiles have format CellN R_a M where N is the cell serial number (from ground up), and M is the number indicating state of charge to which the value corresponds.



Name	Value	Unit
R_a0	-	-
Cell0 R_a flag	FF55	
Cell0 R_a 0	160	977u
Cell0 R_a 1	166	977u
Cell0 R_a 2	153	977u
Cell0 R_a 3	151	977u
Cell0 R_a 4	145	977u
Cell0 R_a 5	152	977u
Cell0 R_a 6	176	977u
Cell0 R_a 7	204	977u
Cell0 R_a 8	222	977u
Cell0 R_a 9	254	977u
Cell0 R_a 10	315	977u
Cell0 R_a 11	437	977u
Cell0 R_a 12	651	977u
Cell0 R_a 13	1001	977u
Cell0 R_a 14	1458	977u
R_a1	-	-
Cell1 R_a flag	FF55	
Cell1 R_a 0	160	977u
Cell1 R_a 1	166	977u
Cell1 R_a 2	153	977u
Cell1 R_a 3	151	977u
Cell1 R_a 4	145	977u
Cell1 R_a 5	152	977u
Cell1 R_a 6	176	977u
Cell1 R_a 7	204	977u
Cell1 R_a 8	222	977u
Cell1 R_a 9	254	977u
Cell1 R_a 10	315	977u
Cell1 R_a 11	437	977u
Cell1 R_a 12	651	977u
Cell1 R_a 13	1001	977u
Cell1 R_a 14	1458	977u
R_a2	-	-
Cell2 R_a flag	FF55	
Cell2 R_a 0	160	977u
Cell2 R_a 1	166	977u
Cell2 R_a 2	153	977u
Cell2 R_a 3	151	977u
Cell2 R_a 4	145	977u
Cell2 R_a 5	152	977u
Cell2 R_a 6	176	977u
Cell2 R_a 7	204	977u
Cell2 R_a 8	222	977u
Cell2 R_a 9	254	977u

Name	Value	Unit
Cell2 R_a 10	315	977u
Cell2 R_a 11	437	977u
Cell2 R_a 12	651	977u
Cell2 R_a 13	1001	977u
Cell2 R_a 14	1458	977u
R_a3	-	-
Cell3 R_a flag	FF55	
Cell3 R_a 0	160	977u
Cell3 R_a 1	166	977u
Cell3 R_a 2	153	977u
Cell3 R_a 3	151	977u
Cell3 R_a 4	145	977u
Cell3 R_a 5	152	977u
Cell3 R_a 6	176	977u
Cell3 R_a 7	204	977u
Cell3 R_a 8	222	977u
Cell3 R_a 9	254	977u
Cell3 R_a 10	315	977u
Cell3 R_a 11	437	977u
Cell3 R_a 12	651	977u
Cell3 R_a 13	1001	977u
Cell3 R_a 14	1458	977u
R_a0x	-	-
xCell0 R_a flag	FFFF	
xCell0 R_a 0	160	977u
xCell0 R_a 1	166	977u
xCell0 R_a 2	153	977u
xCell0 R_a 3	151	977u
xCell0 R_a 4	145	977u
xCell0 R_a 5	152	977u
xCell0 R_a 6	176	977u
xCell0 R_a 7	204	977u
xCell0 R_a 8	222	977u
xCell0 R_a 9	254	977u
xCell0 R_a 10	315	977u
xCell0 R_a 11	437	977u
xCell0 R_a 12	651	977u
xCell0 R_a 13	1001	977u
xCell0 R_a 14	1458	977u
R_a1x	-	-
xCell1 R_a flag	FFFF	
xCell1 R_a 0	160	977u
xCell1 R_a 1	166	977u
xCell1 R_a 2	153	977u
xCell1 R_a 3	151	977u

Name	Value	Unit
xCell1 R_a 4	145	977u
xCell1 R_a 5	152	977u
xCell1 R_a 6	176	977u
xCell1 R_a 7	204	977u
xCell1 R_a 8	222	977u
xCell1 R_a 9	254	977u
xCell1 R_a 10	315	977u
xCell1 R_a 11	437	977u
xCell1 R_a 12	651	977u
xCell1 R_a 13	1001	977u
xCell1 R_a 14	1458	977u
R_a2x	-	-
xCell2 R_a flag	FFFF	
xCell2 R_a 0	160	977u
xCell2 R_a 1	166	977u
xCell2 R_a 2	153	977u
xCell2 R_a 3	151	977u
xCell2 R_a 4	145	977u
xCell2 R_a 5	152	977u
xCell2 R_a 6	176	977u
xCell2 R_a 7	204	977u
xCell2 R_a 8	222	977u
xCell2 R_a 9	254	977u
xCell2 R_a 10	315	977u
xCell2 R_a 11	437	977u
xCell2 R_a 12	651	977u
xCell2 R_a 13	1001	977u
xCell2 R_a 14	1458	977u
R_a3x	-	-
xCell3 R_a flag	FFFF	
xCell3 R_a 0	160	977u
xCell3 R_a 1	166	977u
xCell3 R_a 2	153	977u
xCell3 R_a 3	151	977u
xCell3 R_a 4	145	977u
xCell3 R_a 5	152	977u
xCell3 R_a 6	176	977u
xCell3 R_a 7	204	977u
xCell3 R_a 8	222	977u
xCell3 R_a 9	254	977u
xCell3 R_a 10	315	977u
xCell3 R_a 11	437	977u
xCell3 R_a 12	651	977u
xCell3 R_a 13	1001	977u
xCell3 R_a 14	1458	977u

Cell0 R_a flag,
Cell1 R_a flag,
Cell2 R_a flag,
Cell3 R_a flag,
xCell0 R_a flag,
xCell1 R_a flag,
xCell2 R_a flag,
xCell3 R_a flag

Each subclass (R_a0-R_a3 and R_a0x-R_a3x) in the Ra Table class is a separate profile of resistance values normalized at 0 degrees for each of the cells in a design (cells 0–3) There are 2 profiles for each cell. They are denoted by the x or absence of the x at the end of the subclass Title:
R_a0 or **R_a0x** for cell 0
R_a1 or **R_a1x** for cell 1
R_a2 or **R_a2x** for cell 2
R_a3 or **R_a3x** for cell 3
The purpose for 2 profiles for each series cell is to ensure that at any given time there is at least one profile is enabled and being used while attempts can be made to update the alternate profile without interference. Having 2 profiles also helps reduce stress on the Flash Memory. At the beginning of each of the 8 subclasses (profiles) is a flag called *CellM R_a flag* or *xCellM R_a flag* where “M” is the cell number (0-3). This flag is a status flag indicates the validity of the table data associated with this flag and whether this particular table is enabled/disabled. There are 2 bytes in each flag:

1. The LSB (least significant byte) indicates whether the table is currently enabled or disabled. It has the following options:
   (a) 0x00 : Means the table has had a resistance update in the past; however, it is not the currently enabled table for this cell. (the alternate table for the indicated cell must be enabled at this time)
   (b) 0xff: This means that the values in this table are default values. This table resistance values have never been updated, and this table is not the currently enabled table for this cell. (the alternate table for the indicated cell must be enabled at this time)
   (c) 0x55: This means that this table is enabled for the indicated cell (the alternate table must be disabled at this time.)
2. The MSB (Most significant byte) indicates that status of the data in this particular table. The possible values for this byte are:
   (a) 0x00: The data associated with this flag has had a resistance update and the *QMax Pack* has been updated
   (b) 0x05: The resistance data associated with this flag has been updated and the pack is no longer discharging (this is prior to a *Qmax Pack* update).
   (c) 0x55: The resistance data associated with this flag has been updated and the pack is still discharging (Qmax update attempt not possible until discharging stops).
   (d) 0xff: The resistance data associated with this flag is all default data.

This data is used by the bq20z40/bq20z45 to determine which tables need updating and which tables are being used for the Impedance Track™ algorithm.
Normal Setting: This data is used by the bq20z40/bq20z45 Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This description of the *xCellM R_a flags* are intended for information purposes only. It is not intended to give a detailed functional description for the bq20z40/bq20z45 resistance algorithms.

Cell0 R_a0 – Cell0 R_a14,
xCell0 R_a0 – xCell0 R_a14,
Cell1 R_a0 – Cell1 R_a14,
xCell1 R_a0 – xCell1 R_a14,
Cell2 R_a0 – Cell2 R_a14,
xCell2 R_a0 – xCell2 R_a14,
Cell3 R_a0 – Cell3 R_a14,
xCell3 R_a0 – xCell3 R_a14,

There are 15 values for each R_a subclass in the **Ra Table** class. Each of these values represent a resistance value normalized at 0°C for the associated *Qmax Pack* based SOC gridpoint as found by the following rules:

For *CellN R_aM* where:

1. if 0 ≤ M ≤ 8: The data is the resistance normalized at 0° for: SOC = 100% – (M × 10%)
2. if 9 ≤ M ≤ 14: The data is the resistance normalized at 0 degrees for: SOC = 100% – [80% + (M – 8) × 3.3%]

This gives a profile of resistance throughout the entire SOC profile of the battery cells concentrating more on the values closer to 0%.
Normal Setting: SOC as stated in this description is based on *Qmax Pack*. It is not derived as a function of RSOC or ASOC. These resistance profiles are used by the bq20z40/bq20z45 for the Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This resistance profile description is for information purposes only. It is not intended to give a detailed functional description for the bq20z40/bq20z45 resistance algorithms. It is important to note that this data is in units of milliohms and is normalized to 0°C. Note this data throughout the application development cycle:

1. Watch for negative values in the **Ra Table** class. There should never be negative numbers in profiles anywhere in this class.
2. Watch for smooth consistent transitions from one profile gridpoint value to the next throughout each profile. As the bq20z40/bq20z45 does resistance profile updates these values should be roughly consistent from one learned update to another without huge jumps in consecutive gridpoints.

Revision History

Changes from A Revision (April 2012) to B Revision	Page
• Changed list item 1,0 From: Greater value of TS! and TS2 external inputs are used to generate ***Temperature*** To: Only Temperature sensor TS2 is used to generate ***Temperature***.	50

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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