UCC28070 Implement Bridgeless Power Factor Correction (PFC) Pre-Regulator Design

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ABSTRACT

Bridgeless power factor correction (PFC) topology is attracting attention as a means of satisfying the new high-efficiency requirements. This application report reviews the UCC28070 and its design considerations for bridgeless PFC. It present a bridgeless solution that is relatively easy to implement in that it does not require any additional circuitry for current sensing and that the operation remains very similar to that of a conventional concinuous condustion mode (CCM) PFC.

1 Bridgeless PFC

High-power efficiency is an important concern in the design of a switching mode power supply, especially for energy saving and environmental protection. For instance, the Energy Efficiency Alliance's (NEEA's) 80 PLUS initiative (and moreover its Bronze, Silver and Gold derivatives) force ATX desktop PC and server power designers to create innovative solutiond to improve overall efficiency. The PFC pre-regulator stage can easily consume 5% to 8% of the output power at low line and full load. Zero voltage threshold (ZVT) PFC or Interleaved PFC, for example, are proposed to get higher efficiency and better performance. Meanwhile, bridgeless PFC attracts more interest for it's ability to reduce conduction loss without the input rectifier bridge.

Figure 1 shows the schematic of a classical solution for a bridgeless PFC. There are two switching operating cells at each half-line cycle as shown in Figure 2. Each operating cell consists of a power MOSFET and a diode. Q1 and D1 operate in Boost switching mode for the half-line cycle when the terminal “L” line is high, and the body diode of Q2 is conducted as current return path. On the other half-line cycle, Q2 and D2 operate as Boost switching mode when the terminal “N” line is high, and the body diode of Q1 is conducted as current return path.

Compared to a conventional Boost PFC topology, the losses due to the bridge rectifier are eliminated, but the body diode conduction of the inactive MOSFET is conveyed to coil current. Overall there is only one diode conduction loss for a bridgeless PFC compared to conduction loss from two diodes in a conventional Boost PFC, which can improve efficiency to eliminate the voltage drop of one diode in the line-current path. Consider, for example, a 270-W PFC after MathCAD calculation for power loss. iI a conventional PFC, the bridge rectifier loss is 5.5 W, the power MOSFET loss is 2.26 W, and power efficiency is around 95.3%. In a bridgeless PFC, there is no bridge rectifier loss, only power MOSFET loss of 5.18 W, so overall efficiency is 96.1% with a efficiency improvement between 1% adn 2% after the implementation of the bridgeless PFC.

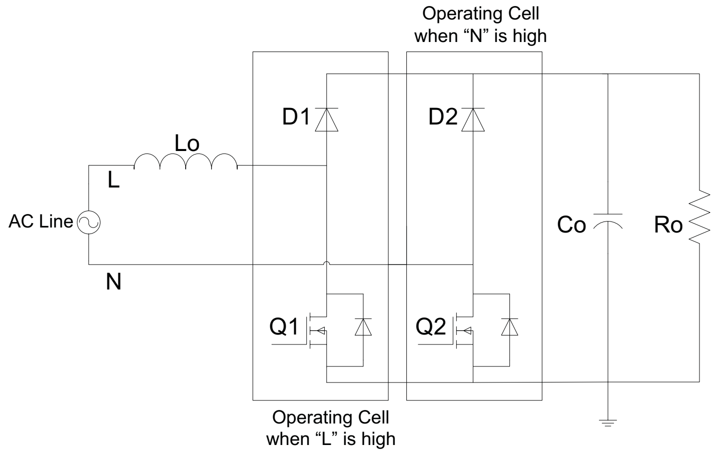

Figure 1. Classical Bridgeless PFC Solution

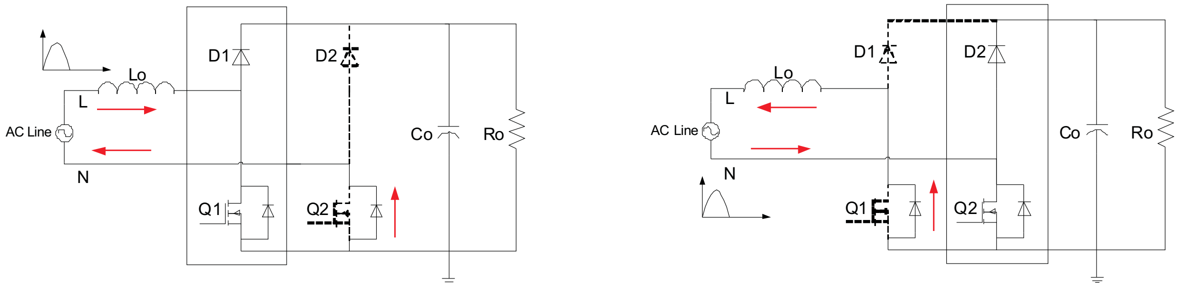

Figure 2. Bridgeless PFC Operation Mode with Different Half-Line Cycle

Despite many advantages of a bridgeless PFC, there are some obstacles that need to overcome.

- Because the line is floating compared to the PFC stage ground, simple circuitry cannot sense input voltage. Normally a low-frequency transformer or optical coupler is used to perform input voltage sensing.
- For ca onventional PFC, the current sense is easy to monitor by simply inserting a shunt sensing resistor at the return path of the inductor current. However, for a bridgeless PFC, current path does not share the same ground at each half-line cycle. A sensing-power MOSFET and diode current are needed, which makes the bridgeless PFC's current sensing complicated and difficult to monitor.
- EMI noise is another issue. For a bridgeless PFC, the output voltage ground is always floating relative to the AC line input. Thus, all parasitic capacitance including MOSFET drain to earth and the output terminals to the earth ground contribute to common mode noise. This large dv/dt at each phase's switching node leads to an increased common mode noise that is difficult to filter. At the same time, the switching node MOSFET Q2 and diode D2 are directly connected to input line terminal, which leads to high dv/dt common mode noise.

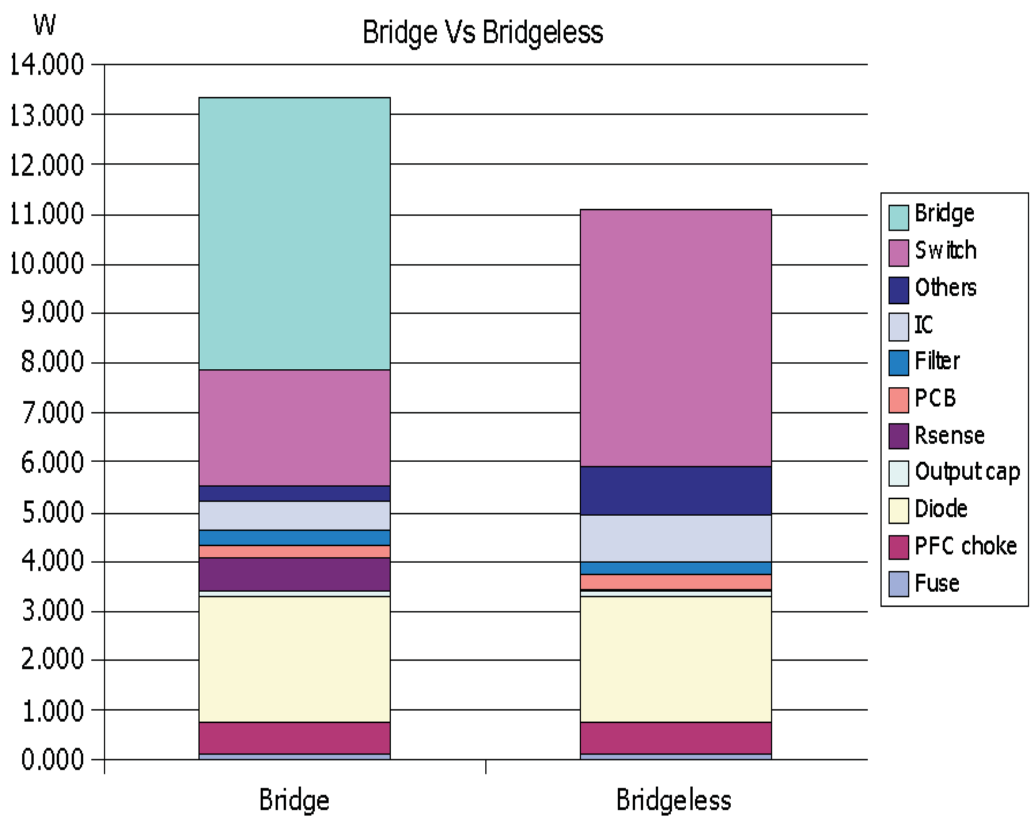

Figure 3. Power Loss Comparison Between Conventional PFC and Bridgeless PFC

2 Simplified Semi-Bridgeless PFC

In order to overcome the previously mentioned drawbacks of classic bridgeless PFC, some improved methods are proposed. Figure 4 show gives a useful semi-bridgeless circuit which is proposed by Step 3. In this topology, the PFC inductor is split into two smaller ones and connected to input line terminal to each switching node. By using two split inductors, direct application of the switching node high dv/dt to the input terminals is removed and thus, the line potentials can be more stable with respect to the board ground. Also, two diodes (Da and Db) link the PFC output ground to the input line, and Da and Db offer the return path, which makes the input line voltage no longer floating but rather traditionally referenced to ground. So the input voltage for the PFC stage is a rectified sinusoid referenced to ground, and the low-frequency transformer or optical coupler is no longer needed to sense the input voltage. A simple resistor divider can be placed in order to sense the input voltage. Moreover, adding the diodes Da and Db can avoid inducing high common noise by connecting the input line and output power ground through diodes.

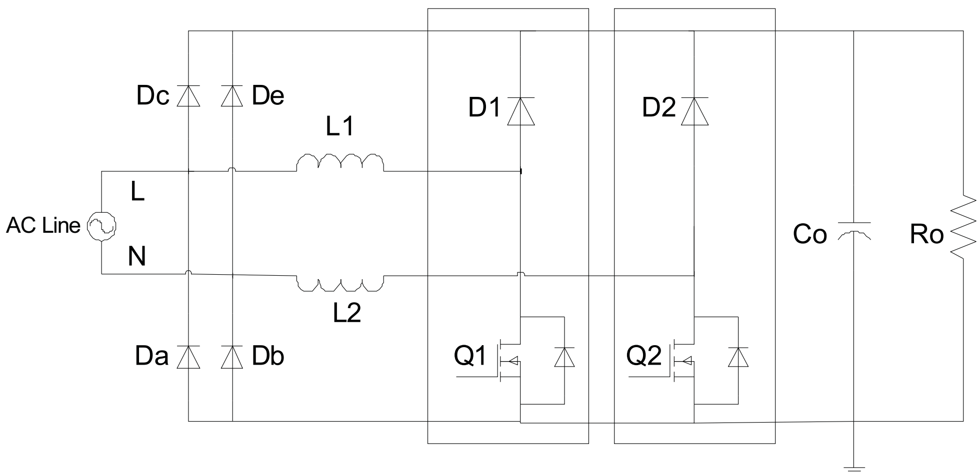

Figure 4. Semi-Bridgeless PFC

It also requires two inrush diodes (Dc and De) to peak charge the common PFC boost capacitor C_O during the initial start up, thereby avoiding the inrush current going through MOSFET during this start-up period. However, after the capacitor has been peak charged, and the converter is operating, the PFC converter power does not conduct through Dc and De. That is different from the traditional Boost PFC, where two of the bridge rectifier diodes are always conducting. As for bridgeless PFC operation analysis, the designer can ignore the effects of Dc and De.

However, the current sensing issue remains to be revolved. As shownin the semi-bridgeless PFC diagram in Figure 4, the current returns not only through Da or Db, but also through the body diode of inactive MOSFET that is not in switching mode. As shown in Figure 5, when “L” line is high with input voltage sinusoid positive (the same results when “N” line is high with input voltage sinusoid negative), unfortunately, the majority portion of current flows through the body diode of inactive MOSFET Q2 whenever MOSFET Q1 turns on or off. Only a small portion of that current flows through the diode Db.

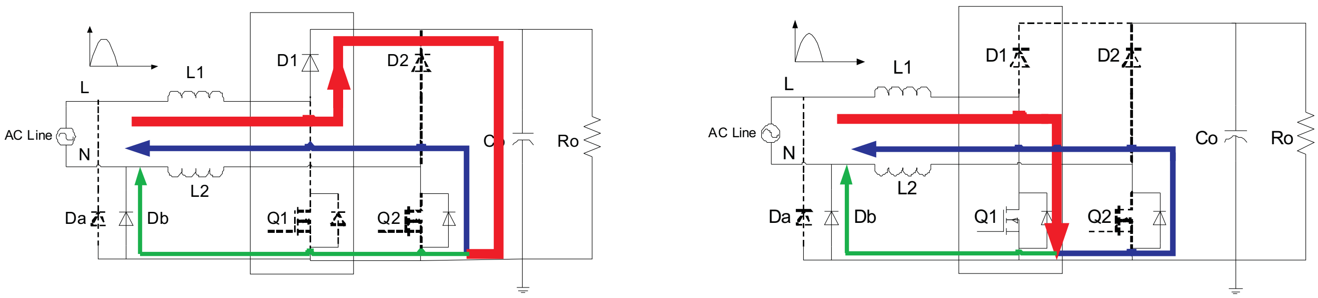

Figure 5. (a) MOSFET Q1 Turns Off and D1 is Conducted (b) MOSFET Q1 Turns On and D1 is Reversed Current Path when “L” Line Voltage is High

Figure 6 shows the PFC inductor current waveform at 90 V_{AC} input and 0.5 A/390 V_{DC} output. There is a large portion of current flowing through the body diode of MOSFET and PFC inductor when the corresponding operating cell is in inactive mode. This is because PFC inductor coil has low impedance at the low line 50 HZ/60 HZ frequency, so it can be regarded as two diodes (Db and body diode of Q2) in parallel to share the return current. If the body diode voltage drop is less than that of Diode Db, a large portion of the current flows to body diode. Although the MOSFET’s body diode conduction has little impact on efficiency Step 1, it becomes difficult to sense the current in a bridgeless PFC. Inserting a shunt sensing resistor on the return path to monitor the current does not work.

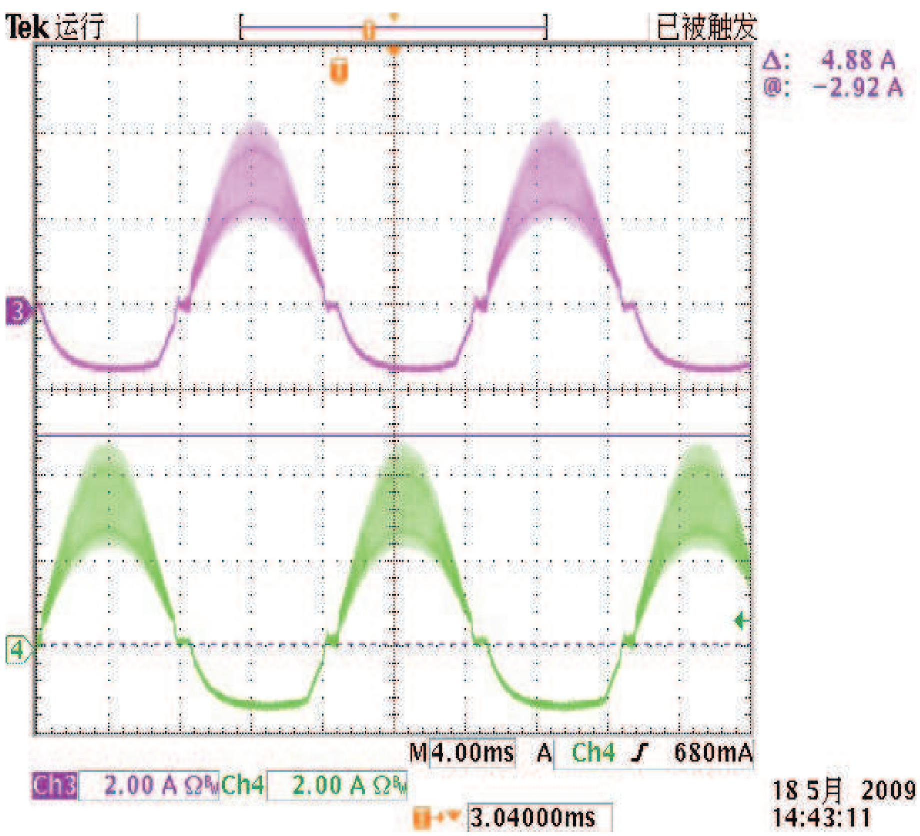

Figure 6. Inductor Current Waveform at 90 V_{AC} Input and 0.5 A/390 V_{DC} Output

There have been some methods described in other papers, such as using four current transformers to monitor current of MOSEFT Q1 and Q2 and output to capacitor with load; or using differential mode amplifier to sense the current in the front of PFC inductor Step 1. In Figure 7 showing a current sensing circuit for this bridgeless PFC, it is necessary to sense the chopping current of the MOSFET and diode and to sum the signals to be applied to resistor R^S. But this method makes the control circuit more complicated and needs a reset network to demagnetize the current sensing transformer. The designer can not easily achieve the simplified bridgeless PFC using the conventional average CCM PFC controller. The designer needs to find an innovative method to sense the current of the modified bridgeless PFC. The TI UCC28070 can be used for the bridgeless PFC topology without needing to modify any control and sensing circuit.

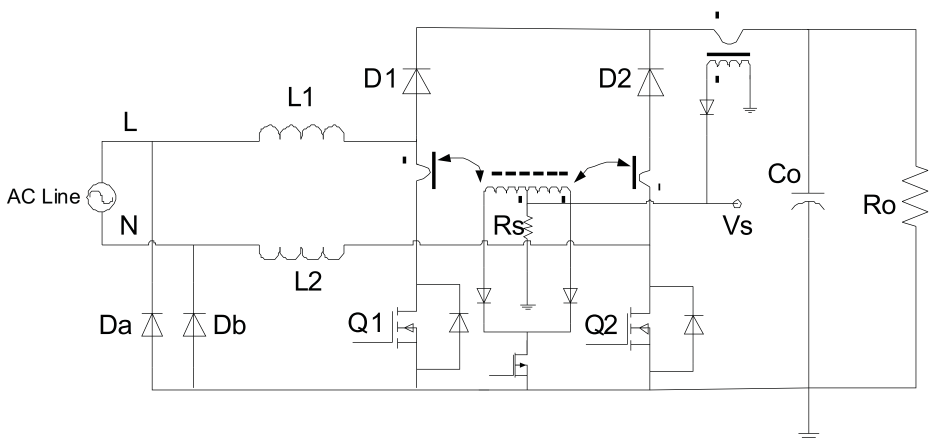

Figure 7. Current Sensing Circuit for Modified Bridgeless PFC

3 Why Use the UCC28070?

The TI UCC28070 is an advanced power factor correction (PFC) device that integrates two pulse-width modulations operating 180° out-of-phase. This device is a good solution for the interleaved average continuous current Mode (CCM) PFC, which generates substantial reduction tp the input and output ripple current. Thus the conduction EMI filtering becomes easier and less expensive. This device is suitable for telecom power rectifiers and high-efficiency AC/DC power supply.

In addition to interleaved CCM PFC control, the UCC28070 is also good candidate for a semi-bridgeless PFC using its unique innovations including current synthesis and quantized voltage feed-forward technique to simplify bridgeless PFC design. Figure 8 is the simplified application diagram for semi-bridgeless PFC using UCC28070, where Dc and De are added only to conduct inrush current during start up period.

As discussed previously in theis paper, current sensing is a critical issue for bridgeless PFC; designers need to add circuits to monitor current. However, UCC28070's current synthesizer can make the sensing circuit simple. This current synthesizer circuitry monitors the MOSFET instantaneous current through a combination of on-time sampling and off-time down-slope emulation. As shown in Figure 8, during the on-time of the GDA or GDB outputs, the inductor current is recoded at CSA and CSB pins respectively via the current transformer network in each output phase. Meanwhile, the continuous monitoring of the input and output voltage via the VINAC and VSENSE pins permits the UCC28070 to internally recreate the inductor current down-slope during each output's respective off-time. Through the selection of the R_{SYNTH} resistor (RSYN), based on the equation below, the internal response may be adjusted to accommodate the wide range of inductances expected across the the application.

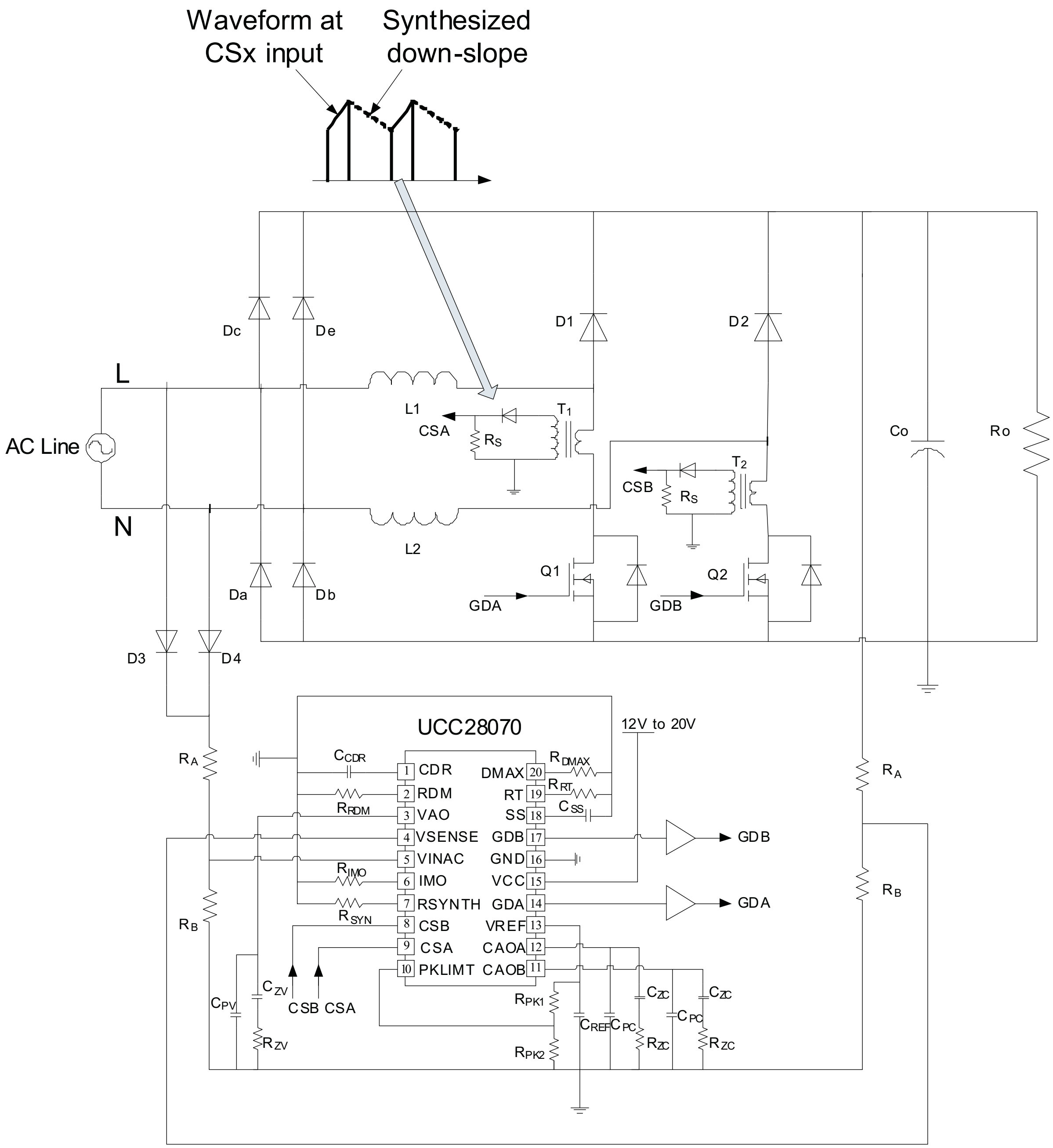

Figure 8. Simplified Application Diagram for UCC28070 Bridgeless PFC

$$R_{SYN}(k\Omega) = \frac{(10 \times N_{CT} \times L_B \times k_R)}{R_S} \quad (1)$$

Where

- L_B = Nominal Zero-Bias Boost Inductance (µH)
- R_S = Sense Resistor (Ω)
- N_{CT} = Current Sense Transformer turns ratio
- $K_R = R_B/(R_A+R_B)$ = the resistor-divider attenuation at the VSENSE and VINAC pins.

A major advantage of the UCC28070 in a bridgeless PFC design is the current synthesis function, which internally recreates the inductor down-slope during the switching period off-time. This eliminates the other need for the current transformer or shunt resistor of bridgeless PFC. A single resistor programming the synthesizer down slope can easily achieve current sensing for bridgeless average CCM PFC without adding any external components. For current transformer, volt-second balancing is very important to avoid its saturation; a possible reset network is needed. Also, to improve noise immunity a current sense offset circuit is added. Refer to UCC28070 datasheet on reset network and offset circuit design in detail.

In addition to current synthesis function, UCC28070 creates unique multiplier architecture to quantize VRMS feed-forward (QVFF) circuitry, which eliminates the requirement for external filtering of the VINAC signal and subsequent slow response to transient line variations. A unique circuit algorithm detects the transition of the peak of VVINAC through seven thresholds and generates an equivalent VFF level centered within the eight QVFF range. The eight QVFF levels are spaced to accommodate the full "universal" line range of 86V~265VRMS.

In summary, UCC28070 can simplify the design of bridgeless PFC because of the following benefits:

- Current synthesizer simplifies the current sensing circuit without adding any additional components, thus average CCM bridgeless PFC can be achieved using simple control method.
- Linear multiplier architecture eliminates the external filtering of the VINAC and slow transient response during line variation. The input sensing voltage circuit is also simplified.
- Frequency dithering achieve a reduction in conducted-EMI noise beyond the capability of the line filter alone. By trimming RRDM and CCDR, we can set the required dither magnitude and dither rate to reduce the EMI noise, which is also critical for bridgeless PFC.
- UCC28070 can control interleaved PFC or bridgeless PFC without any additional modification.

4 Experimental Results

This application design has modified the TI 300-W UCC28070 Interleaved PFC EVM (SLUU312) to a 200-W bridgeless PFC for comparison. This comparison is based on the same board without changing any other parameter or component. Input voltage RMS is between 85 V_{AC} and 265 V_{AC}, output voltage is 390 V_{DC}, line frequency between 47 HZ and 63 HZ and the switching operation frequency is 200 kHZ.

For component selection on the bridgeless PFC, the designer can refer to the TI 300-W Interleaved Application Report (SLUA479) Step 6, however, the designer can allow each inductor to have more inductor ripple current than a bridgeless PFC than is described in that paper, because of the inductor ripple current cancellation inhenent with interleaved PFC. But for bridgeless PFC, there is no ripple cancellation ratio K(D) during the calculation of RMS current and inductance. Assuming the maximum input current was set to 30% of the peak nominal input current at low line, the RMS current and inductance calculate as shown in Equation 3.

$$D_{PLL} = \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}}{V_{OUT}} = \frac{390 - 85\sqrt{2}}{390} \approx 0.69 \tag{2}$$

Input RMS current is calculate in Equation 3 and inductor ripple current is calculate in Equation 4.

$$I_{IN\_RMS} = \frac{P_{OUT}}{V_{IN\_MIN} \times \eta} = \frac{200W}{85V \times 0.9} = 2.6A \tag{3}$$

$$\Delta IL = \frac{P_{OUT} \times \sqrt{2} \times 0.3}{V_{IN\_MIN} \times \eta} = \frac{200W \times \sqrt{2} \times 0.3}{85V \times 0.9} \approx 1.1A \tag{4}$$

As shown in Figure 5, the minimim inductance at low line can be calculated as shown in Equation 5.

$$L1 = L2 \frac{V_{IN\_MIN} \times \sqrt{2} \times D_{PLL}}{\Delta IL \times fs} = \frac{85\,V \times \sqrt{2} \times 0.69}{1.1\,A \times 200\,kHZ} » 370\ \mu H \tag{5}$$

The total inductor RMS current is the Equation 6.

$$I_{L1\_RMS} = I_{L2\_RMS} = \sqrt{\left(\frac{P_{OUT}}{V_{IN\_MIN} \times \eta}\right)^2 + \left(\sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{\frac{V_{IN\_MIN}\sqrt{2}\sin(\theta)}{L1 \times fs} \times \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}\sin(\theta)}{V_{OUT}}}{\sqrt{12}}}\right)^2} \approx 2.7A25\,A \times 0.2 = 5\,A \tag{6}$$

For the other calculations regarding the MOSFETs and diodes, the designer can refer to Step 6. Please note that for a bridgeless PFC, the power ratings are not half of P_{OUT} compared with interleaved PFC when calculating the current values.

Figure 9 gives the efficiency comparison between conventional PFC and bridgeless PFC at 110 V_{AC} and 220 V_{AC}. Generally, the efficiency improvement of a bridgeless PFC is approximately between 1% and 2% to conventional bridgeless PFC. Figure 11 through Figure 16 show the testing waveforms at 90 V_{AC}, 110 V_{AC} and 265 V_{AC}, illustrating how the UCC28070 can achieve bridgeless PFC with easy current sensing and no additional complicated circuitry.

5 Conclusion

THe UCC28070 with its current synthesis and quantized voltage feed-forward is good candidate for bridgeless PFC. This application report uses TI 300W UCC28070 Interleaved PFC demo board to modify to a simplified semi-bridgeless PFC. The experiment concludes that the UCC28070 can be used to design a bridgeless PFC with higher efficiency and high power factor without any additional circuitry.

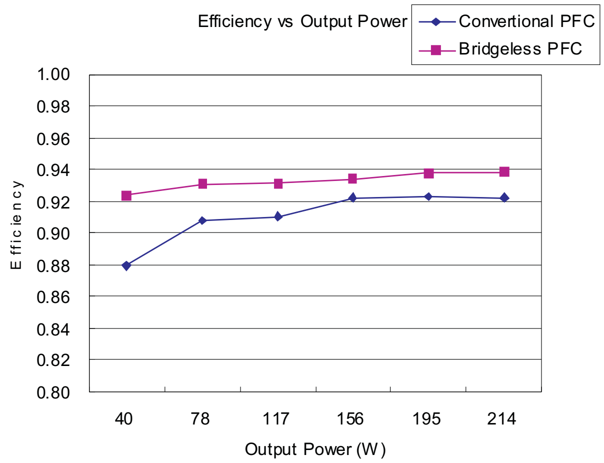

Figure 9. Efficiency at V_{IN}=110 V_{AC}

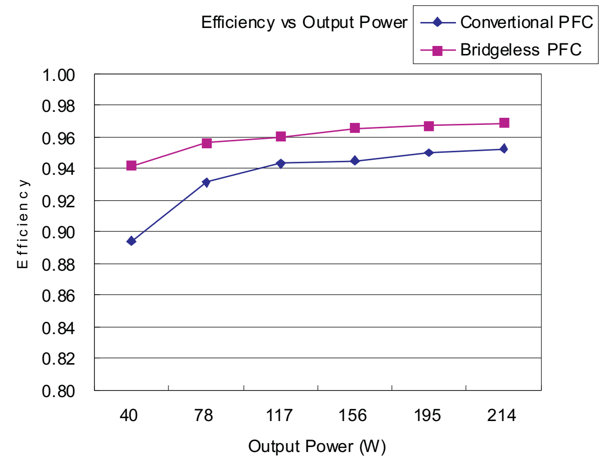

Figure 10. Efficiency at V_{IN} = 220 V_{AC}

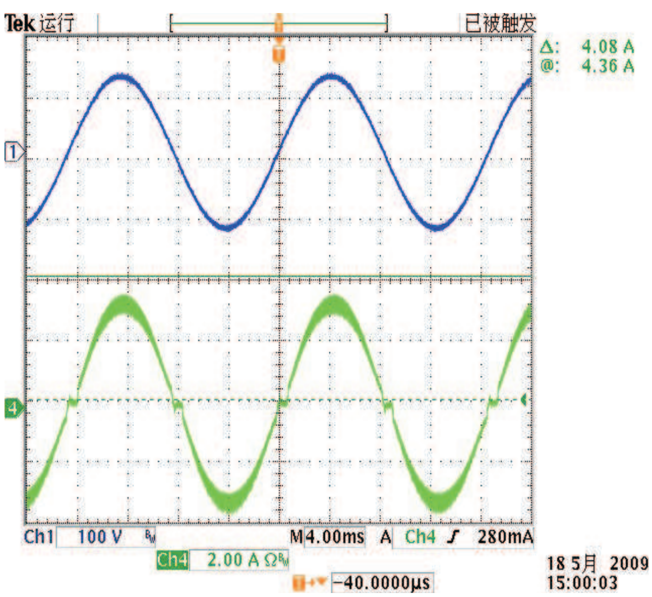

Figure 11. Input Voltage V_{IN} = 90 V_{AC} and I_{OUT}= 0.5 A

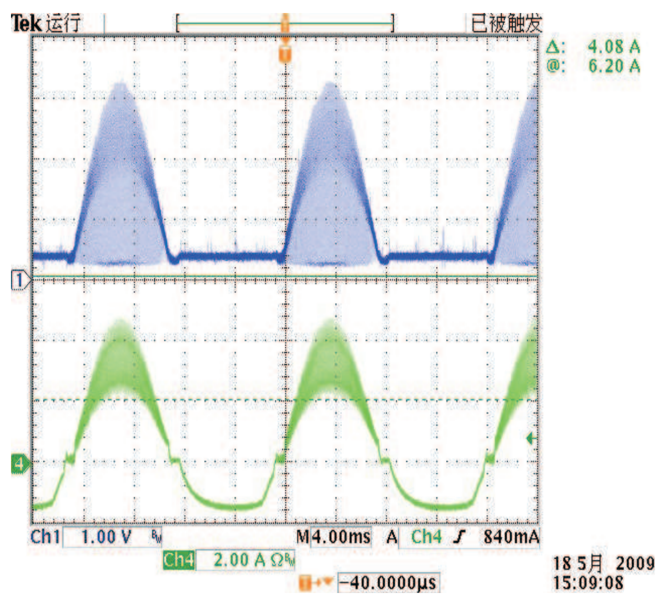

Figure 12. Current Sensing CSA Voltage and PFC Inductor Current at V_{IN} = 90 V_{AC} and I_{OUT}= 0.5 A

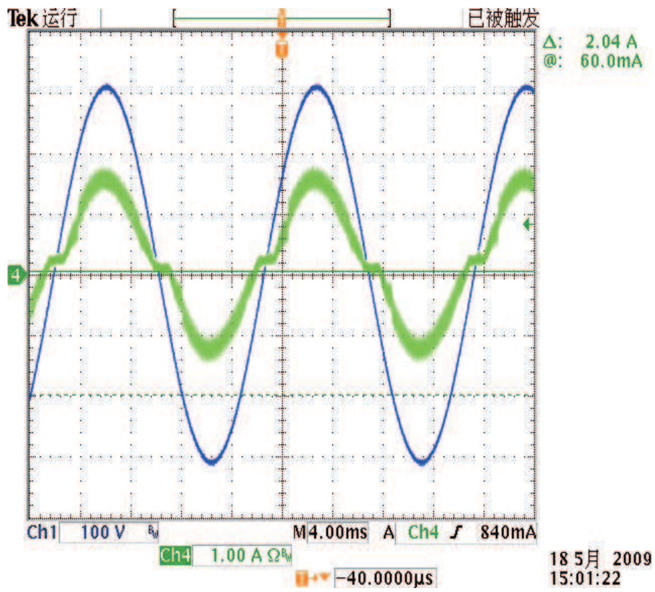

Figure 13. Input Voltage V_{IN} and Input Current Waveform at 220 V_{AC} Input and I_{OUT}= 0.5 A

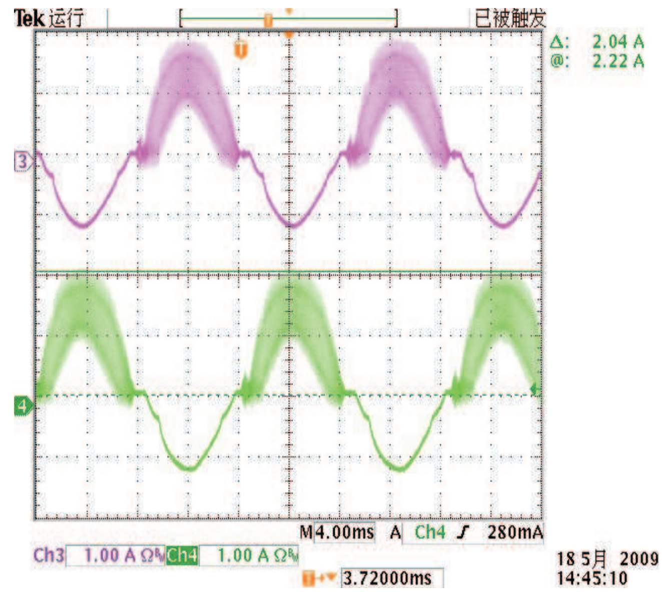

Figure 14. PFC Inductor Current on Each Operating Cell at V_{IN} = 220 V_{AC} and I_{OUT}= 0.5 A

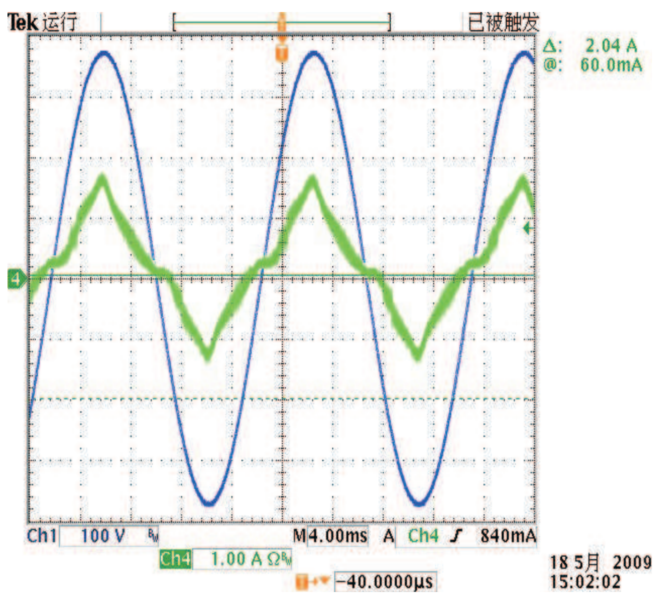

Figure 15. Input voltage V_{IN} and Input Current waveform at 265 V_{AC} Input and I_{OUT}= 0.5 A

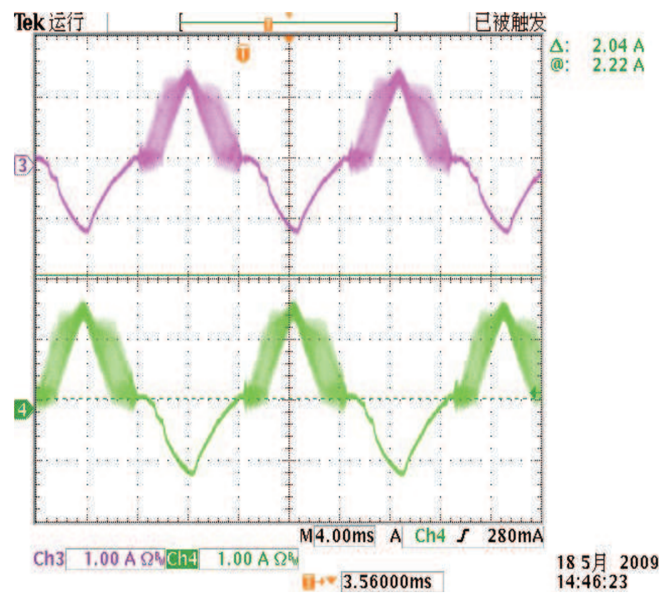

Figure 16. PFC Inductor Current on Each Operating Cell at 265 V_{AC} Inputand I_{OUT}= 0.5 A

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