

A High-Efficiency Synchronous Rectifier Flyback for High-Density AC/DC Adapter

Application Report



Literature Number: SLUA604

August 2011

A High Efficiency Synchronous Rectifier Flyback for High Density AC/DC Adapter

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ABSTRACT

With the fast development of the tablet PC, the increasing load demand requires the adapter to have high power density, high efficiency, and low profile. This application note presents a high efficiency Flyback converter with output synchronous rectification, which can achieve high efficiency within a wide load range to meet the high density requirements. By using Texas Instrument’s UCC28610 green mode controller and the UCC24610 Synchronous Rectifier (SR) controller, a 17W SR Flyback converter reference design, PMP4305, with 5.6V output voltage demonstration board is designed with experimental verification.

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1 Introduction

In the recent consumer market trend, the tablet Personal Computer (tablet PC) is a hot topic because of its ease of use and wireless network connectivity to support multiple functions for end users. Because of these additional functions, such as wireless for Internet and local network connection or other external accessories, and desired fast Li-battery charging, the tablet PC demands much higher power than before. So the key design challenge for the power supply adaptor of a tablet PC is to achieve higher power rating with the same small form factor, which means the trends for tablet PC power supply adapter are higher density and higher efficiency.

In the small wattage power supplies, the Flyback converter is widely used because of its simplicity and low cost. However, due to the high peak and RMS currents, the MOSFET and output rectifier diode in the Flyback have high conduction losses, which results in its relatively low efficiency. Through power loss analysis on Flyback converters, there are two key power loss factors: the first one is main MOSFET switching loss on the primary side during switch turn-on when the MOSFET has a high drain to source voltage, V_{ds} . And the second is the conduction loss of the secondary side output diode. In order to reduce both switching losses on the primary side and conduction losses on the secondary side, there are some methods of improvement, such as implementing valley switching on the primary side with frequency variation to optimize wide load range efficiency, and using a synchronous rectifier on the secondary side. This application note presents a high efficiency Flyback with variable frequency switching and secondary side synchronous rectification to improve the overall efficiency for high density adapters. Texas Instruments' UCC28610 is used on the primary side and is a green mode Flyback controller with variable switching frequency in which every switching cycle immediately follows at least one zero crossing detected by the ZCD pin. This method of switching results in ensuring that the converter is always in discontinuous current mode and that switching actually takes place at or near the lowest V_{ds} voltage as it will occur on the downslope of the resonant ring. The UCC24610 is a synchronous controller which ensures the output SR-MOSFET operates as a near-ideal diode to reduce the conduction loss without any current reversing issue. Figure 1 shows the simplified block diagram for this SR-Flyback converter using the UCC28610 and UCC24610.

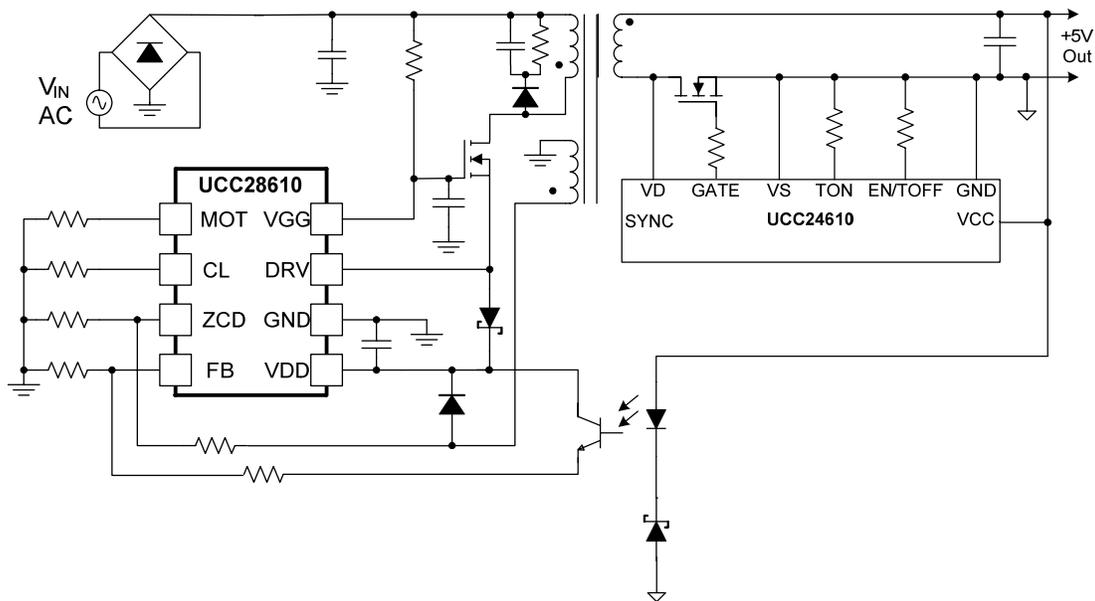


Figure 1. Simplified SR-Flyback schematic with UCC28610 & UCC24610

2 Synchronous Rectifier Flyback Topology

The use of a low-voltage-low-R_{ds(on)} MOSFET has become attractive to replace the Schottky diode rectifiers in high current applications because it offers several system advantages such as dramatic reduction in conduction losses and better thermal management of the entire system by reducing the cost of the heat sink and PCB space. The implementation of SR control in the Flyback topology ranges from conventional self-driven (secondary winding voltage detection) to a more complex current-driven solution, or a combination of both to improve the existing SR-Flyback topology. Self-driven is a simple solution, but the turn off delay of the SR may cause overshoot current if the turn-off signal is issued after the secondary current commutation period. Those conventional ideas become quite complicated with additional discrete devices and have made the cost and part count issues even worse. The technique of drain-to-source voltage sensing has been proposed in recent years. The UCC24610 is an ideal device for an SR-Flyback using direct drain-to-source voltage sensing, and is optimized for output voltages from 4.5V to 5.5V, although it is suitable for use with lower and higher output voltages as well, with some circuit modifications.

Figure 2 shows the ideal operating waveforms of the UCC24610 on the secondary side synchronous rectifier. When the voltage drop across the SR-MOSFET (V_{ds}) exceeds $V_{TH(on)}$, the gate voltage of SR-MOSFET will be driven high with turn-on rise time. Once the SR-MOSFET is turned on, when the voltage drop across SR-MOSFET (V_{ds}) rises above $V_{TH(off)}$, the gate voltage of the SR-MOSFET will be driven low with turn-off falling time. Because no timing signal needs to be transferred from the primary side and no timing components are needed on the secondary side, the solution is very simple to implement using the SR-MOSFET drain-to-source voltage sensing.

According to Figure 2, it is easy to conclude that the voltage drop when using an SR-MOSFET is far less than the conduction drop that would occur with a Schottky diode, which results in reduced conduction losses and thus overall efficiency improvement in an SR-MOSFET application. In this 17W adapter reference design, we compare the 40V/49A MOSFET BSC093N04LSG with the 40CTQ045 Schottky diode in order to estimate the efficiency improvement by using SR-MOSFET on the secondary side.

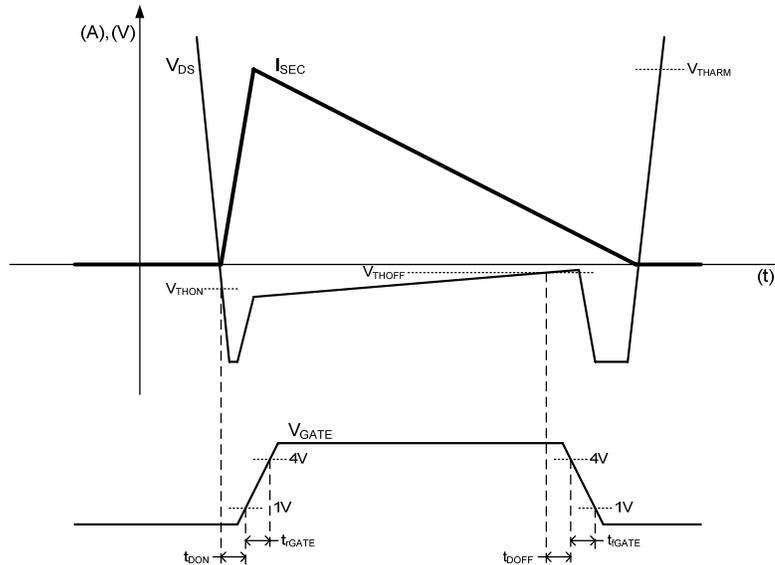


Figure 2. SR-Flyback operating waveforms on the secondary side

The total losses of the SR-MOSFET can be divided into four loss factors: conduction loss driver loss, body diode loss, and switching loss during turn on. The equation below shows the power loss of the SR-MOSFET.

$$P_{mos} = (I_{rms}^2 \times R_{dson}) + (Q_g \times V_{cc} \times f_s) + (I_d \times V_f \times t_d \times f_s) + \left(\frac{1}{2} \times I_{spk} \times \left(\frac{V_{in}}{n} + V_{ol} \right) \times t_r \times f_s \right)$$

According to the BSC093N04LSG MOSFET's datasheet, we can get $R_{dson}=10m\Omega$ at 100 deg C, $Q_g=24nC$; and assuming the body diode conduction time of 500ns and the forward voltage drop, V_f , is equal to 1.1V. The SR-MOSFET power loss calculates to:

$$P_{mos} = 0.454W .$$

According to the datasheet of the 40CTQ150, the diode losses include conduction loss and reversed power loss. In this case, only the conduction loss is considered because the inverse power loss for a Schottky diode is relatively low. So the diode rectifier loss can be calculated as shown in the below equation:

$$P_{diode} = I_{fav} \times V_f = 3A \times 0.42V = 1.26W$$

Comparing the above power loss of the SR-MOSFET with the one of Schottky diode, the efficiency at full load will improve approximately 4% by using SR-MOSFET instead of the Schottky diode. The below curve gives the estimated data for delta power loss when using Schottky diode and SR-MOSFET with current from 0A to 3A, and delta power loss is equal to the difference power loss between Schottky diode and SR-MOSFET when output current changed from 0A to 3A as below equation. The Figure 3 gives power loss estimation when using Schottky diode or SR-MOSFET for this 17W Flyback adapter.

$$\Delta P = P_{diode} - P_{mos}$$

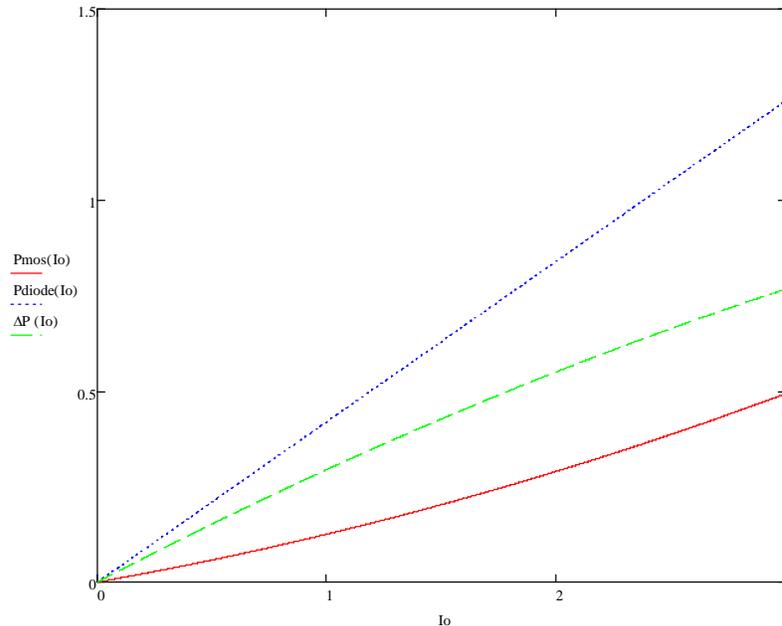


Figure 3. Power loss estimation when using Schottky diode or SR-MOSFET

3 Synchronous Rectifier Flyback Light Load Mode

Although a synchronous rectifier can help to improve a Flyback converter’s efficiency at full load, it normally will sacrifice some efficiency at light load or no load. The reason is: when conventional self-driven synchronous rectification is implemented in a Flyback converter, there is usually no DCM operation any more. When the secondary SR current drops to zero, because the SR is still on, the secondary current will go negative continuously until the SR is turned off by the primary side switch turning on. At light load or no load, there is a significant amount of energy circulating between the primary side and secondary side. This circulating energy increases the conduction losses and decreases the efficiency at light load or no load conditions.

In order to improve this SR-Flyback light load performance and allow it operating in DCM, the UCC24610 compares the SR-MOSFET's voltage of V_d and V_s , only when V_d falls more than -150mV below V_s , the GATE output goes high and the minimum TON timer is triggered. The GATE voltage stays high as long as the programmed minimum TON timer has not expired; after the minimum TON timer expires, the GATE output is turned off when the V_d - V_s voltage rises to -5mV. It is essentially monitoring the current flowing through the SR-MOSFET in order to control the gate output so the SR-MOSFET works just like a near-ideal diode and there is no reverse current during light load mode.

To achieve high efficiency and low standby loss at the same time, the UCC24610 also provides a light load mode to minimize standby losses which is achieved through the programmed minimum on-time. During normal operation, the synchronous rectifier conduction time is longer than the programmed minimum on-time. If the load current decreases enough that the SR conduction time becomes shorter than the programmed minimum on-time, a light-load condition is detected. The light-load latch is set and the next GATE output pulse is blanked, so only the body diode of the controlled SR-MOSFET conducts. This comparison between SR conduction time and minimum on time occurs every switching cycle, regardless of whether the GATE output pulse is enabled or blanked. When load current increases enough that the body-diode conduction time becomes longer than the programmed minimum on time, the light-load latch is cleared and the next GATE output pulse is enabled and the controlled MOSFET resumes SR operation. Figure 4 depicts the progression into Light-Load mode for a DCM flyback application as the load decreases, while Figure 5 depicts the reverse progression back to run mode.

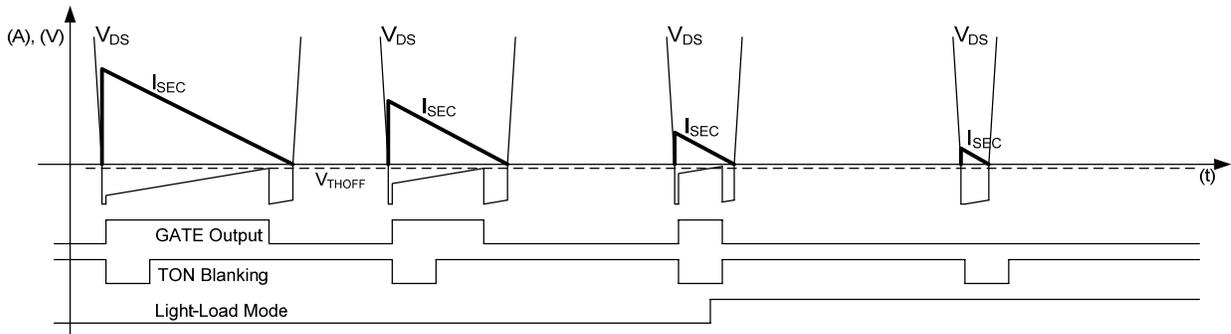


Figure 4. Decreasing Load Current Progression Leads to Light-Load-Mode Operation

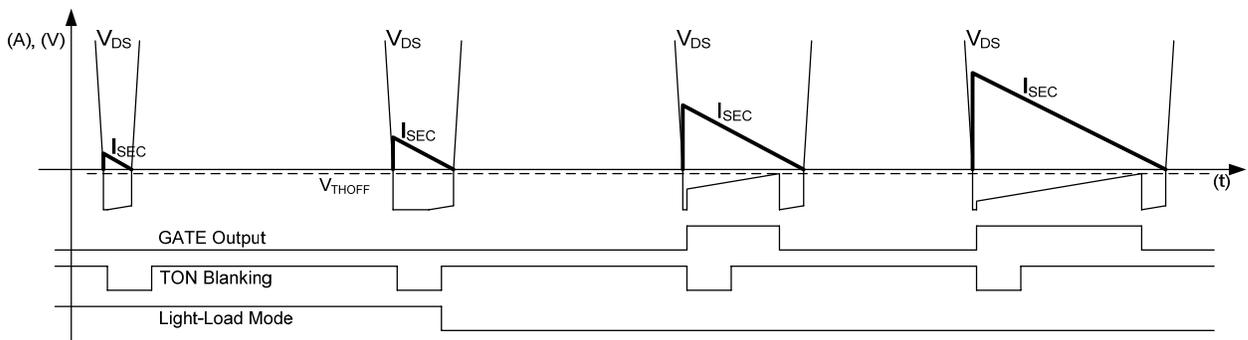


Figure 5. Increasing Load Current Progression Returns to Run-Mode Operation

Based on the above light load mode, the UCC24610 has utilized this programmable minimum on time TON architecture so that the MOSFET works as a near-ideal diode, the output current will not reverse its direction as is common in most SR-Flyback, and this will increase the light load efficiency. Meanwhile, with the proper programmed minimum on time, the UCC24610 can be disabled during no-load condition to minimize the standby loss.

Besides the light load performance improvement, the minimum on-time TON is programmed with a resistor from TON (pin 3) to GND to blank the response of the turn-off detection circuit to prevent GATE from being turned-off from spurious crossings of VTH(off) due to noise and ringing. TON is triggered by the GATE turning on.

4 17W adapter design

Based on UCC28610 (green mode Flyback controller) and UCC24610 (green rectifier controller), this application note demonstrates a 17W/5.6V high efficiency SR-Flyback converter reference design, PMP4305. The dimensions for this demonstration board is 39mm(L)x50mm(W)x20mm(H), with a power density of 7W/in³. Figure 6 shows the PMP4305 reference design board photos with the electrical specifications summarized in Table 1.

4.1 Design Specification

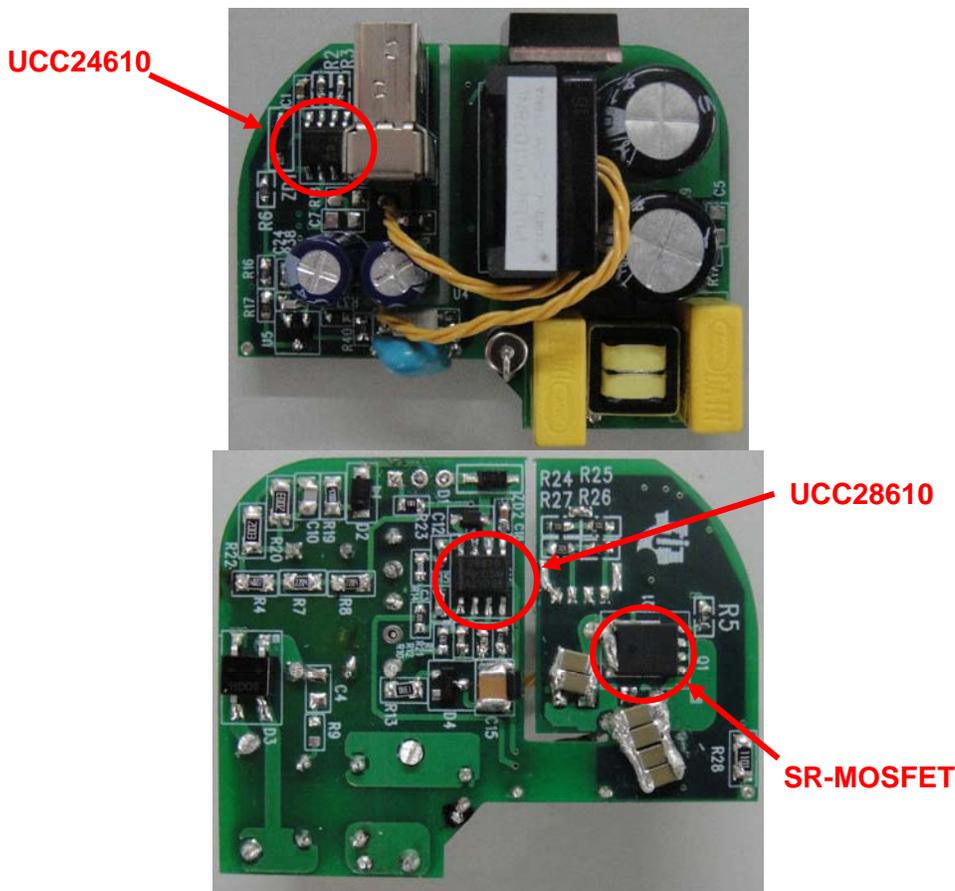


Figure 6. Photos of 17W adapter demonstration board, PMP4305

Table 1. Electrical Design Specification

Specification Items	Min	Typical	Max
Input AC Voltage	90Vac	220Vac	264Vac
Output Voltage Tolerance	5.45V	5.6V	5.8V
Allowable output voltage range during Transient	5.3V		5.8V
Output Power			17W
Efficiency(Full load)	84%		
Turn-on Delay			5s
Output Rise time			20ms
Standby Loss			150mW
Output Ripple			200mV
Overload protection		4A	

4.2 Schematic

Figure 7 shows the schematic of this 17W, 5.6V output voltage demonstration board design. The schematic includes an input EMI filter, the bridge diode, the cascade Flyback converter stage with the UCC28610 controller on the primary side, and a synchronous rectifier controlled by the UCC24610 on the secondary side.

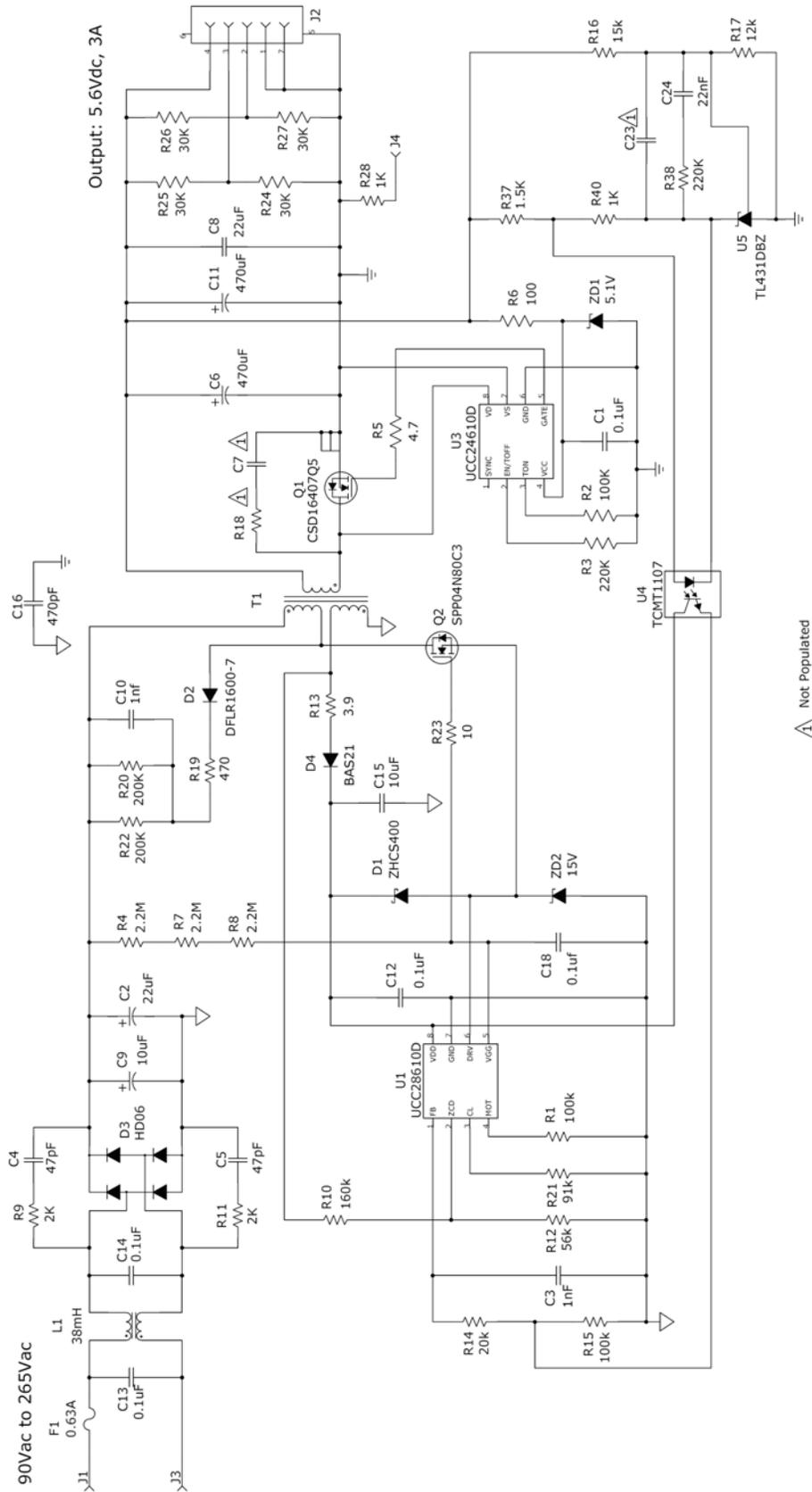


Figure 7. Schematic of the design

4.3 Input Capacitor Selection

Because of the limited space, to decrease the volume of input electrolytic bulk capacitor, we assume the minimum voltage of the input capacitor is 60% of the peak voltage; the minimum and maximum input capacitor voltage can be calculated as below:

$$V_{cap\ max} = 90V \times \sqrt{2} = 127.279V$$

$$V_{cap\ min} = 90V \times \sqrt{2} \times 0.6 = 76.37V$$

The input electrolytic bulk capacitor will be charged when input voltage is higher than the minimum bulk voltage and will provide energy after the voltage reaches maximum voltage. The conduction angle can be calculated as:

$$\theta = 90 - a \sin\left(\frac{V_{cap\ min}}{V_{cap\ max}}\right) \times \frac{180}{\pi} = 90 - a \sin\left(\frac{76.37V}{127.279V}\right) \times \frac{180}{\pi} = 53.13$$

With an input AC line frequency of 50Hz, the discharge time of input capacitor can be calculated as below:

$$T_{dis} = \frac{1}{2 \times f_{line}} \times \left(1 - \frac{\theta}{180}\right) = \frac{1}{2 \times 50Hz} \times \left(1 - \frac{53.13}{180}\right) = 7.05ms$$

The input bulk capacitor needs to provide energy during the discharge time. Assuming the converter's efficiency is 0.85. The maximum input power can be calculated as below:

$$P_{in} = \frac{P_o}{\eta} = \frac{17W}{0.85} = 20W$$

The input bulk capacitance can be calculated as below:

$$C_{in} = \frac{2 \times P_{in} \times T_{dis}}{V_{cap\ max}^2 - V_{cap\ min}^2} = \frac{2 \times 20W \times 7.05ms}{127.279^2 V^2 - 76.37^2 V^2} = 27 \mu F$$

From the above calculation, we can choose a 10uF and 22uF electrolytic capacitors in parallel as the input bulk capacitance.

4.4 Transformer Design

4.4.1 Turns Ratio Chosen

In this design, the UCC28610 has a PWM modulation algorithm that varies both switching frequency and primary current while maintaining discontinuous current mode (DCM) or transition mode operation over the entire operating range. To calculate the turn ratio of transformer, it is assumed that the converter operates at transition mode at the minimum input voltage and full output load, and the maximum duty cycle is defined as 0.5. The turn's ratio for the Flyback's transformer can be calculated as below equation:

$$n = \frac{V_{cap\ min} \times D_{max}}{V_o \times (1 - D_{max})} = \frac{76.37V \times 0.5}{5.6V \times (1 - 0.5)} = 13.6$$

In order to minimize the standby loss, the bias output voltage for UCC28610 is setting to 16V. And the turn ratio can be calculated the same as above equation.

4.4.2 Core Selection

4.4.2.1 Primary and Secondary RMS Current Calculation

The primary peak and RMS Current is calculated as below:

$$I_{inavg} = \frac{P_o}{\eta \times V_{cap\ min}} = \frac{17W}{0.85 \times 76.37V} = 0.262A$$

$$I_{inpk} = \frac{I_{inavg} \times 2}{D_{max}} = \frac{0.262A \times 2}{0.5} = 1.048A$$

$$I_{inrms} = I_{inpk} \times \sqrt{\frac{D_{max}}{3}} = 1.048A \times \sqrt{\frac{0.5}{3}} = 0.428A$$

As for secondary RMS current calculation, the secondary conduction duty cycle can be calculated as below:

$$D_{sec} = \frac{2 \times I_o}{I_{inpk} \times n} = \frac{2 \times 3A}{1.048A \times 13.5} = 0.421$$

So the secondary winding RMS current can be calculated as below:

$$I_{srms} = I_{inpk} \times n \times \sqrt{\frac{D_{sec}}{3}} = 1.048 \times 13.6 \times \sqrt{\frac{0.421}{3}} = 5.338A$$

4.4.2.2 Inductance selection

To trade off the core's size and efficiency, the normal operation frequency is set to 100 kHz at full output load, and the primary inductance of transformer can be calculated as below equation:

$$L_p = \frac{2 \times P_o}{\eta \times I_{inpk}^2 \times f_s} = \frac{2 \times 17W}{0.85 \times 1.048^2 A^2 \times 100 \times 10^3 Hz} = 360\mu H$$

4.4.2.3 Core Selection

Because the adapter operates in a sealed case without the advantages of an open frame in regards to thermal dissipation, the current density should not be too high in order to avoid an excessive high temperature rise. In this case, the current density is chosen to be 6A/mm². Assuming the core's fill factor K to be 0.32 to ensure adequate winding room and the B_{max} to be 320mT, the below equation should be considered:

$$\begin{cases} L_p \times I_{inpk} = N_p \times B_{max} \times A_e \\ N_p \times (I_{prms} + \frac{N_s}{N_p} \cdot I_{srms}) = K \times A_w \times j \end{cases}$$

From the equation above, we can derive the area product (AP) as below.

$$A_p = A_e \cdot A_w = \frac{L_p \times I_{inpk} \times (I_{prms} + \frac{I_{srms}}{n})}{K \times j \times B_{max}} = \frac{360\mu H \times 1.048A \times (0.428A + \frac{5.338A}{13.6})}{0.32 \times 6 \frac{A}{mm^2} \times 3200G} = 5.034 \times 10^{-10} m^4$$

Based on the above Ap value, the core of an EPC17 is chosen for this 17W/5.6V adapter project design.

So the number of turns can be calculated as below:

$$N_p = \frac{L_p \times I_{inpk}}{B_{max} \times A_e} = \frac{360 \times 10^{-6} H \times 1.048A}{3200G \times 22.8 \times 10^{-6} m^2} = 52$$

$$N_s = \frac{N_p}{n} = \frac{52}{13.6} = 4$$

Choose the current density to be 6A/mm² based on thermal considerations. The wire can be selected as below:

$$S_p = \frac{I_{prms}}{j} = \frac{0.428A}{6A/mm^2} = 0.071mm^2$$

$$S_s = \frac{I_{srms}}{j} = \frac{5.338A}{6A/mm^2} = 0.89mm^2$$

To get better performance, we need to choose the wire no less than twice of the skin depth. The skin depth can be calculated as below□

$$\Delta = \frac{7.5}{\sqrt{fs}} = \frac{7.5}{\sqrt{100 \times 10^3}} = 0.24mm$$

From the result, the wire diameter should be less than 0.48mm. So, AWG 25 wire is chosen.

$$S_{25} = 0.1624mm^2$$

$$\frac{S_p}{S_{25}} = \frac{0.071mm^2}{0.1624mm^2} = 0.43$$

$$\frac{S_s}{S_{25}} = \frac{0.89mm^2}{0.1624mm^2} = 5.5$$

For the primary winding, we can choose AWG 25 or thinner wire and the secondary winding needs to use 6 wires in parallel, of 25 AWG.

4.5 Main MOSFET Selection

The MOSFET selection needs to consider both the voltage stress and efficiency. The maximum voltage stress on the primary MOSFET is about 600V and the current stress is equal to the primary peak current. Considering the voltage derating of the MOSFET, we choose an 800V 4A SPP04N80C3 as the main MOSFET. The power loss on the MOSFET can be calculated as below:

$$\begin{aligned} P_{mos} &= (I_{irms}^2 \times R_{dson}) + \left(\frac{1}{2} \times C_{oss} \times (V_{in} - n \cdot V_o)^2 \times f_s \right) + (Q_g \times V_{cc} \times f_s) \\ &+ \left(\frac{1}{2} \times I_{inpk} \times (V_{in} - n \cdot V_{o1}) \times t_f \times f_s \right) = 0.428^2 A^2 \times 2\Omega + \frac{1}{2} \times 12 \times 10^{-12} F \times (90 \cdot \sqrt{2}V - 13.6 \times 5.6V) \times 100 \times 10^3 Hz \\ &+ 26 \times 10^{-9} C \times 16V \times 100 \times 10^3 Hz + \frac{1}{2} \times 1.048A \times (90 \times \sqrt{2}V - 13.6 \times 5.6V) \times 16 \times 10^{-9} s \times 100 \times 10^3 Hz = 0.451W \end{aligned}$$

4.6 SR-MOSFET Selection

The voltage stress of SR-MOSFET can be calculated as below:

$$V_{dssyn} = \frac{V_{inmax}}{n} + V_o = \frac{264 \times \sqrt{2}V}{13.6} + 5.6V = 33.2V$$

The current stress is equal to the secondary peak current. To get better efficiency, choose a BSC093N04LSG MOSFET with Vds voltage rating of 40V and 49A rated current.

The power loss in the SR-MOSFET can be calculated as below:

$$\begin{aligned} P_{mos} &= (I_{srms}^2 \cdot R_{dson}) + (Q_g \times V_{cc} \times f_s) + (I_d \times V_f \times t_d \times f)_s + \\ &\left(\frac{1}{2} \times I_{spk} \times \left(\frac{V_{in}}{n} + V_o \right) \times t_r \times f \right)_s = 5.338^2 A^2 \times 10m\Omega + 24 \times 10^{-9} C \times 16V \times 100 \times 10^3 Hz \\ &+ 2.5A \times 1.1V \times 500 \times 10^{-9} s \times 10^5 Hz + \frac{1}{2} \times 13.62A \times \left(\frac{101.8V}{13.6} + 5.6V \right) \times 2.4 \times 10^{-9} s \times 10^5 Hz = 0.454W \end{aligned}$$

4.7 Output Capacitor Selection

Output capacitors should be designed to meet the output ripple requirements. The output capacitor will be charged when the secondary current is greater than the output current and will be discharged during the rest of the cycles as shown in Figure 8.

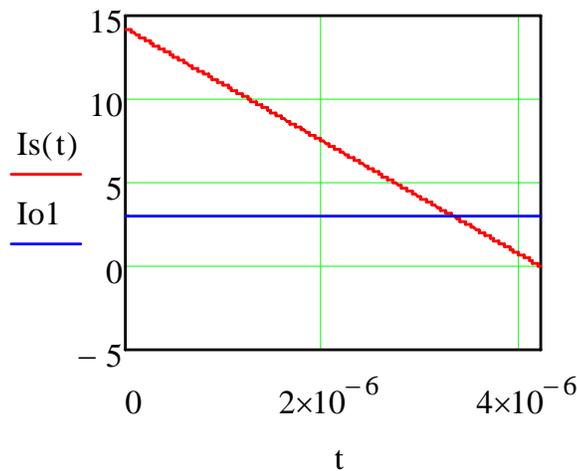


Figure 8. Output capacitor charge sketch

From Figure 8, $I_s(t)$ is the current of secondary winding and I_{o1} is the full load output current. When the current of $I_s(t)$ greater than I_{o1} , the output capacitors will be charged from the transformer. The following equations can be used to calculate the output capacitor values for a desired output voltage ripple:

$$C_{out} = \frac{(I_{spk} - I_o)^2 \times D_{off}}{2 \times \Delta V_o \times I_{spk} \times f_s} = \frac{(13.6A - 3A)^2 \times 0.421}{2 \times 200 \times 10^{-3}V \times 13.6A \times 100 \times 10^3 Hz} = 86\mu F$$

The ESR of the capacitor accounts for the output voltage ripple and can be calculated as below:

$$\Delta V_o = ESR \times (I_{spk} - I_o)$$

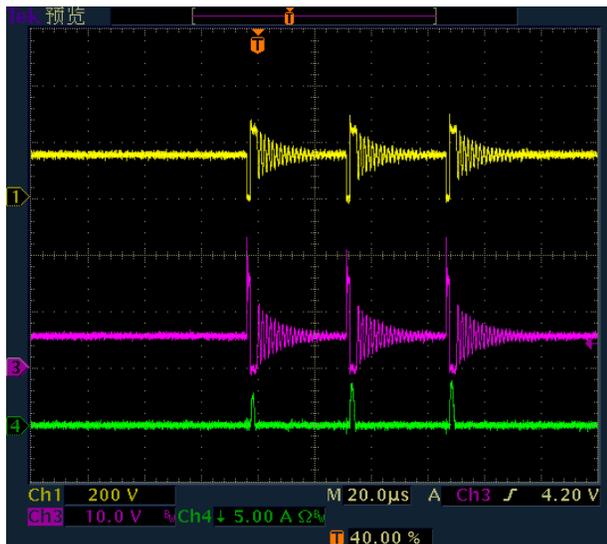
A Flyback converter operating in DCM has higher peak currents than a Flyback operating in CCM so that the ESR is the main consideration factor for output capacitor selection. In this design, the output voltage ripple must to be less than 200mV with approximately 14A of secondary side ripple current. A capacitor with an ESR less than 15mOhm is required.

4.8 Experimental Results

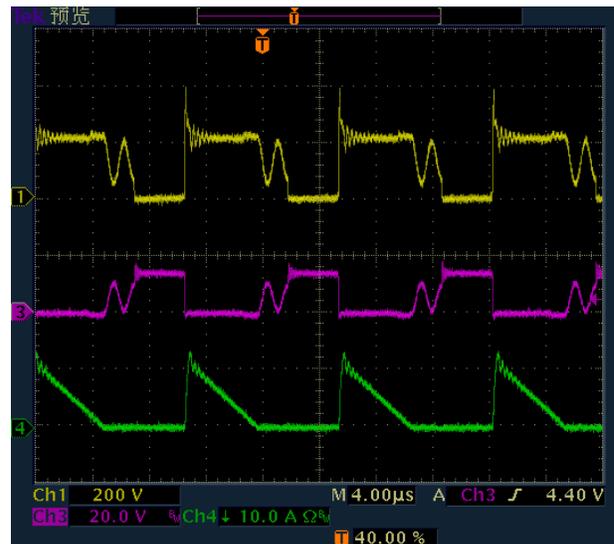
4.8.1 Vds and Ids of SR-MOSFET

Figure 9 shows the operation waveforms with MOSFET Vds voltage (CH1); SR-MOSFET Vds voltage (CH3) and SR-MOSFET Ids current (CH4) at full load and no load. According to the no load waveforms, the UCC28610 can operate in green mode with burst switching to improve no load efficiency. And the conduction period time of SR-MOSFET is less than the programmed minimum on-time, which results in the UCC24610 operating in light load mode without gate voltage to the SR-MOSFET. The body diode of the SR-MOSFET will conduct at no load to avoid the high frequency switching losses and reversed current on the SR-MOSFET. Based on the operation modes of the UCC28610 and UCC24610, this solution can improve no load and light load efficiency over conventional methods.

Figure 9 also gives the full load waveforms at 110Vac and 220Vac input. From the Vds voltage waveform of the SR-MOSFET, it shows the SR-MOSFET conducts energy during the secondary side on time, which can improve the full load efficiency with lower conduction loss.



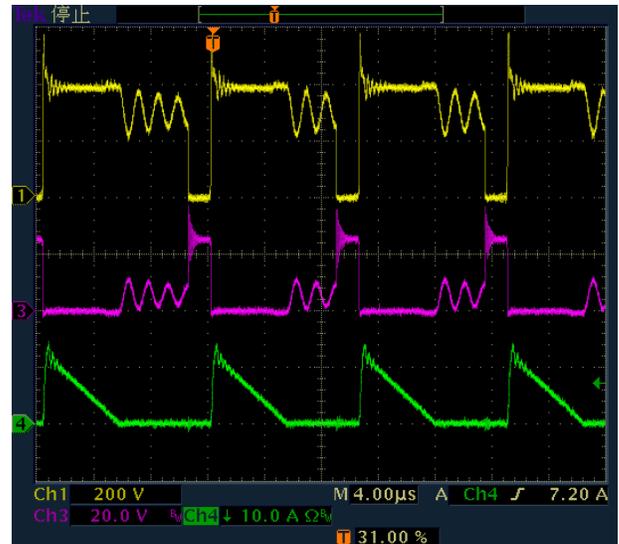
MOSFET Vds and Ids at 110V no load
CH1: 200V/div CH3: 10V/div CH4:5A/div



MOSFET Vds and Ids at 110V full load
CH1: 200V/div CH3: 20V/div CH4:5A/div



MOSFET Vds and Idsat 220V no load
CH1: 200V/div CH3: 20V/div CH4:5A/div



MOSFET Vds and Ids at 220V full load
CH1: 200V/div CH3: 20V/div CH4:5A/div

Figure 9. Voltage and Current on MOSFETs at 110Vac and 220Vac

As mentioned above, in the drain-to-source sensing technique used by the UCC24610, when the voltage drop across the SR-MOSFET (V_{ds}) rises above the $V_{TH(off)}$ threshold, the gate voltage of the SR-MOSFET will be driven to low and the body diode of the SR-MOSFET will take over to transfer energy during this short period. The optimal design is to reduce the body diode conduction period to as small as possible. However, there is a trade off between the SR-MOSFET $R_{ds(on)}$ and body diode conduction time. As shown in Figure 10, the red dashed line gives the operating voltage and current waveform when using an SR-MOSFET with a lower $R_{ds(on)}$. Although the lower $R_{ds(on)}$ can help to reduce conduction loss during the SR-MOSFET on-time, it will trigger the $V_{TH(off)}$ earlier resulting in a longer body diode conduction time, which increases the conduction losses on the secondary side. In this design, the BSC093N04LSG is selected for the SR-MOSFET with 9.3mOhm $R_{ds(on)}$; this is a trade off to maximize the overall efficiency. Figure 11 is the test waveforms with CH3 showing the V_{ds} of SR-MOSFET. It shows the period of SR-MOSFET on-time and body diode conduction time. If a very low $R_{ds(on)}$ was chosen, the body diode conduction time would have been longer and the efficiency would have been lower than expected because of body diode conduction.

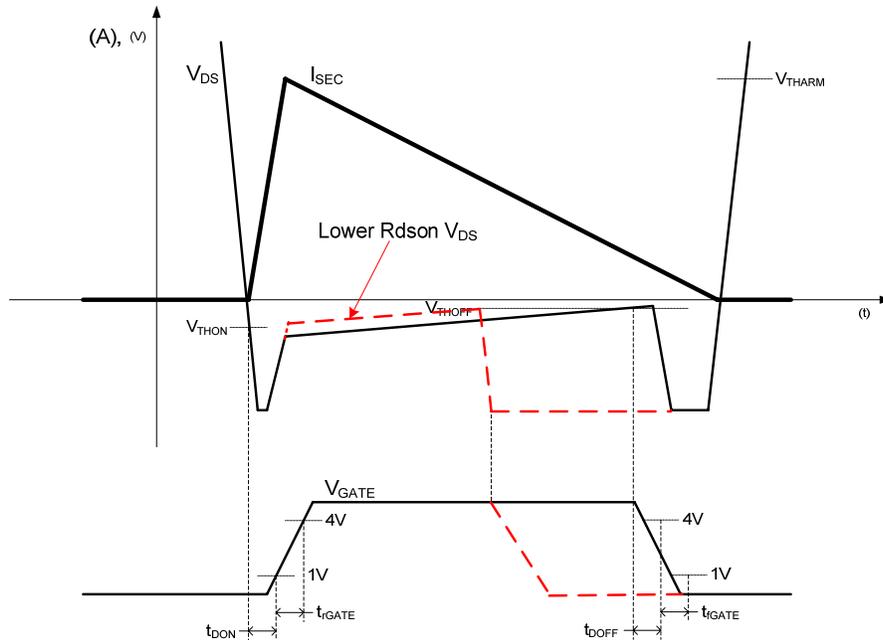


Figure 10. Secondary side voltage and current waveform comparing lower Rdson SR-MOSFET

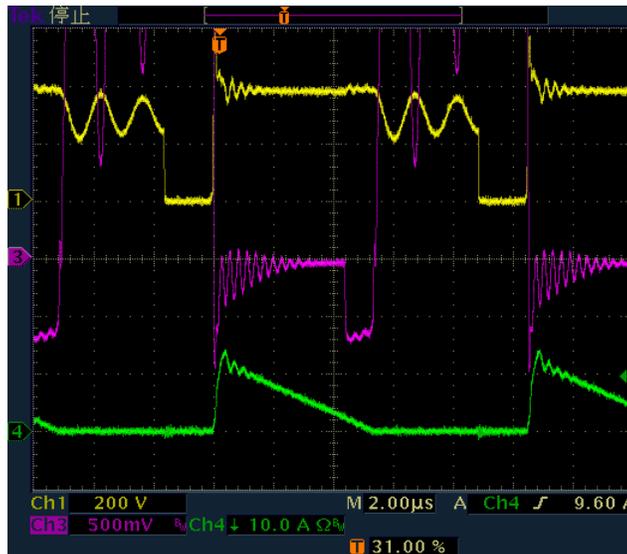


Figure 11. Voltage and Current on MOSFET at 220Vac

CH1: 200V/div CH3: 500mV/div CH4:10A/div

4.8.2 Voltage Tolerance

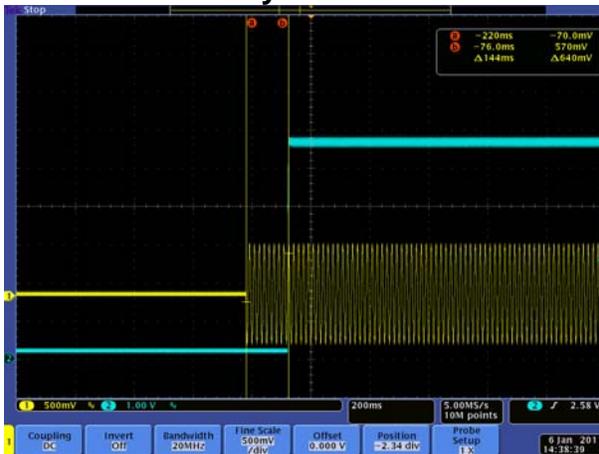
Table 2 gives the output voltage tolerance with no load and full load, it successfully meets the specification within 5.45V to 5.8V at all line and load conditions.

Table 2. Voltage Tolerance

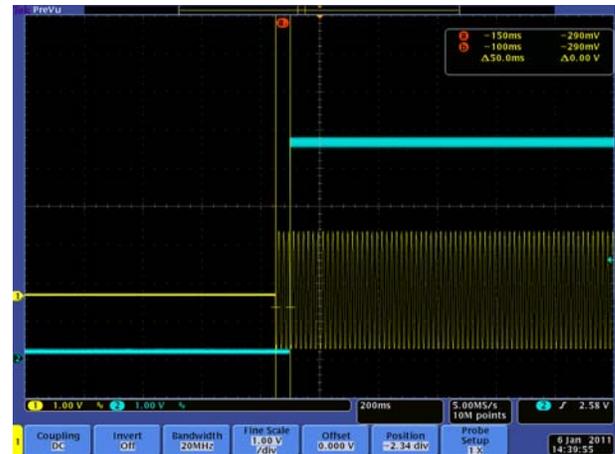
Vin (Vac)	0A	3A
-----------	----	----

115	5.603V	5.600V
230	5.605V	5.601V

4.8.3 Turn on Delay



Full load turn on at 90V input
CH1:100V/div CH2:1V/div



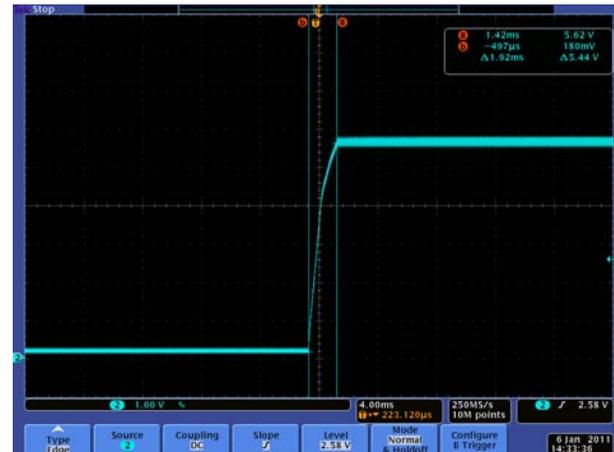
Full load turn on at 264V input
CH1:100V/div CH2:1V/div

Figure 12. Turn on delay at 90Vac and 264Vac

4.8.4 Output Rise Time



Full load rise time at 90V input
CH2:1V/div

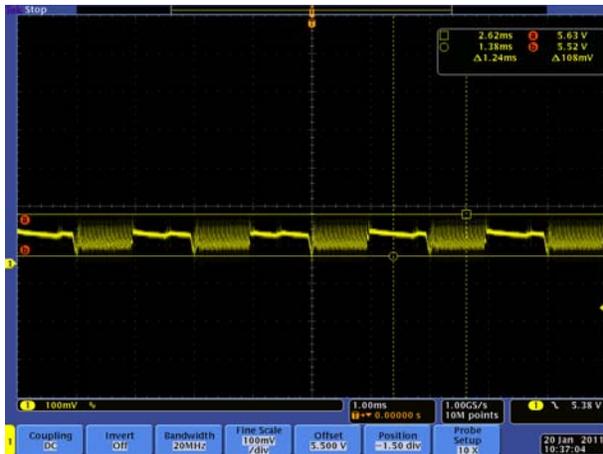


Full load rise time at 264V input
CH2:1V/div

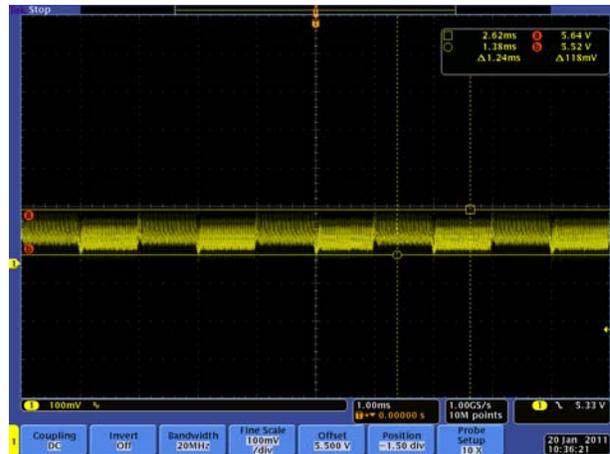
Figure 13. Rise time at 90Vac and 264Vac Full load

4.8.5 Dynamic Performance

Figure 14 and 15 show the output voltage waveform under transient response test between different loads. With fast loop response, the output voltage can be controlled within the range of 5.3V to 5.8V.



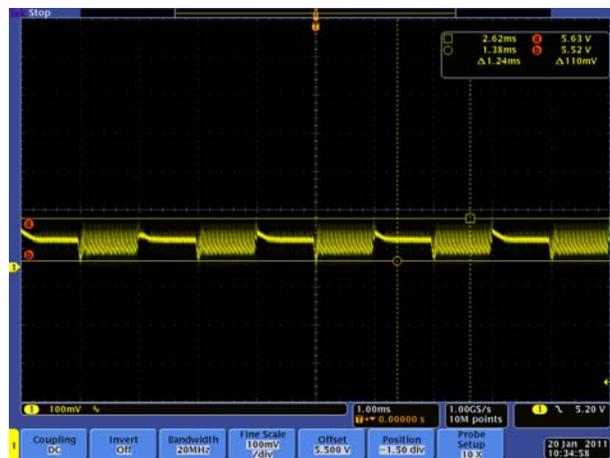
0A to 1A CH1:100mV/div



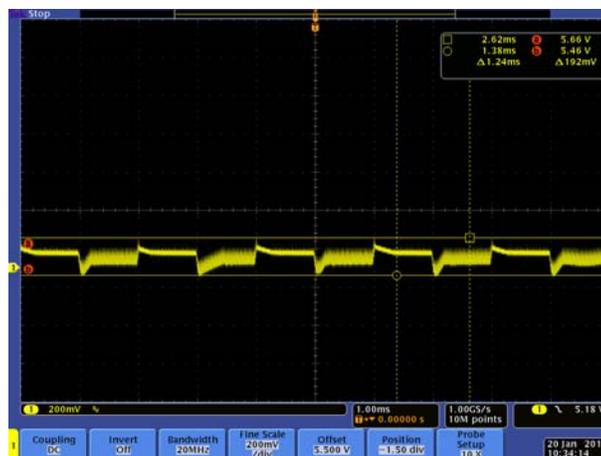
1A to 2A CH1:100mV/div



2A to 3A CH1:100mV/div

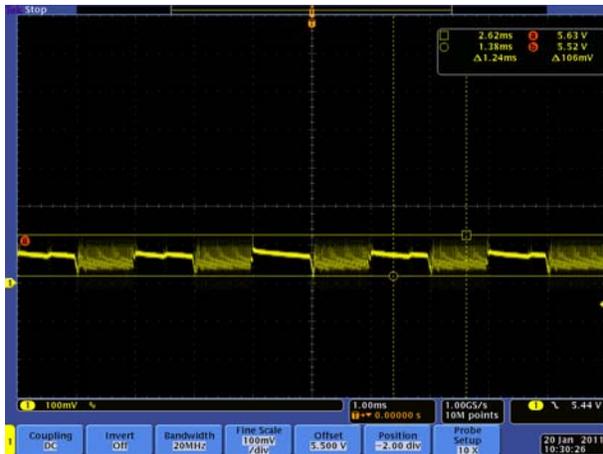


0.08A to 1.5A CH1:100mV/div

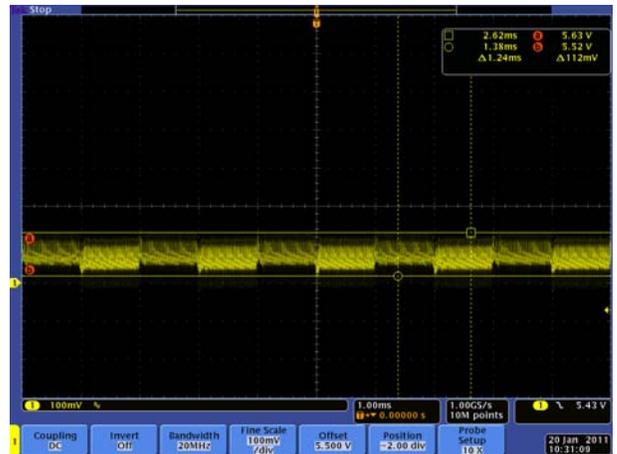


0.08A to 3A CH1:200mV/div

Figure 14. 115Vin Dynamic Performance in different dynamic range



0A to 1A CH1:100mV/div



1A to 2A CH1:100mV/div



2A to 3A CH1:100mV/div



0.08A to 1.5A CH1:100mV/div

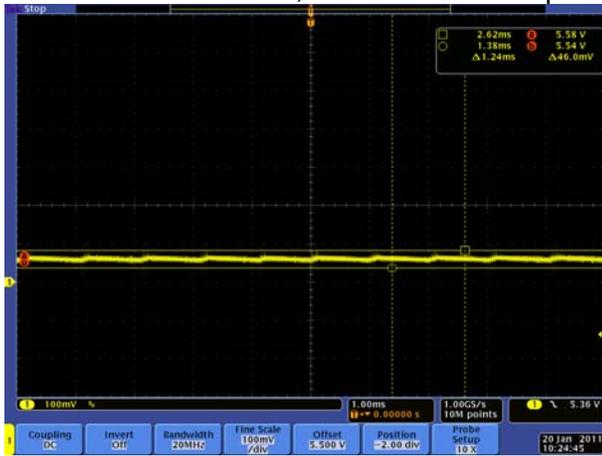


0.08A to 3A CH1:200mV/div

Figure 15. 230Vin Dynamic Performance in different dynamic load ranges

4.8.6 Output Ripple

Figure 16 to 18 shows the output voltage ripple performance at no load, half load, and full load with different input voltages. From the test results, at all test conditions the output voltage ripple is below 200mV, which meets the specification requirement.

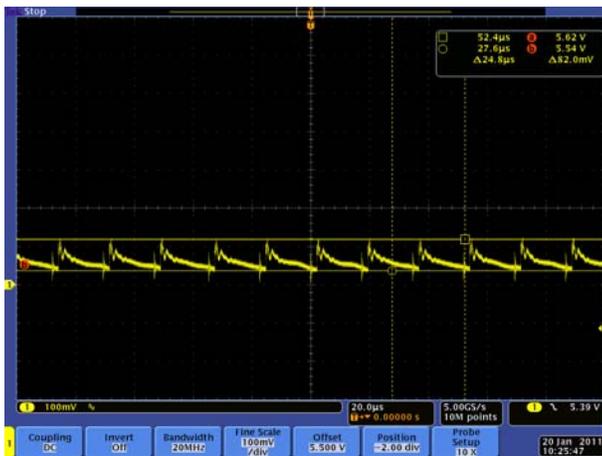


No load ripple CH1:100mV/div at 115V input

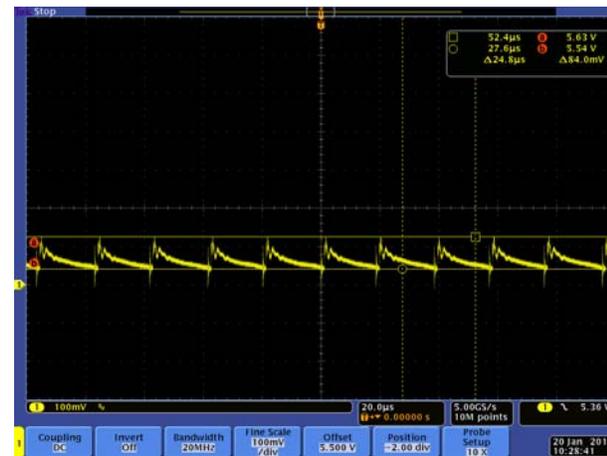


No Load ripple CH1:100mV/div at 230V input

Figure 16. No load Output Ripple in 115Vac and 230Vac



Half load ripple at 115V input CH1:100mV/div



Half load ripple Ch1:100mV/div at 230V input

Figure 17. Half Load output ripple in 115Vac and 230Vac



Full load ripple at 115V input CH1:100mV/div



Full load ripple at 230V input CH1:100mV/div

Figure 18. Full load output voltage Ripple in 115Vac and 230Vac

4.8.7 Efficiency

Figure 19 gives the efficiency performance using the SR-MOSFET with different line input voltages and Figure 20 gives the efficiency comparison curves when using an SR-MOSFET or Schottky diode. From the efficiency curves below, the efficiency can be improved about 4 percent from 0.75A to 3A which is consistent with the theoretical analysis discussed in Section 2.

Meanwhile, from Figure 20, the standby power loss is a little higher when using an SR-MOSFET instead of the Schottky diode. Although the UCC24610 has light load mode to reduce stand by power without turning on the SR-MOSFET, the body diode of the SR-MOSFET will have higher conduction losses than a Schottky diode at light load and the UCC24610 will also consume some power. In order to reduce the standby power with SR control, an external circuit can be used to disable the UCC24610 using EN/TOFF pin. Also, a Schottky diode may be added in parallel with the SR-MOSFET to help reduce standby power loss.

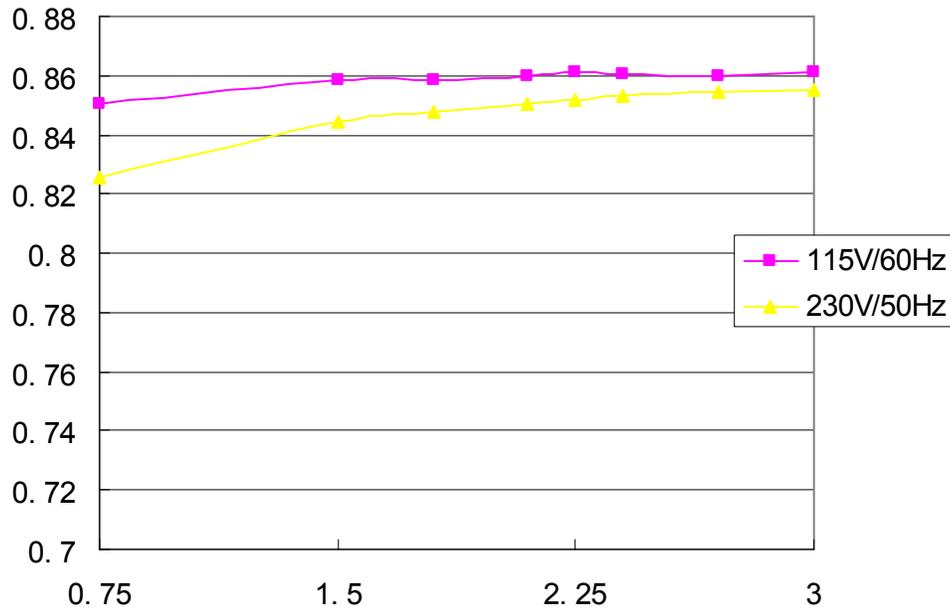


Figure 19. Efficiency Curve with different input voltages

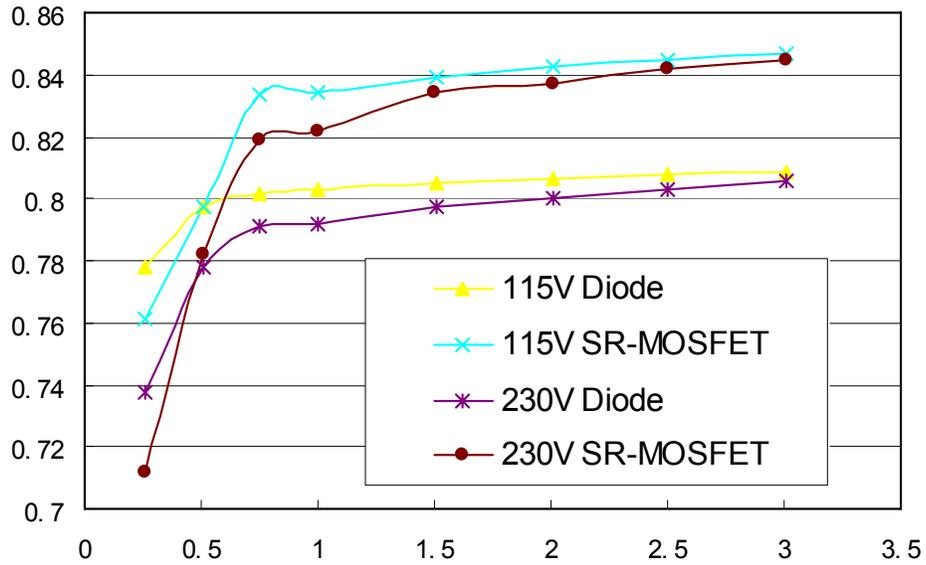


Figure 20. Efficiency Comparison between Schottky diode and SR-MOSFET

4.8.8 No load Power Loss

Table 3. No load power loss at different input voltages

Vin	Input power at no load
-----	------------------------

100V/50Hz	0.090W
115V/60Hz	0.095W
230V/50Hz	0.120W

4.8.9 Over load Protection

The unit will shutdown when the load current increases to 4A and will try to restart every 750ms.



Overload protection at 115V input
CH2:2V/div CH4:2A/div



Overload protection at 230V input
CH2:2V/div CH4:2A/div

Figure 21. Over load protection in 115Vac and 230Vac input

5 Bill of Materials

Table 4 lists the PMP4305 demonstration board components as configured corresponding to the schematic shown in Figure 7. Part types and manufacturers can be modified according to specific application requirements.

Table 4. Bill of Materials

Count	Ref Des	Description	Part Number	MFR
2	C13,14	CAP .10UF 305VAC EMI SUPPRESSION	B32921C3104M	EPCOS
3	C1,C12,C18	CAP, CER 0.1UF 25V X7R RAD	RDER71E104K0K1C03B	Murata
1	C24	CAP CER 22000PF 50V 10% X7R 0603	GRM188R71H223KA01D	Murata
1	C3	CAP, CER 1NF 16V 10% X7R 0603	GRM033R71C102KD01D	Murata
1	C23	NA		
1	C10	CAP CER 1000PF 250V 10% X7R 0805	GRM21AR72E102KW01D	Murata
1	C8	CAP CER 22UF 10V X7R 1210	GCM32ER71A226KE12L	Murata
2	C4,C5	CAP CER 470PF 250V X7R 0805	C0805C471KARACTU	Kemet
1	C7	NA		
1	C15	CAP CER 10UF 25V X7R 1210	GCM32ER71E106KA57L	Murata
2	C6,C11	CAP, Aluminum, 6.3V 560uf, 20%	PE561M6R3E080P1PF	Capxon
1	C2	CAP 22UF 400V ELECT KXG RAD	EKXG401ELL220MK20S	United Chemi-Con

1	C9	CAP, Aluminum, 400V 10uf, 20%	EGS106M2GG16RR	Samxon
1	D4	DIODE SWITCH 200V 250MW SOT23-3	BAS21	Diodes
1	D3	RECT BRIDGE GP 600V 0.8A MINIDIP	HD06	Diodes
1	D2	DIODE STD REC 1A 600V POWERDI123	DFLR1600-7	Diodes
1	ZD2	Diode, Zener, 15V, 5-mA	BZT52C15	Diodes
1	ZD1	DIODE ZENER 5.1V 500MW SOD-123	BZT52C5V1-7-F	Diodes
1	D1	DIODE SCHOTTKY 40V 0.4A SOD-323	ZHCS400	Diodes
1	U4	OPTOCPL PHOTOTRANS 1CH 160% 4SOP	TCMT1107	Vishay
1	L1	Common choke 38mH		
1	F1	FUSE 3.6X10 FAST IEC .630A AXL	0876.630MXEP	littlefuse
1	J2	USB Connector		
1	C16	CAP 470PF 250VAC CERAMIC Y1/X1	ECK-ANA471MB	Panasonic - ECG
1	R23	RES 10.0 OHM 1/10W 1% 0603 SMD	std	std
1	R15	RES 100K OHM 1/10W 1% 0603 SMD	std	std
1	R38	RES 220K OHM 1/10W 1% 0603 SMD	std	std
1	R17	RES 12.0K OHM 1/10W 1% 0603 SMD	std	std
1	R16	RES 15.0K OHM 1/10W 1% 0603 SMD	std	std
1	R10	RES 160K OHM 1/10W 1% 0603 SMD	std	std
1	R37	RES 1.50K OHM 1/10W 1% 0603 SMD	std	std
1	R14	RES 20.0K OHM 1/10W 1% 0603 SMD	std	std
1	R12	RES 56.0K OHM 1/10W 1% 0603 SMD	std	std
1	R1	RES 100K OHM 1/10W 1% 0603 SMD	std	std
1	R21	RES 91.0K OHM 1/10W 1% 0603 SMD	std	std
1	R40	RES 1.00K OHM 1/10W 1% 0603 SMD	std	std
1	R13	RES 3.9 OHM 1/8W 1% 0805 SMD	std	std
2	R9,R11	RES 2.00K OHM 1/10W 1% 0603 SMD	std	std
1	R18	NA		
3	R4,R7,R8	RESISTOR 2.20M OHM 1/8W 1% 0805	std	std
1	R19	RES 470 OHM 1/8W 1% 0805 SMD	std	std
1	R28	RES 1.00K OHM 1/4W 1% 1206 SMD	std	std
2	R20,R22	RES 200K OHM 1/4W 1% 1206 SMD	std	std
1	R6	RES 100 OHM 1/10W 1% 0603 SMD	std	std
1	R2	RES 100K OHM 1/10W 1% 0603 SMD	std	std
1	R3	RES 220K OHM 1/10W 1% 0603 SMD	std	std
4	R24,R25,R26,R27	RES 30.0K OHM 1/10W 1% 0603 SMD	std	std
1	R5	RES 4.7 OHM 1/10W 1% 0603 SMD	std	std
1	Q2	MOSFET N-CH 800V 4A TO-220	SPP04N80C3	Infineon
1	U5	IC, Precision Adjustable Shunt Regulator	TL431AIDBZ	TI
1	Q1	MOSFET N-CH 40V 49A TDSO8	BSC093N04LS G	Infineon
1	U3	IC, SECONDARY-SIDE SYNCHRONOUS RECTIFIER	UCC24610D	TI

		CONTROLLER FOR 5V SYSTEMS		
1	U1	IC, Quasi-Resonant Flyback Green-Mode Controller	UCC28610D	TI
1	T1	PG1078NL S01	PG1078NL S01	Pulse

6 Conclusion

A Synchronous Rectifier Flyback controlled by Texas Instruments' UCC28610 and UCC24610 is proposed in this application note. The theory of a SR-Flyback converter is introduced with main design considerations given. A reference design, PMP4305, of 17W/5.6V Universal AC/DC adapter is designed with experimental verification, which shows higher efficiency and higher power density than a conventional Flyback converter.

7 References

UCC28610 Green-Mode Flyback controller Datasheet, Texas Instruments, ([SLUS888D](#))

UCC24610 GREEN Rectifier™ Controller Device Datasheet, Texas Instruments, ([SLUSA87B](#))

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