Digital Loop Exemplified

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1 Introduction

Industry standard for the control of switch mode power supply (SMPS) systems has been analog control. Now with the advent of high speed, lower cost digital ICs there has been an increased interest in digital control of SMPS. Digital control offers opportunities to optimize operation w.r.t control, efficiency, line and load regulation. The ease of loop control is what makes digital control most attractive especially in non-isolated buck application. A converter with a digital loop can act as its own network analyzer. Based on measurement of the system, a device can optimize its loop response. This is of special advantage in point of load bucks to compensate for actual capacitive loading and adjust as components age. The aim and challenge of this paper is to compare the feedback loop of analog buck solution and feedback loop of a digital buck solution. The entire frequency domain to time domain calculations will be clearly stated and this will give a theoretical confidence in moving from analog to digital solution. A TPS40k analog buck solution will be compared to an UCD921x digital solution and its feedback loops will be designed

2 Feedback Theory

A system always exists in time domain. It can be represented in different domains to get more information on the nature and characteristic of the system. The various domains for signals and systems are as shown in table 1.

Table 1.

Domain	Continuous	Discrete	Used for
Time	t	n	Responses, wave shapes
Frequency	ω	ω	Spectral analysis
Pole-zero	s	z	Analysis, design

The pole-zero domain is of importance in power supply design and in the rest of the paper our discussions will be based on pole zero responses. In the pole-zero domain, the continuous plane is called the s-plane and the discrete plane is called the z-plane. Although a system always exists in the time domain whether it is continuous or discrete, it is important to transit between the various system representations to gather important characteristic information about the system. The pole-zero domain provides information about damping, natural frequencies, time constants and dominant time constants for analysis and design. The transfer function, location of poles and zeros and the like help us in this analysis

Stability of a control system is ascertained from the roots of the characteristic equation. If the roots lie on the right half of “s” plane system is unstable. The transfer function provides a basis for determining important system response characteristics without solving the complete differential equation. These transfer functions are represented in the form of a numerator polynomial and a denominator polynomial in terms of the Laplace variable. In general the transfer function is of the form:

$$H(s) = \frac{b_m s^m + b_{m-1} s^{m-1} + \ldots + b_1 s + b_0}{a_n s^n + a_{n-1} s^{n-1} + \ldots + a_1 s + a_0}$$

The order of the denominator polynomial “n” indicates the order of the system. The above equation can be represented in the factored form as

$$H(s) = \frac{N(s)}{D(s)} = K \frac{(s - z_1)(s - z_2) \ldots (s - z_{m-1})(s - z_m)}{(s - p_1)(s - p_2) \ldots (s - p_{n-1})(s - p_n)},$$

For values of s = z1, z2…zm, the transfer function is a zero and these values are called zeros of the system. The values of s = p1, p2…pn, the transfer function is infinity and these values are called poles of the system. The roots of the characteristic equation varies between poles and zeroes

The feedback loop has to be stable to obtain the desired operation of the power supply. For this negative feedback is used where the output voltage is compared to the reference voltage VREF and the difference is amplified by the error amplifier. The error voltage output of the error amplifier is inverted with respect to the output voltage and is therefore *-180°* out of phase. The goal of the feedback loop is to minimize the error between output voltage and reference voltage. The error is small when the overall feedback loop gain is high. An ideal feedback loop would have infinite gain for all frequencies providing stability for all load conditions. The stability of a feedback system can be characterized in terms of how closely the gain through the feedback path approaches a gain of less than 1, under the conditions of interest. Because the feedback has both a magnitude component and a phase component relative to the output, stability can be expressed in terms of gain margin and phase margin. Therefore the design of the control system involves modifying the loop gain. A compensator network is added for this purpose

3 The Analog Loop In S-Plane

A typical block diagram of a power supply is as shown in figure 1. It consists of a controller, power stage and feedback stage. The feedback stage acts as the interface between the output of the power stage and the input of the controller. The feedback section senses the output of the power stage which may be voltage or current or both of various levels and then converts it to the voltage or current or both to the controller input level and compares with a given reference to generate a signal which is fed to the controller, which in turn controls the power stage as desired. These three blocks were designed and implemented in analog domain. With the growing popularity of microcontrollers and digital signal controllers (DSC), one has seen the possibility of dividing the feedback block into two sections; one section gets inputs from the power stage in analog domain and the other section converts this analog signal to digital domain and interfaces with the DSC

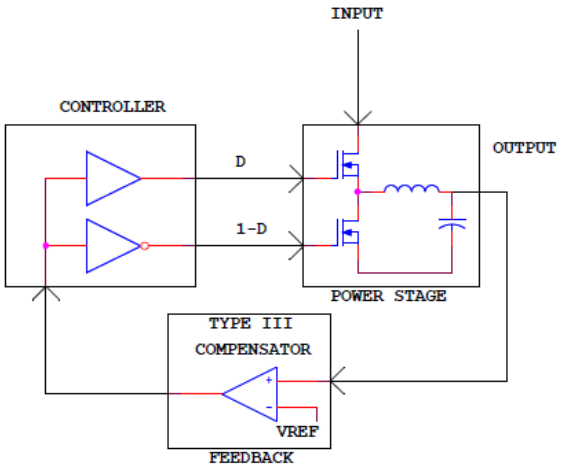

Figure 1.

In analog controllers such as the TPS40k, the compensation is mainly done by a type-III compensator as shown in figure 2. This compensation network has 3 pole points and two zero points, which can be fixed by means of the correct calculation of the values for the individual components

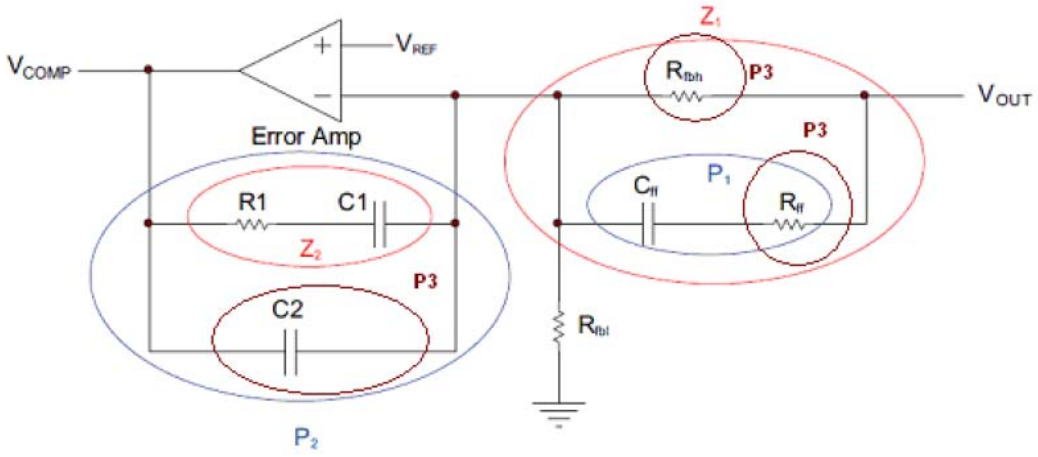

Figure 2.

The error amplifier transfer function with Type III compensation is as below:

$$G_E = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{s \cdot C_2} \; // \left(R_1 + \frac{1}{s \cdot C_1}\right)}{R_{fbh} // \left(R_{ff} + \frac{1}{s \cdot C_{ff}}\right)}$$

By algebraic manipulations it can be expressed in terms of poles and zeros as

$$G_E = \frac{R_{fbh} + R_{ff}}{R_{fbh} \cdot R_{ff} \cdot C_2} \cdot \frac{\left(s + \frac{1}{R_1 \cdot C_1}\right) \cdot \left(s + \frac{1}{(R_{fbh} + R_{ff}) \cdot C_{ff}}\right)}{s \cdot \left(s + \frac{(C_1 + C_2)}{R_1 \cdot C_1 \cdot C_2}\right) \cdot \left(s + \frac{1}{R_{ff} \cdot C_{ff}}\right)}$$

This equation gives two zeros at frequencies of Fz1, Fz2 and three poles at frequencies of Fp1, Fp2, Fp3

$$F_{Z1} = \frac{1}{2\pi \cdot (R_{fbh} + R_{ff}) \cdot C_{ff}} \quad \text{and} \quad F_{Z2} = \frac{1}{2\pi \cdot R_1 \cdot C_1}$$

$$F_{P1} = \frac{1}{2\pi \cdot R_{ff} \cdot C_{ff}} \quad \text{and} \quad F_{P2} = \frac{1}{2\pi \cdot R_1 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)} \quad F_{P3} = \frac{1}{2\pi \cdot \frac{R_{fbh} + R_{ff}}{R_{fbh} \cdot R_{ff} \cdot C_2}}$$

The bode plot for the above type III compensation is given in figure 3.

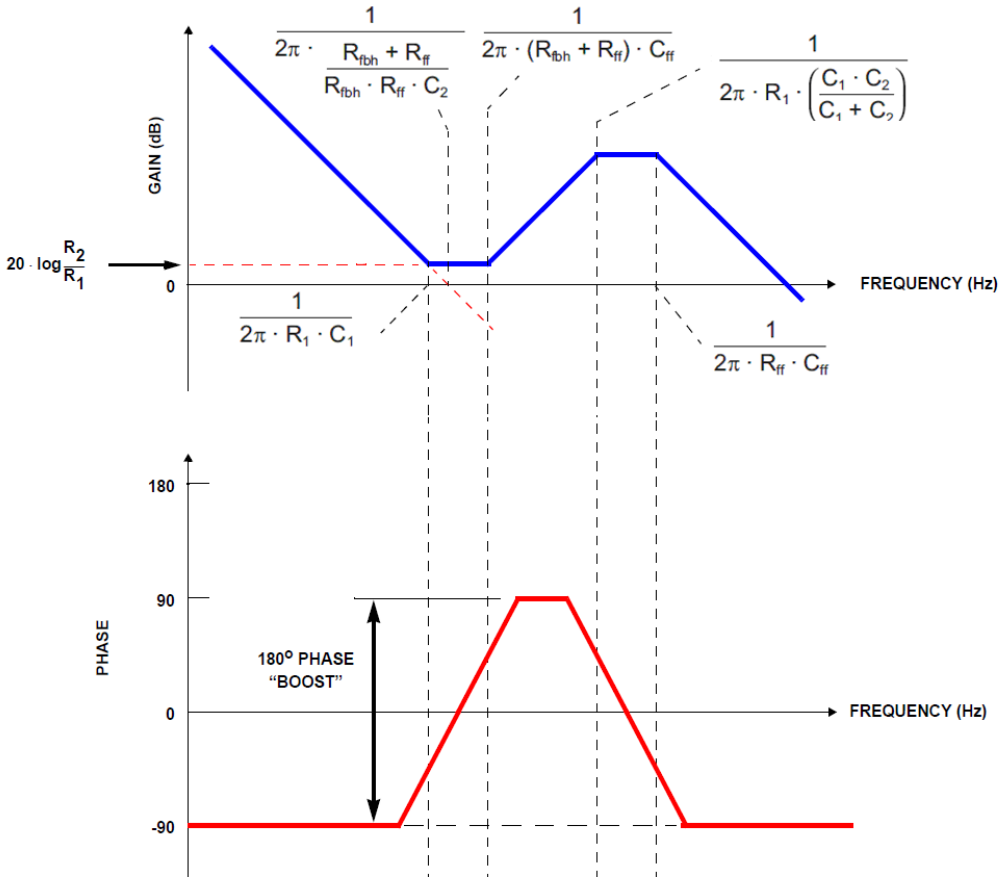

Figure 3.

Type III compensation provides two zeros and two poles which push the cross-over frequency as high as possible and boosts the phase margin greater than 45 degree. A higher bandwidth yields a faster load transient response. The faster transient response results in a smaller output voltage spike

The individual values of R and C required for compensating the error amplifier is as below:

$$F_C = \frac{F_{SW}}{10}$$

$$R_{ff} = \frac{1}{2\pi \cdot C_{ff} \cdot F_{SW}}$$

$$C_{ff} = \frac{\sqrt{L \cdot C_{OUT}}}{K \cdot R_{fbh}} \quad R_1 = \frac{(2\pi \cdot F_C)^2 \cdot L \cdot C_{OUT} + 1}{2\pi \cdot F_C \cdot C_{ff}} \cdot \frac{V_{RAMP}}{V_{IN}}$$

$$C_1 = \frac{\sqrt{L \cdot C_{OUT}}}{K \cdot R_1} \quad C_2 = \frac{1}{2\pi \cdot R_1 \cdot F_{SW}}$$

Rfbh and Rfbl are decided by the output voltage

For TPS40k series of controllers there is a loop stability tool which is available online which calculates the values for the R and C in the above pole-zero equation.

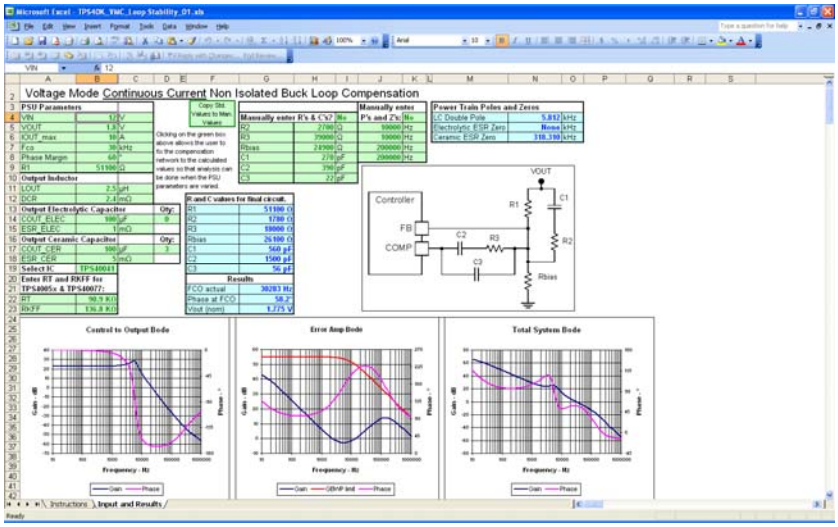

Figure 4.

4 The Digital Loop In Z-Plane

While transiting from an analog domain to a digital domain, two key components are essential. One is the analog to digital converter and the other is the sample and hold circuit. The sample and hold circuit consists of two important functions, one is sampling the signal at pre-determined times and second is holding the value till the next sample so that the ADC can convert the held analog value to the corresponding digital value. The sampling logic signal in practice is of the order of few hundred nanoseconds to a few micro seconds to allow for the acquisition of the analog signal by the hold circuit. A typical digital power supply block is as shown in figure 5

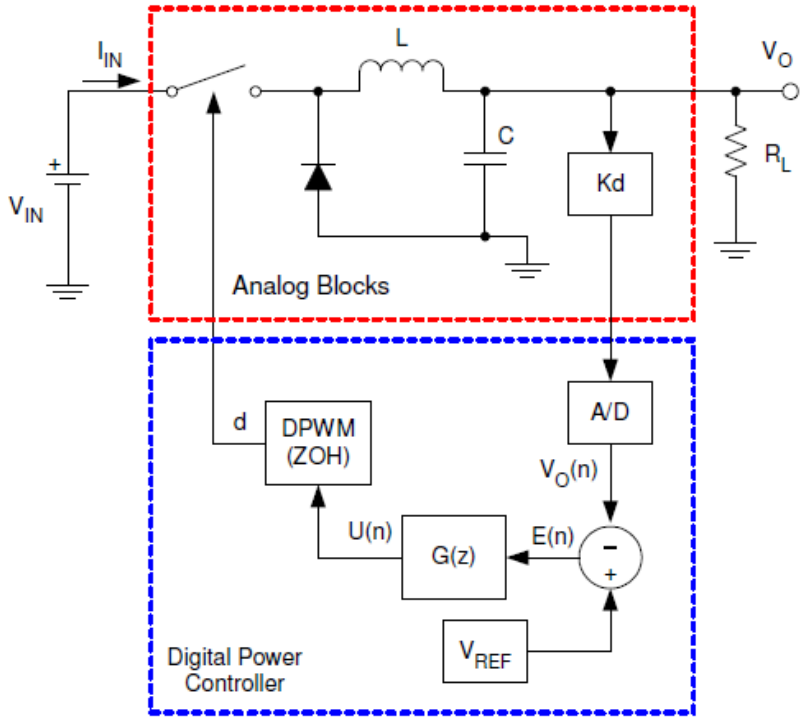

Figure 5.

Consider the signal x(t) shown in figure 5. For simplicity, the signal x(t) considered is a linear ramp. The signal is sampled with sample interval T. The sample interval is the inverse of the sampling frequency. The sampling frequency is chosen such that it is at least twice the maximum frequency component of the band-limited signal x(t). The discretized signal x(n) is shown in figure 6 and its discrete domain representation is as below:

$$x(n) = \sum_{k=0}^{\infty} x(k).\ \delta(n-k)$$

Or

$$X(z) = \sum_{k=0}^{\infty} x(k)z^{-k}$$

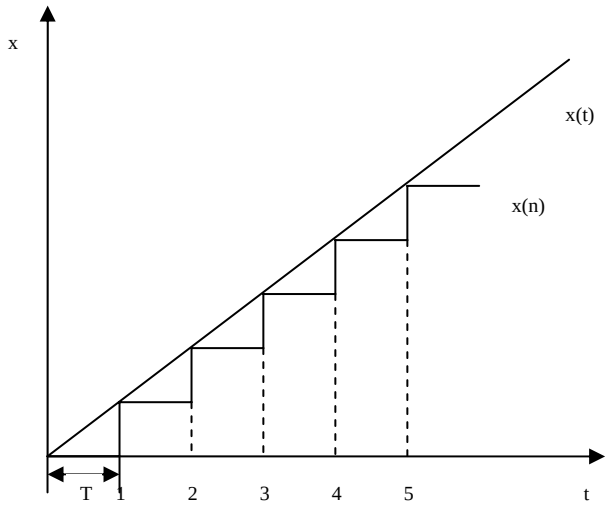

Figure 6.

If the above equation of X (z) is multiplied by z^{-1} then,

$$X(z) \cdot z^{-1} = \sum_{k=0}^{\infty} x(k)z^{-(k+1)}$$

This when reconstructed will give a signal that is delayed w.r.t the original signal x(t) by one unit time step (i.e. 1T). This implies that passing a signal through a z^{-1} block introduces a unit time delay. If one were to pass a signal through z^{-m} block, then the input signal will be time shifted by m time delays or by mT. While implementing a unit delay in hardware, one will have to pass the input signal in a memory element for a period of 1T. Then after 1T duration has elapsed, the value in the memory is released as output and current input is stored in the memory

All systems in digital domain are considered as digital filters as they modify the wave shape of the signal and hence the harmonic amplitude. Therefore, any design in the digital domain is a digital filter design. There are broadly two distinct type of filters, finite impulse response (FIR) filter and infinite impulse response (IIR) filter

Digital Filters are based on the common difference equation for Linear Time-Invariant (LTI) – systems:

$$\sum_{m=0}^{N-1} a_m \cdot y[n-m] = \sum_{k=0}^{N-1} b_k \cdot x[n-k]$$

- **y(n) = output signal**
- **x(n) = input signal**
- **a_m, b_k = coefficients**
- **N = number of coefficients (order of system)**

Normalized to a0 = 1 we derive the basic equation in time domain:

$$y(n) = \sum_{k=0}^{N-1} b_k \cdot x[n-k] - \sum_{m=1}^{N-1} a_m \cdot y[n-m]$$

The transfer function of a digital filter of order N in frequency domain is

$$\underline{H}(z) = \frac{\underline{Y}(z)}{\underline{X}(z)} = \frac{\sum_{k=0}^{N-1} b_k z^{-k}}{1 + \sum_{m=1}^{N-1} a_m z^{-m}}$$

A FIR filter is built by using only z^{-1} blocks and gain blocks as shown in figure 7. Here all poles are at z =0 and only the location of zeros can be designed by the choice of the scalar gains b0, b1…. Furthermore FIR filter is an open loop filter. The number of unit delay elements indicates the order of the filter.

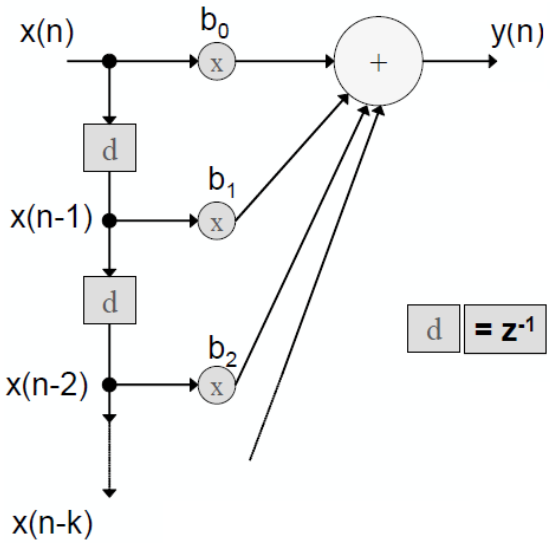

Figure 7.

With an IIR filter both poles and zeros can be designed leading to much better cut-off filters. It can be realized as shown in figure 8. In an IIR filter, the order of the system is the number of poles of the IIR filter

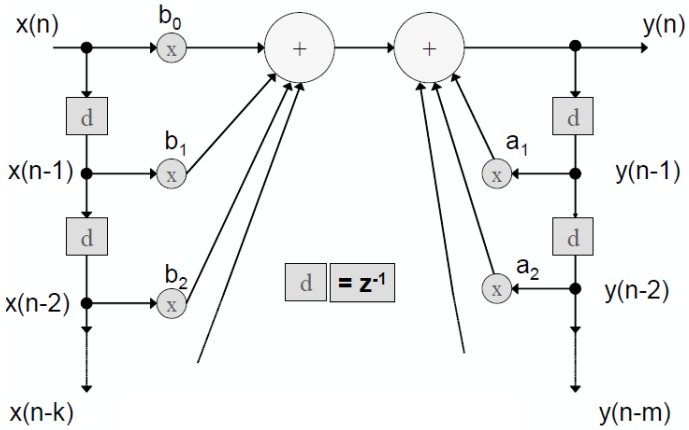

Figure 8.

Digital controllers compensate the error voltage using digital-filter techniques. This enables the compensator to be programmable. It also allows the manufacturer to incorporate a nonlinear response to the error. The required number of poles and zeros in the digital filter depends on the application. For a voltage-mode buck regulator, two zeros are needed to compensate for the second order plant (power stage) and a pole at the origin is needed to minimize steady-state error. Control engineers will recognize this as a proportional, integral, derivative (PID) compensator. The below equation is this two-zero, one-pole filter expressed in the discrete-time, or *z* domain. Here *z*–1 represents a unit-sample delay

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{K_0 + K_1 z^{-1} + K_2 z^{-2}}{1 - z^{-1}}$$

One approach to constructing a digital filter to be used as the compensator is shown in figure 9. Here the multiplication of the error by the numerator-filter coefficients K0, K1 and K2 is done using a table look-up technique. This is the method used by the Texas Instruments UCD9112 digital controller. By using a table for each product in the numerator of the compensator-transfer function, non-linear gains can be built into the table. The down side to this technique is that the tables grow geometrically with increasing dynamic range on the error signal. In the UCD9112 the sampled error signal has a 4-bit range so each table is 16 elements long.

Additional poles can be incorporated into the compensator to shape noise in the compensated error. The addition of a second pole has the effect of smoothing the quantization error in the compensator output. In general, a two-zero/two pole digital filter has the following form given below:

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 - a_1 z^{-1} - a_2 z^{-2}}$$

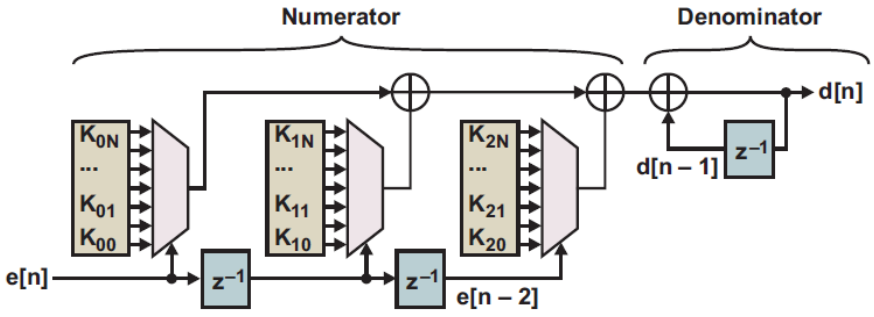

Figure 9.

The discrete-time-domain difference equation resulting from the previous equation is

$$d[n] = b_0 \times e[n] + b_1 \times e[n-1] + b_2 \times e[n-2] - a_1 \times d[n-1] - a_2 \times d[n-2]$$

Expressing the difference equation in this form is called the *direct* form. A direct-form digital filter has a topology that follows this equation as shown in figure 10. The Texas Instruments UCD92xx family of digital-POL controllers uses this filter arrangement for the compensator

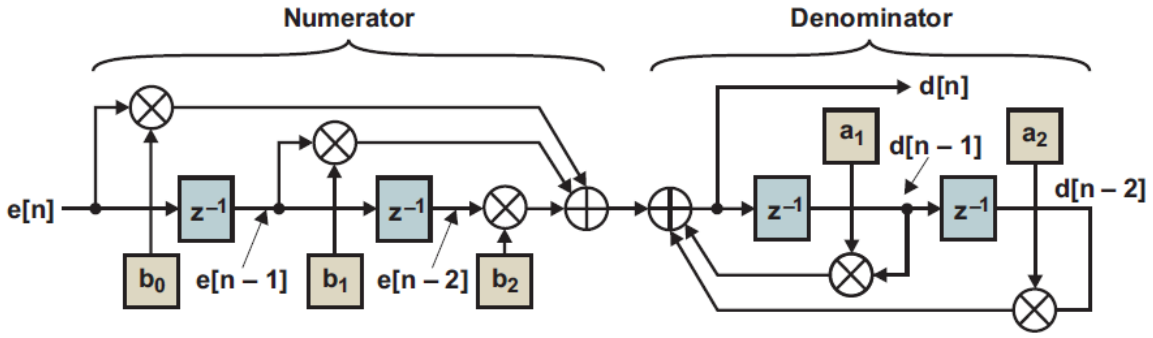

Figure 10.

Finally, the two-pole, two-zero digital filter can be realized as a parallel-filter structure. Some digital controllers use this implementation for the compensator. The classic proportional, integral, derivative (PID) controller is a parallel filter structure. Even if the hardware realization of the filter is not implemented as a PID controller, it is useful to express the filter in this form mathematically

$$G_c(z) = \frac{d(z)}{e(z)} = K_P + K_I \frac{z}{z-1} + K_D \frac{z-1}{z-\alpha}$$

In the above equation we see that a PID compensator is the sum of the voltage error multiplied by a proportional gain, KP, the voltage error multiplied by a integral gain, KI, and accumulated, and the voltage error subtracted from the previous voltage error and multiplied by KD. We can multiply this expression out so that it is expressed as a ratio of polynomials with a common denominator as in below equation to show that the PID controller is an equivalent representation of the direct-form filter

$$G_c(z) = \frac{(K_P + K_I + K_D)z^2 - (K_P(1+\alpha) + K_I\alpha + 2K_D)z + (K_P\alpha + K_D)}{z^2 - (1+\alpha)z + \alpha}$$

In figure 11, dI[n] is the integrator state and represents the average duty cycle for the controlled loop. dD [n] is the derivative state and is zero at steady state. Of the three K gains, KD is the largest and is a function of the location of the zeros in the compensator-transfer function

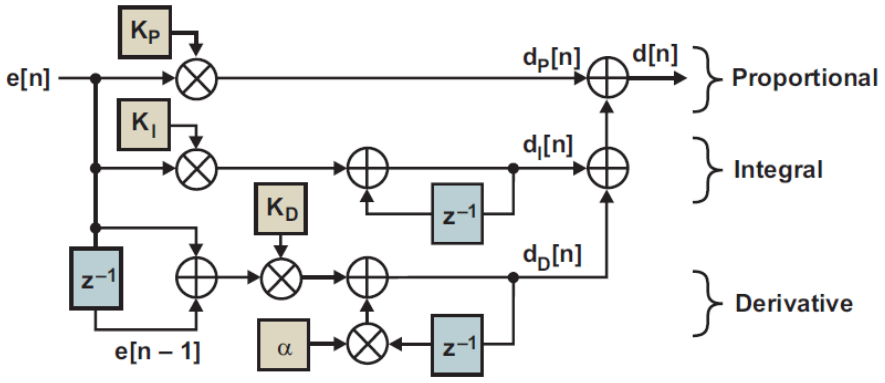

Figure 11.

One of the most straightforward ways to determine what compensation to apply to a SMPS is to express the total open loop gain and plot the magnitude and phase of the loop gain as a Bode plot. From the Bode plot, the stability metrics of phase margin and gain margin can be determined and adjustments to the compensation made until the desired metrics are obtained. Since most power engineers are familiar with the behavior of the total loop gain as the gain and compensating zeros are changed, it is advantageous to first define the compensation as a continuous-time transfer function with specified gain, zeros, and poles. Then this continuous-time transfer function is transformed to the discrete-time domain to determine the discrete filter coefficients. Either of the below two equations can be used to describe the continuous-time prototype controller. If the compensating zeros are complex, the second equation is a more convenient form

$$G_c(s) = K_{DC} \frac{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{s\left(\frac{s}{\omega_{p2}}+1\right)} \qquad G_c(s) = K_{DC} \frac{\frac{s^2}{\omega_r^2}+\frac{s}{\omega_r Q}+1}{s\left(\frac{s}{\omega_{p2}}+1\right)}$$

Once the design parameters of ωr, Q, ωp2 and KDC are determined, the continuous-time transfer function is mapped to the z-domain using the bilinear transformation

$$s = 2f_{sw}\frac{z-1}{z+1}$$

Here fsw is the sampling frequency used by the compensating digital filter. This is typically the switching frequency. This mapping results in the following relationship between the continuous time design parameters and the discrete-filter coefficients

$$b_0 = K_{DC}\left(\frac{\omega_p}{2f_{sw}+\omega_p}\right)\left(\frac{2f_{sw}}{\omega_c^2}+\frac{1}{\omega_c Q}+\frac{1}{2f_{sw}}\right) \qquad a_1 = \frac{-4f_{sw}}{2f_{sw}+\omega_p}$$

$$b_1 = K_{DC}\left(\frac{\omega_p}{2f_{sw}+\omega_p}\right)\left(\frac{-4f_{sw}}{\omega_c^2}+\frac{1}{f_{sw}}\right)$$

$$b_2 = K_{DC}\left(\frac{\omega_p}{2f_{sw}+\omega_p}\right)\left(\frac{2f_{sw}}{\omega_c^2}-\frac{1}{\omega_c Q}+\frac{1}{2f_{sw}}\right) \qquad a_2 = -\omega_p\left(\frac{2f_{sw}-\omega_p}{2f_{sw}+\omega_p}\right)$$

The most basic method of designing the compensator tunes the zeros and poles to obtain the desired bandwidth while maintaining reasonable phase and gain margins (>45° and >10 dB, respectively). However, these criteria may not be sufficient to provide optimal performance

It was earlier mentioned in the introduction that the digital power supply can act as its own network analyzer and also auto-tune its performance based on load conditions. A controller optimized for one set of operating conditions might actually become unstable under other conditions. Real-time system identification and controller auto tuning can fine-tune controller parameters, either during development or in actual operation. The system identification and auto tuning techniques are used in the TI UCD9240 digital controller. The system is perturbed by an excitation signal and then the response to that excitation is measured. The excitation signal can be an impulse, a step, white noise, or a sine wave. Exciting the system by injecting a sine wave into the feedback loop is the technique used by power system/dynamic network analyzers because it produces the highest signal-to-noise measurement of the system-transfer function. The UCD9240 digital controller and its supporting design software use this approach

This technique synthesizes a digital-sinusoidal signal and injects it into the closed-loop system. Then the response to that excitation is measured at another point in the loop. From this measured closed loop response the open-loop gain is calculated. Repeating this over a range of frequencies provides the data necessary to create the Bode plot for the system. Figure 12 shows the location of the injected signal, r[n], and of the measurement point's e[n] and d[n] in the UCD9240

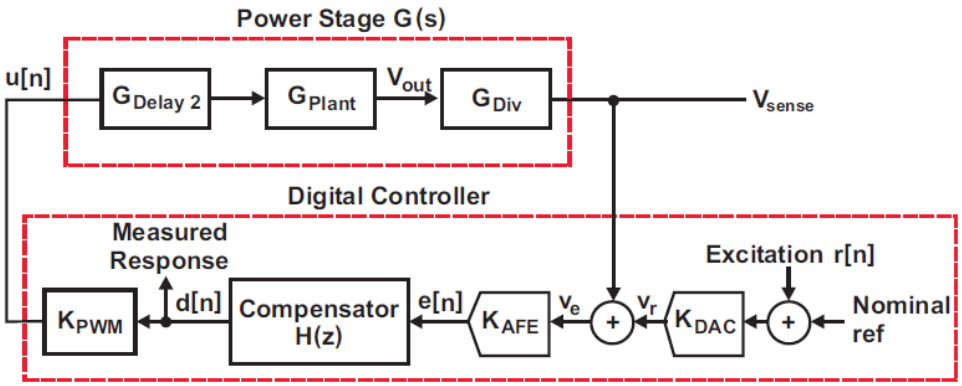

Figure 12.

To generate the excitation signal, a table look-up technique is used. The table contains a sequence for one period of the sine wave and a pointer is stepped through the table at different rates to generate each excitation frequency. To measure the response, the same table is used to generate a cosine and a sine sequence. These two sequences are multiplied by the response vector, d[n], and summed to obtain a complex estimate of the response at the excitation frequency. This is repeated at each frequency for which a measurement is desired. From the complex estimate of the response, we can generate the Bode plot for the system. Because most of the gains in the system are digital—the compensator, the digital PWM, the computational delay, etc.—this technique produces an accurate estimate of the transfer function of the power stage. Then, once we have that estimate, we can use it to make decisions about the optimal compensation of the loop

Traditional controllers usually require redesign or retuning during development to account for wide variations in the power-supply parameters and operating conditions. Most of the well-known digital autos tuning techniques try to shape the frequency response of the closed-loop gain. The controller coefficients are tuned to achieve the desired phase and gain margins and loop bandwidth. These techniques do not guarantee optimal time domain- transient performance. A user interface that can communicate with the digital controller provides an adequate tool for auto tuning. The TI GUI can perform auto tuning based on both the frequency response of the system and the time-domain simulation results. Auto tuning based on frequency response can use the simulation results or the system identification technique previously described. Figure 13 shows the Auto-Tune design screen of the TI GUI for the UCD9240. The auto tuning process uses criteria such as crossover frequency, phase margin, gain margin, DC gain (the loop gain at 10 Hz), and the maximum closed-loop output impedance for frequency-response shaping. The user chooses the desired value and the weight applied to each criterion. The GUI also supports time-domain criteria including settling time, overshoot, and undershoot. The GUI iterates the compensator coefficients to achieve the desired frequency response and time-domain simulation results. After evaluating the results, the user can load the final compensator coefficients into the device register of the UCD9240

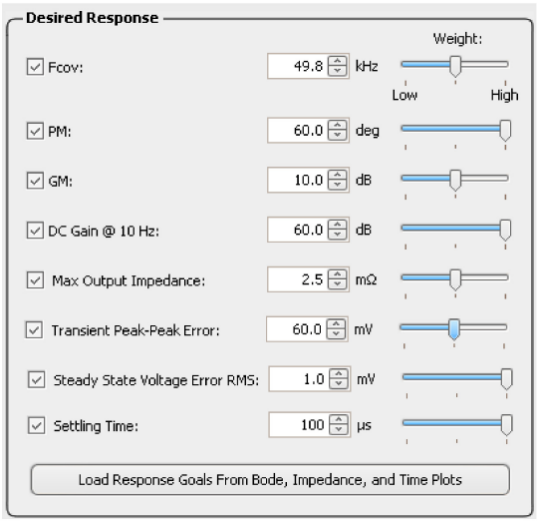

Figure 13.

Figure 14 shows the compensator design window available with the UCD9240. The GUI accepts the compensator coefficients in various forms, including real zeros, complex zeros, or PID coefficients. The user interface calculates the z-domain compensator-transfer function using a bilinear mapping technique. The resulting z-domain transfer function is then applied to the plant transfer function to provide the loop gain.

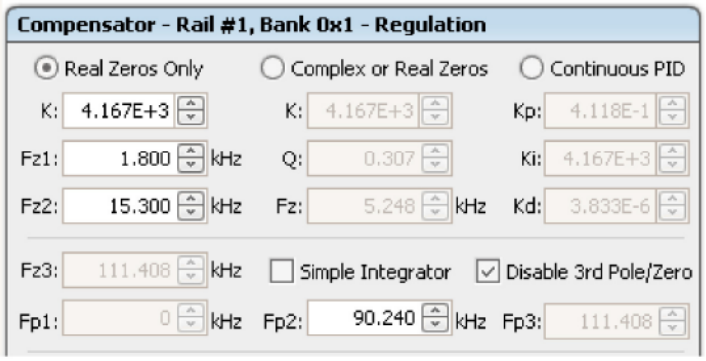

Figure 14.

The UCD9240 implements bit formatting and arithmetic in such a manner that the equivalent gain of the eADC and DPWM equals unity (neglecting the quantization effect on the gain). Therefore, the gain factors for the loop gain are the control-to-output-voltage transfer function of the power stage, Gvd; the output-voltage sense, H; and the compensator, Gc.

5 Mapping Between S-Plane And Z-Plane

The physical system exists in the continuous or analog domain. When expressed in the digital domain with the sampling information incorporated, it would give a better understanding if one is able to relate critical s domain parameter in z domain, The z-plane variable “z”, the s-plane variable “s” and the sampling time T are related by the following relation:

$z = e^{sT}$, S = □ jw $z = e^{\sigma} e^{j\omega T}$

The above equation is of the form $re^{j\theta}$, where r = e^{σ} and q = wT

The Cartesian co-ordinate system is used in s-plane and the polar co-ordinate system is used in z-plane on account of mapping rule

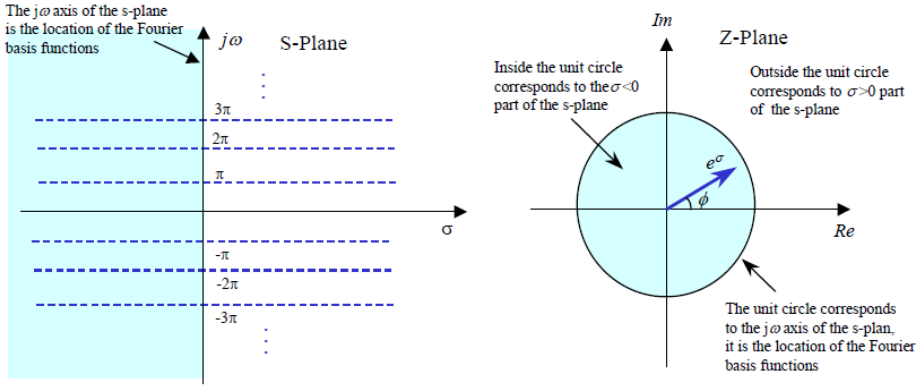

Figure 15.

The whole of the positive real axis maps to the real axis between 1 and infinity in the z-plane. The right half of the s-plane is called the unstable region. It can be shown that the area outside the unit circle in the z-plane is the unstable region. Thus for a discrete system transfer function if the poles and zeros lie inside the unit circle, the system is stable whereas if they’re outside the unit circle, the system is unstable

6 Conclusion

Analog and Digital Controller Performance can be compared as given in table 2:

Table 2.

Control Properties	ANALOG	DIGITAL
Switching frequency (CPU limitations)	+	-
Precision (tolerances, aging, temperature effects, drift, offset, etc.)	-	+
Resolution (numerical problems, quantization, rounding, etc.)	+	-
Bandwidth (sampling loop, ADC – DAC speed)	+	-
Instantaneous over current protection	+	-
Compatibility with power components	+	-
Power requirements	+	-
Communication, data management	-	+
Understanding theory	+	-
Advanced control algorithm (non-linear control, improved transient)	-	+
Multiple loops	-	+
Cost of controller	+	-
Cost of a platform (flexibility, time to market)	-	+
Component count (comparable functionality, integration)	-	+
Reliability	+	?

The digital control loop theory was discussed in detail along with the traditional analog loop comparisons and with this clear understanding we can now design around the digital controllers like the UCD92xx with complete ease and comfort. The references mentioned at the end will further help in understanding the other blocks of a digital power supply and their modeling

7 References

1. Power Electronics Essentials – L Umanand
2. A practical introduction to digital power supply control – Laslo Balogh
3. Designing the Digital Compensator for a UCD91xx-Based Digital Power Supply – Shamim Choudhury
4. Applying Digital Technology to PWM Control-Loop Designs - Mark Hagen and Vahid Yousefzadeh

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