

UCC28722/UCC28720 5W USB BJT Flyback Design Example

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Introduction:

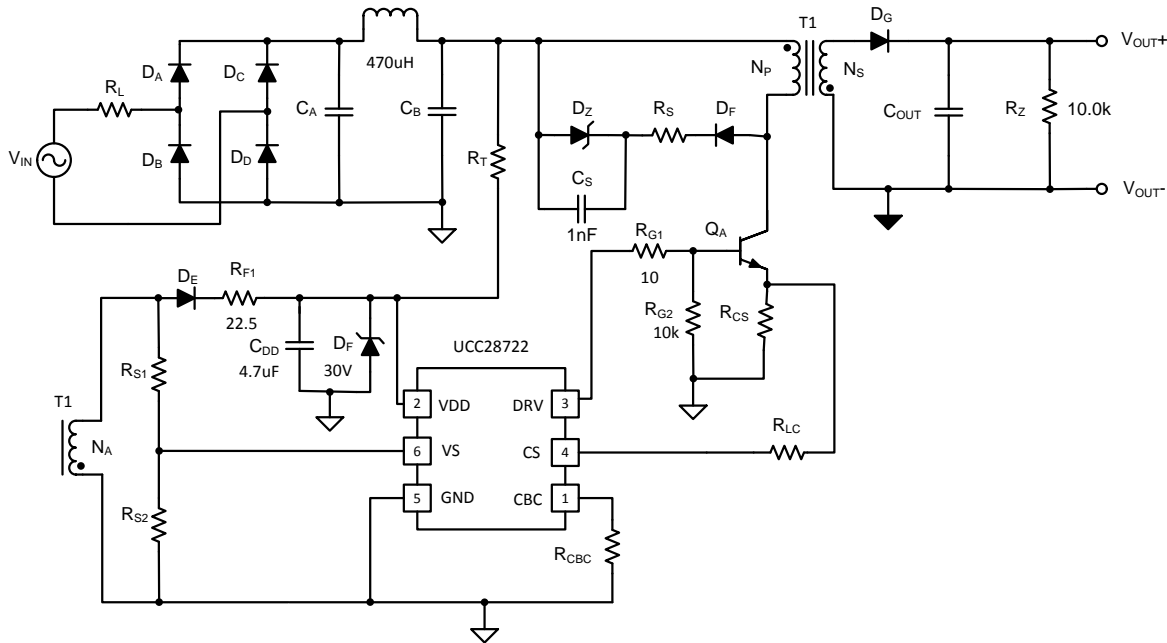
In USB and isolated low power converter designs-quasi resonant and discontinuous conduction mode flyback converter topologies are a popular choice, due to their low parts count and relatively low cost. To reduce the cost even further, TI has developed a quasi-resonant/discontinuous current mode flyback controller with primary-side control. This removes the need for optocoupler and TL431 feedback circuitry reducing the cost of these low power designs even more. The control methodology uses a combination of primary peak current amplitude modulation (AM) and frequency modulation (FM) to regulate the output current and voltage please refer to data sheet [1] for controller details. This design example is a theoretical design that shows how to use the UCC28722 in a 5W USB application. The calculations were used to design the UCC28720EVM-212 reference design [2]. Note the UCC28722 is cost reduced version of the UC28720. To reduce the cost of the UCC28722 the internal startup circuit was removed. This device requires a trickle charge resistor from the bulk input voltage during power up.

Design Specifications:

Description	Minimum	Typical	Maximum	Units
RMS Input Voltage	90 (V_{INMIN})	115/230	265 (V_{INMAX})	V
No Load Input Power			50 (P_{INL})	mW
Output Voltage	4.75	5 (V_{OUT})	5.25	V
Output Voltage Ripple			100 (V_{RIPPLE})	mVpp
Output Load Step (0.1 to 0.6A), (0.6 to 0.1A)	4.1 (V_{OTRM})		6.0	V
Output Current			1 (I_{OUT})	A
Switching Frequency			74 kHz (f_{MAX})	kHz
Full Load Efficiency	73(η)	74		%

Table 1, Design Specifications

Functional Schematic:



Note R_T is not required on UCC28720

Figure 1, UCC28722 5W Offline Flyback Functional Schematic

Selecting R_{CBC} Resistor:

In this design cable compensation was not used and resistor R8 was not populated. Please refer to the data sheet on how to setup cable compensation [1].

Initial Power Budget:

To meet the efficiency (η) goal an initial power loss budget (P_{BUDGET}) needs to be set.

$$P_{OUT} = V_{OUT} \times I_{OUT} = 5V \times 1A = 5W$$

$$P_{BUDGET} = \left(\frac{P_{OUT}}{\eta} \right) - P_{OUT} \approx 1.849W$$

Bridge Rectifier Selection (D_A ..D_D):

For this design a 600V, 0.8A, bridge rectifier from Diodes Incorporated was chosen for the bridge rectifier diode (D_A.. D_D), part number HD06.

$$V_{FDA} = 1V, \text{ forward voltage drop of bridge rectifier diode (} V_{FDA} \text{)}$$

$$I_{DA} = \left(\frac{\frac{P_{OUT}}{\eta}}{V_{INMIN} \frac{2}{\pi} \sqrt{2}} \right) = \frac{5W}{90V \frac{2}{\pi} \sqrt{2}} \approx 85mA, \text{ bridge rectifier average diode current (I}_{DA})$$

$$P_{DA} = V_{FDA} \times I_{DA} = 85mW, \text{ estimate power dissipated in bridge rectifier diode (P}_{DA})$$

Estimate remaining power budget based on bridge rectifier loss.

$$P_{BUDGET} = P_{BUDGET} - 2 \times P_{DA} \approx 1.68W$$

Transformer Calculations (T1):

Transformer demagnetizing duty cycle (D_{MAG}) is fixed to 42.5% based on the UCC28720/2 control law methodology [1].

$$D_{MAG} = 0.425$$

T_R is the estimated period of the LC resonant frequency at the switch node.

$$T_R = 2\mu s$$

Calculate maximum duty cycle (D_{MAX}):

$$D_{MAX} = 1 - D_{MAG} - f_{MAX} \frac{T_R}{2} = 1 - 0.425 - 74kHz \frac{2\mu s}{2} = 0.501$$

Calculate transformer primary peak current (I_{PPK}) based on a minimum flyback input voltage. This calculation includes a factor of 0.6 to account for the reduction in flyback input voltage caused by the ripple voltage across the input capacitors (C_A and C_B).

$$I_{PPK} = \frac{2 \times P_{OUT}}{\eta \times V_{INMIN} \sqrt{2} \times 0.6 \times D_{MAX}} = \frac{2 \times 5W}{0.75 \times 90V \sqrt{2} \times 0.6 \times 0.47} = 358mA$$

Selected primary magnetizing inductance (L_{PM}) based on minimum flyback input voltage, transformer, primary peak current, efficiency and maximum switching frequency (f_{MAX}).

$$L_{PM} = \frac{\frac{2 \times P_{OUT}}{\eta}}{I_{PPK}^2 \times f_{MAX}} = \frac{2 \times 5W}{(350mA)^2 \times 74kHz} \approx 1.44mH$$

$V_{QA_CE(SAT)} = 1V$, estimated voltage drop across transistor during conduction

$V_{RCS} = 0.78V$, voltage drop across current sense resistor

$V_{DG} = 0.6V$, estimated forward voltage drop across output diode

Calculate transformer turns ratio primary to secondary (a_1) based on volt-second balance.
Note in the following equation L_{SM} is secondary magnetizing inductance.

$$a_1 = \frac{N_P}{N_S} = \sqrt{\frac{L_{PM}}{L_{SM}}} = \frac{D_{MAX} \times (V_{INMIN} \sqrt{2} \times 0.6 - V_{QA_CE(SAT)} - V_{RCS})}{D_{MAG} \times (V_{OUT} + V_{DG})} \approx 15.7$$

$V_{DDMIN(on)} = 8.15V$, UCC28722 minimum VDD voltage before UVLO turnoff.

$V_{DE} = 0.6V$, estimated auxiliary diode forward voltage drop

$V_{OUT_INIT} = 2V$, Minimum voltage on the output when adapter is connected to a device with a depleted battery.

Calculate transformer auxiliary to secondary turns ratio (a_2)

$$a_2 = \frac{N_A}{N_S} = \frac{V_{DDMIN} + V_{DE}}{V_{OUT_INIT} + V_{DG}} \approx 3.37$$

Transformer primary RMS current (I_{PRMS})

$$I_{PRMS} = I_{PPK} \sqrt{\frac{D_{MAX}}{3}} = 146mA$$

Transformer secondary peak current RMS current (I_{SPK})

$$I_{SPK} = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} \approx 4.71A$$

Transformer secondary RMS current (I_{SRMS})

$$I_{SRMS} = I_{SPK} \sqrt{\frac{D_{MAG}}{3}} \approx 1.77A, \text{ transformer secondary RMS current}$$

Estimate power dissipated by the UCC28722 IC (P_{IC})

$$V_{DD} = V_{OUT} \times a_2 \approx 16.83V, \text{ Estimated } V_{DD}$$

$$I_{RUN} = 2mA, \text{ Typical IC run current}$$

$$I_{DRS(MAX)} = 37mA, \text{ Average Maximum Drive Current}$$

$$I_{DRS(MIN)} = 19mA, \text{ Average Minimum Drive Current}$$

$$I_{DRS(AVG)} = \frac{I_{DRS(MAX)} + I_{DRS(MIN)}}{2} \times D_{MAX} = 14mA, \text{ Average Base Drive Current}$$

$$P_{IC} = V_{DD} (I_{RUN} + I_{DRS(AVG)}) \approx 270mW$$

Calculate auxiliary winding peak current (I_{APK})

$$I_{APK} = \frac{P_{IC} \times 2}{(V_{OUT} + V_{DE}) \times a_2 \times D_{MAG}} = 67mA$$

Calculate auxiliary winding RMS current (I_{ARMS})

$$I_{ARMS} = I_{APK} \sqrt{\frac{D_{MAG}}{3}} \approx 25mA$$

For this transformer we allow for 3% efficiency loss from the transformer (P_{T1})

$$P_{T1} = P_{OUT} \times 0.03 = 150mW$$

Recalculate remaining power budget

$$P_{BUDGET} = P_{BUDGET} - P_{T1} \approx 1.26W$$

A Würth Electronik transformer was designed for this application, part number 7508110151, which has the following specifications:

$$a_1 = 15.42$$

$$a_2 = 3.2$$

$$L_{PM} = 1.5mH$$

$$L_{LK} = 20\mu H, \text{ primary leakage inductance}$$

Input Capacitor Selection ($C_{IN} = C_A + C_B$):

Calculate input capacitor charge time (t_{CH}) based on 40% input capacitor ripple voltage.

$$t_{CH} = \frac{1 - \sin^{-1}\left(\frac{V_{INMIN}\sqrt{2} - V_{INMIN}\sqrt{2} \times 0.6}{V_{INMIN}\sqrt{2}}\right)}{4 \times 47Hz} = 3.4ms$$

Calculate flyback average primary current (I_{PT1}) during input capacitor discharge.

$$I_{PT1} = \frac{\frac{P_{OUT}}{\eta \times V_{INMIN}\sqrt{2}} + \frac{P_{OUT}}{\eta \times V_{INMIN}\sqrt{2} \times 0.6}}{2} = 72mA$$

Calculate total input capacitance (C_{IN}) based on minimum flyback input voltage and 40% ripple voltage across the input capacitor.

$$T_{RL} = \frac{1}{2 \times 47Hz} \approx 11ms, \text{ longest period of the rectified line voltage}$$

$$V_{INRIPPLE} = V_{INMIN} \times \sqrt{2} \times 0.4 \approx 50.9V, \text{ input ripple to the flyback converter}$$

$$C_{IN} = \frac{I_{PT1}(T_{RL} - t_{CH})}{V_{INRIPPLE}} \approx 10\mu F$$

$$C_A = C_B = \frac{C_{IN}}{2} = 5\mu F$$

Calculate input capacitor (C_A) RMS current (I_{C_ARMS}) based on 40% input capacitor ripple voltage.

$$I_{CINP} = \frac{2 \times (C_A + C_B) \times V_{INMIN} \sqrt{2} \times 0.4}{t_{CH}} \approx 311mA, \text{ peak input capacitor charge current (} I_{CINP} \text{)}$$

$$I_{CA_RMS} = \sqrt{\left(\frac{I_{CINP}}{2} \sqrt{\frac{t_{CH}}{3 \times T_{RL}}} \right)^2 + \left(\frac{I_{CINP}}{2} \sqrt{\frac{T_{RL} - t_{CH}}{3 \times T_{RL}}} \right)^2 - \left(\frac{I_{PT1}}{2} \right)^2} \approx 82mA$$

Estimate of capacitor C_B 's low frequency ($1/T_{RL}$) RMS current (I_{CB_LFRMS})

$$I_{CB_LFRMS} = I_{CA_RMS}$$

Estimate of C_B 's high frequency RMS current (I_{CB_HFRMS})

$$I_{CB_HFRMS} = \sqrt{\left(I_{PPK} \sqrt{\frac{D_{MAX}}{3}} \right)^2 - \left(I_{PPK} \frac{D_{MAX}}{2} \right)^2} \approx 116mA$$

Estimate of C_B 's total RMS current (I_{CB_RMS})

$$I_{CB_RMS} = \sqrt{\left(I_{CB_LFRMS} \right)^2 + \left(I_{CB_HFRMS} \right)^2} \approx 142mA$$

For this design 4.7uF, 400V electrolytic capacitors, from Nichicon part number UVR2G4R7MPD were chosen for the design.

$$C_A = C_B = 4.7\mu F$$

These capacitors had a measured ESR of 5 ohms at 74 kHz

$$ESR_{CA} = ESR_{CB} = 5\Omega$$

Recalculate remaining power budget based on power dissipation by the ESRs in the input capacitors.

$$P_{BUDGET} = P_{BUDGET} - \left(I_{CA_RMS} \right)^2 \times ESR_{CA} - \left(I_{CB_RMS} \right)^2 \times ESR_{CB} \approx 1.126W$$

Filter Inductor (L_A):

Filter inductor (L_A) is used for EMI filtering. In this design it is just a place holder and the design has not been optimized for EMI. 470uH inductor from Bourns was chosen, part number RLB0608-471KL. This inductor has a DCR of 6.5 ohms.

$$DCR = 6.5\Omega$$

Recalculate power budget based on DCR losses

$$P_{BUDGET} = P_{BUDGET} - (I_{PRMS})^2 \times DCR \approx 0.987W$$

Fusible Resistor (R_L):

To limit the inrush current during power and for safety a 10 ohm, 3W fusible resistor from Bourn, part number PWR4522AS10R0JA was placed at the input of this design.

$$R_L = 10\Omega$$

Recalculate power budget based on estimated R_L losses

$$P_{BUDGET} = P_{BUDGET} - \left(\frac{P_{OUT}}{V_{INMIN} \times \eta} \right)^2 \times R_L \approx 0.929W$$

Current Sense Resistor (R_{CS}):

For this design 2.15 ohm resistor was selected based on a nominal maximum current sense signal of 0.78V.

$$R_{CS} = \frac{0.78V}{I_{PPK}} = 2.2\Omega \approx 2.15ohm$$

$$P_{RCS} = (I_{PRMS})^2 \times R_{CS} = 46mW, \text{ nominal current sense resistor power dissipation}$$

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{RCS} \approx 0.883W$$

Select Output Diode (D_G):

Calculate diode reverse voltage (V_{RDG})

$$V_{RDG} = V_{OUT} + V_{INMAX} \sqrt{2} \frac{1}{a_1} \approx 29.3V$$

Calculate peak output diode (I_{DGPK})

$$I_{DGPK} = I_{SPK} = 4.7A$$

For this design we selected a 3A, 40V schottky rectifier with a forward voltage drop (V_{FDG}) of 0.31V.

$$V_{FDG} = 0.31V$$

Estimated diode power loss (P_{DG})

$$P_{DG} = \frac{P_{OUT} \times V_{FDG}}{V_{OUT}} \approx 310mW$$

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{DG} \approx 573mW$$

Select Output Capacitors (C_{OUT}):

Select output ESR based on 90% of the allowable output ripple voltage

$$ESR_{COUT} = \frac{V_{RIPPLE} \times 0.9}{I_{SPK}} = \frac{100mV \times 0.9}{4.7A} = 19m\Omega$$

For this design the output capacitor (C_{OUT}) was selected to prevent V_{OUT} from dropping below the minimum output voltage during transients (V_{OTRM}).

$$V_{OTRM} = 4.1V$$

$$C_{OUT} \geq \frac{2ms \times \frac{P_{OUT}}{V_{OUT} \times 2}}{V_{OUT} - V_{OTRM}} = 1.1mF$$

For this design example two 680uF capacitors were selected in parallel on the output, with an ESR of 7 mΩ each.

$$C_{OUT} = 2 \times 680uF = 1.36mF$$

$$ESR_{COUT} = \frac{7m\Omega}{2} = 3.5m\Omega$$

Estimate total output capacitor RMS current (I_{COUT_RMS})

$$I_{COUT_RMS} = \sqrt{\left[\frac{I_{SPK} \times \sqrt{D_{MAG}}}{\sqrt{3}} \right]^2 - \left(\frac{P_{OUT}}{V_{OUT}} \right)^2} \approx 1.46A$$

Estimate total output capacitor loss (P_{COUT})

$$P_{COUT} = (I_{COUT_RMS})^2 \times ESR_{COUT} \approx 7.5mW$$

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{COUT} \approx 565mW$$

Select BJT Q_A:

For this design we had chosen 800V 1A transistor with the following characteristics:

$$V_{CE(sat)} = 0.6V, \text{ Transistor Collector Emitter Saturation}$$

$$V_{BE(sat)} = 0.6V, \text{ Base Emitter Saturation}$$

$$t_r = 140ns, \text{ Estimated collector rise time}$$

Estimate transistor losses (P_{QA}):

$$V_{FLY} = V_{INMIN} \times \sqrt{2} - \frac{V_{INRIPPLE}}{2} - 2 \times V_{FDA} \approx 99.8V, \text{ Average Minimum Input Voltage}$$

$$I_{DRS(AVG)} = \frac{D_{MAX} (I_{DRS(MIN)} + I_{DRS(MAX)})}{2} = 14mA, \text{ Average Base Drive Current}$$

$$I_{CE(AVG)} = \frac{I_{PPK} \times D_{MAX}}{2} = 90mA, \text{ Average Collector Emitter Current}$$

$$P_{QA} = I_{DRS(AVG)} \times V_{BE(SAT)} + I_{CE(AVG)} \times V_{CE(SAT)} + I_{PPK} \times \frac{(V_{FLY} + (V_{OUT} - V_{DG})a1)}{2} \times t_r \times f_{MAX} = 373mW$$

Recalculate the power budget

$$P_{BUDGET} = P_{BUDGET} - P_{QA} \approx 192mW$$

Setup Zener Clamp to Protect FET Q_A:

$$V_Z = 82V, \text{ Zener Clamp Voltage (D}_Z\text{)}$$

$$V_{CE_MAX} = 800V, \text{ FET maximum drain to source voltage}$$

$$V_{CLAMP} = V_{CE_MAX} \times 0.9 - V_{INMAX} \sqrt{2} \approx 345.2V, \text{ Available Clamp Voltage to Protect FET Q}_A$$

$$R_S = \frac{V_{CLAMP} - 0.6 - V_Z}{I_{PPK}} \approx 734\Omega$$

Select a standard resistor for the design.

$$R_S = 750\Omega$$

Estimate Zener Clamp/L_{LK} power dissipation (P_{LLK})

$$P_{LLK} = \frac{L_{LPK} \times (I_{PPK})^2 \times f_{MAX}}{2} = 95mW$$

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{LLK} \approx 97mW$$

Trickle Charge Resistor (R_T):

To reduce no load power losses R_T and to keep no load power to a minimum, three 1.47MΩ are used in series for R_T

$$R_T = 1.47M\Omega \times 3 = 4.41M\Omega$$

$$P_{RT} = \frac{(V_{INMAX} \sqrt{2})^2}{R_T} \approx 32mW, \text{ Total trickle charge resistor power dissipation}$$

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{RT} \approx 65mW$$

VDD Capacitor Selection (C_{DD}):

$$V_{VDD(ON)} = 21V, \text{ Typical VDD turn-on threshold}$$

$$V_{VDD(OFF)} = 7.7V, \text{ Typical VDD turnoff threshold}$$

$$C_{DD} = \frac{(I_{DRS(AVG)} + I_{RUN}) \times C_{OUT} \times V_{OUT_INIT}}{(V_{VDD(ON)} - V_{VDD(OFF)}) \times I_{OUT}} \approx 3.3\mu F$$

Select standard capacitor value for the design

$$C_{DD} \approx 4.7\mu F$$

Note after C_{DD} has been charged up to the device turn on threshold ($V_{VDD(on)}$), the UCC28722 will initiate three small gate drive pulses (DRV) and start sensing current and voltage. (Please refer to figure 2) If a fault is detected such as an input under voltage or any other fault, the UCC28722 will terminate the gate drive pulses and discharge C_{DD} to initiate an under voltage lockout. This capacitor will be discharged with the run current of the UCC28722 (I_{RUN}) until the V_{DD} turnoff ($V_{VDD(off)}$) threshold is reached. Note the C_{DD} discharge time (t_{CDD}) from this forced soft start can be calculated knowing the controller run current (I_{RUN}) without out gate driver switching and the controller's VDD turnoff threshold ($V_{VDD(off)}$) and the following equations. If no fault is detected, the UCC28722 will continue driving Q_A and controlling the input and output currents and a soft start will not be initiated.

$$t_{CDD} = C_{DD} \frac{V_{VDD(on)} - V_{VDD(off)}}{\left(\frac{V_{INMAX} \sqrt{2}}{R_T} - I_{RUN} \right)} = 33ms, \text{ Discharge for soft start Reset}$$

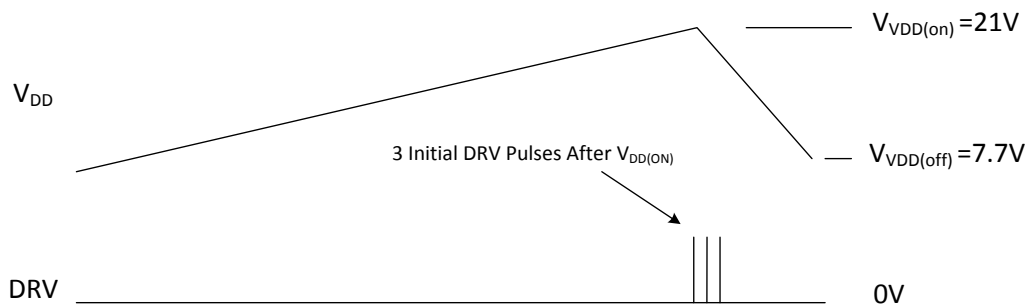


Figure 2, VDD and DRV at Startup with Fault

Select VS voltage divider (R_{S1} , R_{S2}):

$$I_{VSL(run)} = 225\mu A \text{ VS Line-sense run current}$$

Note R_{S1} so the converter will go into under voltage lockout when the input is below 80% of the minimum specified input voltage.

$$R_{S1} = \frac{\frac{a_2}{a_1} V_{INMIN} \sqrt{2} \times 0.8}{I_{VSL(run)}} \approx 93.9k\Omega$$

Select a standard resistor for the design

$$R_{S1} = 82.5k\Omega$$

Calculate R_{S2}

$$R_{S2} = \frac{4V}{\frac{(V_{OUT} + V_{DG}) \times a_2 - 4V}{R_{S1}}} \approx 23.7k\Omega$$

Select a standard resistor for the design

$$R_{S2} = 27.4k\Omega$$

Calculate VS divider power dissipation (P_{VS})

$$P_{VS} = \frac{(\sqrt{D_{MAX}} (V_{OUT} + V_{DG}) a_2)^2}{(R_{S1} + R_{S2})} \approx 1.2mW$$

Select auxiliary diode (D_E) for this design that had a forward voltage drop (V_{DE}) of 0.6V.

$$V_{DE} = 0.6V$$

$$V_{DD} = (V_{OUT} + V_{DG}) \times a_2 - V_{DE} \approx 17.3V, \text{ UCC28700 supply voltage at } V_{DD}$$

$$V_{RDE} = V_{DD} + V_{INMAX} \sqrt{2} \times \frac{a_2}{a_1} \approx 95V, \text{ maximum reverse voltage across } V_{DE}$$

Calculate D_E power dissipation (P_{DE})

$$P_{DE} = (I_{RUN} + I_{DRS(AVG)}) \times V_{DE} \approx 9.6mW$$

Recalculated power budget

$$P_{BUDGET} = P_{BUDGET} - P_{VS} - P_{DE} \approx 54mW$$

Preload Resistor Selection (R_Z):

To keep the output voltage from climbing at no load a pre-load resistor is required. This is generally a trial and error process. For this design the preload resistor that kept the output regulated under no load conditions was 10 k Ω .

$$R_Z = 10.0K$$

Calculate R_Z power dissipation (P_{RZ})

$$P_{RZ} = \frac{(V_{OUT})^2}{R_Z} \approx 2.5mW$$

Recalculated power budget and there is 52 mW of margin left in the power budget to meet the efficiency requirements of the design. Note in production designs, more margin might be required. Also note these calculations are estimations and the final design may need to be adjusted to hit efficiency requirements and regulation requirements.

$$P_{BUDGET} = P_{BUDGET} - P_{RZ} \approx 52mW$$

Internal Blanking

The UCC28722 controller regulates the output voltage by sensing the auxiliary (Aux) winding. This removes the need for opto isolator feedback scheme reducing the cost of the design. However, this voltage control feedback scheme is susceptible to leakage spikes at the switch node that occur in most flyback converters. This signal is coupled through the turns ratio of the transformer (T1) and shows up on the Aux winding during t_{LK_RESET} , please refer to figure 3 for details.

To help insure the leakage spike on the Aux winding does not cause a control issue the UCC28720/22 blanks (t_B) the Aux signal to the controller for 600 ns to 2.2 us depending on loading. Please see the data sheet details [1]. **Note the ringing on the auxiliary winding needs to be less than 100mV peak to peak after t_B . Snubbing circuitry on the secondary and/or auxiliary winding may be required to reduce ringing.**

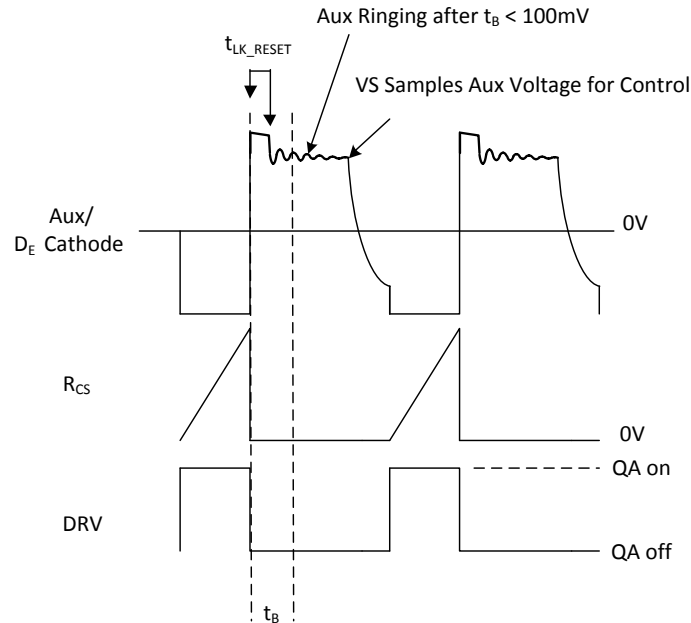


Figure 3, Auxiliary Winding VS Blanking

To ensure the leakage spike does not cause control issues it needs to be dissipated before the Aux blanking (t_B) has terminated. The tank frequency (f_{LC}) between the switch node capacitance (C_{SWN}) and the transformer leakage inductance (L_{LK}) should be greater than 1MHz.

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{LK} \times C_{SWN}}}$$

$$f_{LC} \geq \frac{1}{2 \times 500ns} = 1MHz$$

Select line compensation resistor R_{LC} :

Resistor R_{LC} provides offset to the peak current comparator input (CS). R_{LC} is adjusted to terminate the gate drive signal (B) early to prevent primary current (A) from over shooting [1]. Please refer to figures 4 and 5 for details.

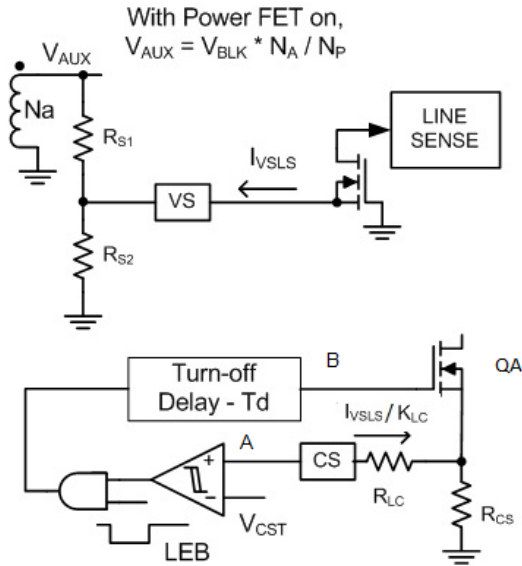


Figure 4, Peak Current Limit Comparator

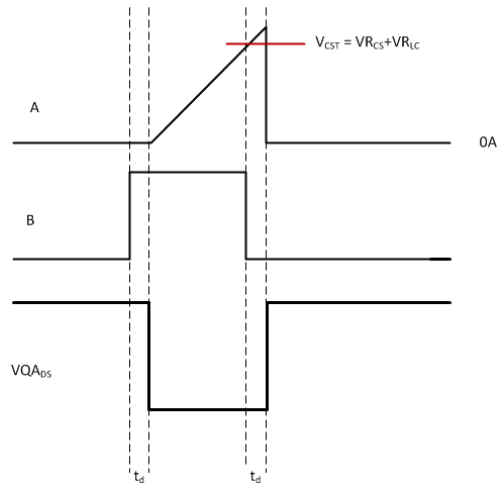


Figure 5, CS(A), Q_{A_g} (B), $V_{QA_{DS}}$ Signals

$$K_{LC} = 25, \text{ Line Compensating Ratio [1]}$$

Calculate R_{LC} initial resistor setting based on $Q_{A_{DS}}$ rise and fall time (t_r)

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_r \times a1}{L_{PM}} \approx 6.3k\Omega, \text{ Starting Point for } R_{LC}$$

In circuit adjust R_{LC} so the maximum output current is (I_{OUT}). For this design RLC was set to 1 k Ω .

$$R_{LC} = 1k\Omega$$

Estimate no load input power (P_{NL}):

$f_{MIN} = 650Hz$, Minimum operating frequency

$I_{WAIT} = 95\mu A$, VDD input current at 1 kHz operating frequency [1]

$$P_{VDD} = I_{WAIT} \times V_{DD} + \frac{(I_{DRS(max)} + I_{DRS(min)}) \times V_{DD}}{2} \times \frac{f_{MIN}}{f_{MAX}} \approx 5.9mW, \text{ Estimated UCC28722 power dissipation}$$

Estimate switching losses (P_{SWFM}) at high line at f_{MIN}

$$P_{SWFM} = [V_{INMAX} - (V_{OUT} - V_{VDG}) \times a1] \times \frac{I_{PPK}}{3} \times t_r \times f_{MIN} \approx 1.6mW$$

$$P_{LLK} = \frac{L_{LPK} \times \left(\frac{I_{PPK}}{3}\right)^2}{2} \times f_{MIN} \approx 92\mu W, \text{ estimate of leakage power dissipation at no load}$$

The estimated no load input power (P_{NL}) is roughly 42 mW.

$$P_{NL} = P_{VDD} + P_{SWFM} + P_{RZ} + P_{RT} + P_{LLK} \approx 42mW$$

5W EVM Schematic:

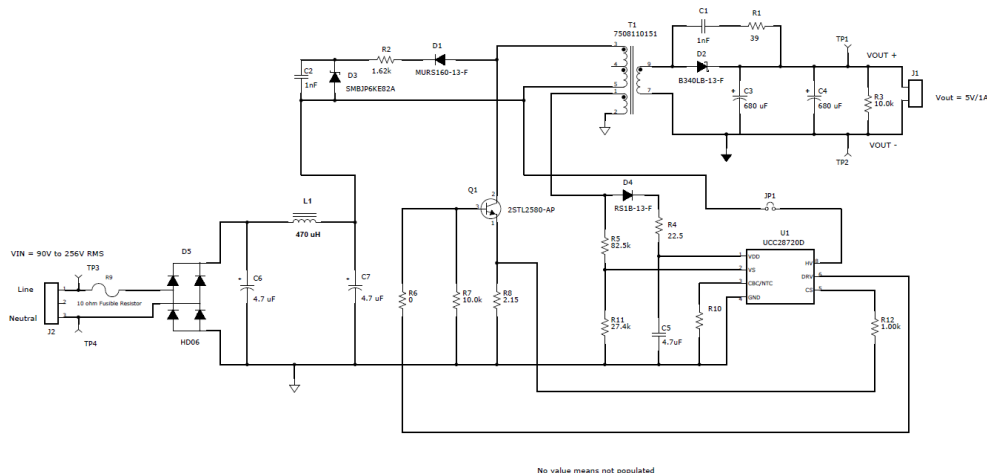


Figure 6, UCC28720EVM-212 Schematic

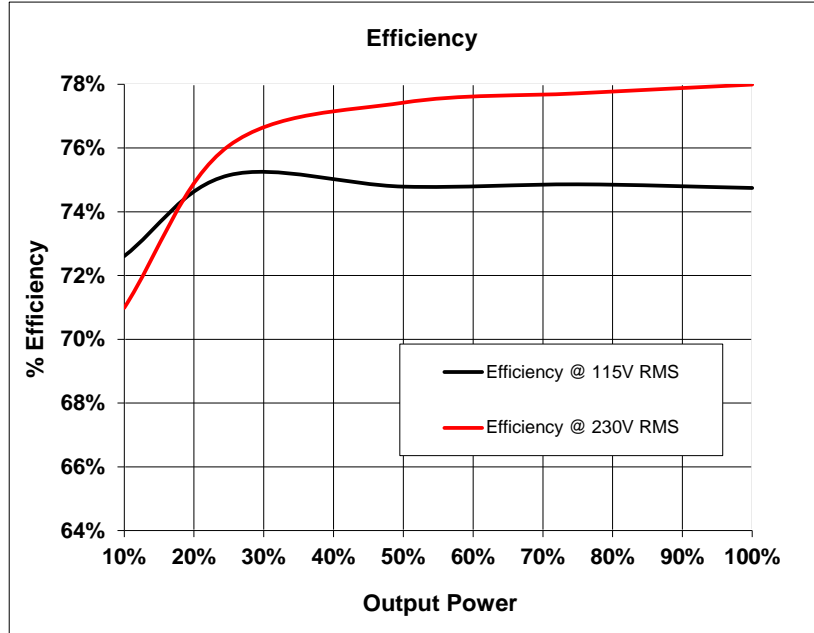


Figure 7, Efficiency

REFERENCES

- [1] UCC28722 Data Sheet, Constant-Voltage, Constant-Current Controller with Primary Side Regulation, SLUSBL7, December 2013, <http://www.ti.com/lit/gpn/ucc28722>
- [2] Using the UCC28722EVM-212, UCC28700EVM-212 5W USB Adapter, SLUU968, July 2012, <http://www.ti.com/litv/pdf/sluaa92>

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