

# HotRod QFN Package PCB Attachment

Stefan (Włoddek) Wiktor

## ABSTRACT

HotRod Quad flatpack No Leads (QFN) are leadless packages specifically designed for power applications. The small footprint, standard QFN pitch, low parasitics along with high current capability of these packages are ideal for power converters application. The electrical connections are made via lands on the bottom side of the component to the surface of the connecting substrate (PCB). This application report presents users with information about attaching HotRod QFN devices to the printed circuit boards.

## 1 Introduction

Quad flat no leads (QFNs) HotRod is a thermally enhanced plastic package that uses new copper leadframe technology. It eliminates power device wire bonds by attaching the power device and/or die directly to the leadframe. This construction results in a cost effective advanced packaging that improves electrical and thermal performance over traditional leaded packages. The HotRod QFN also improves the application efficiency by eliminating wire bonds connection between the die and the leadframe and minimizes the package parasitic.

HotRod QFNs have solder lands on all sides as well as power buses for enhanced current charging capability. HotRod QFNs are available in number of formats and sizes. The package is molded and mechanically singulated from a matrix of leadframes. Package size is determined by the encapsulated die size, and number of signal pins.

**NOTE:** This HotRod QFN PCB application report provides general guidelines. Precise process development and experimentation are needed to optimize the specific application needs and performance.

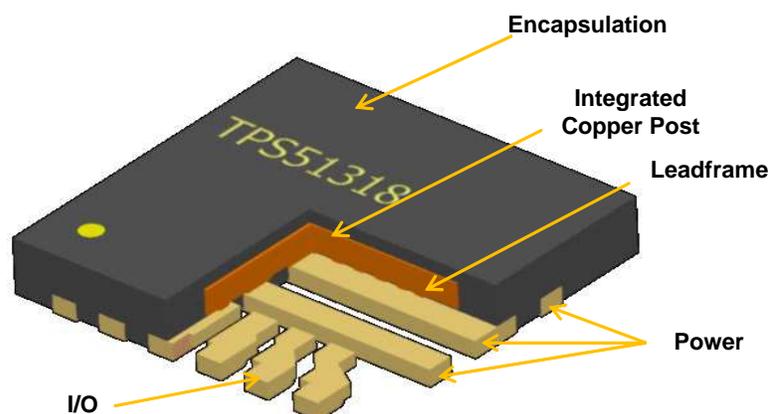


Figure 1. HotRod QFN Structure And Die Attachment

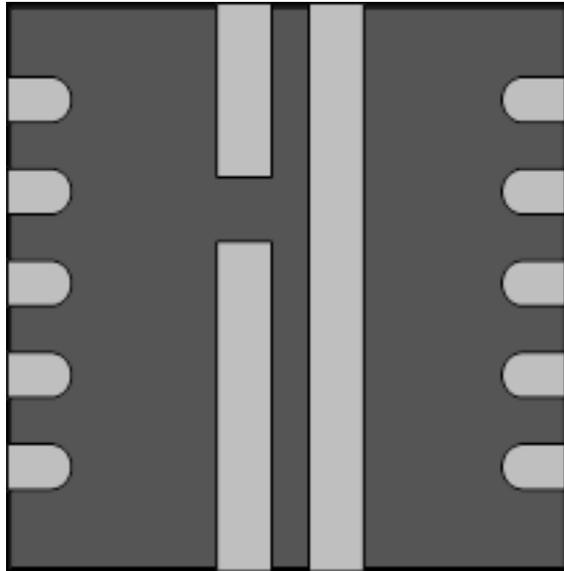


Figure 2. Package Outline

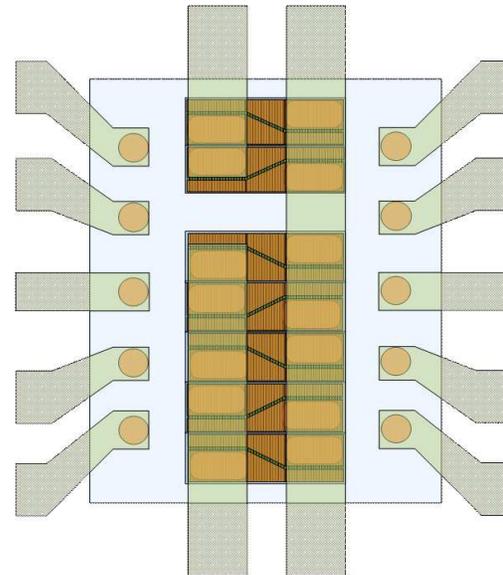


Figure 3. Die to Leadframe Interface

## 2 Manufacturing Consideration

### 2.1 SMT Process

Many factors contribute to a high-yielding assembly process. [Table 1](#) highlights the key elements of SMT process.

Table 1. SMT Essentials

SMT ESSENTIAL	DESCRIPTION
Solder paste quality	Uniform viscosity and texture. Free from foreign materials. Solder paste must be used before the expiration date. Shipment and storage temperature must be maintained at the proper level. Paste must be protected from drying out on the solder stencil.
PCB quality	HotRod QFN is intended for power application and copper thickness of between 2 oz. and 3 oz. is recommended for the best electrical performance. The plated solder land area must be clean and flat. The attachment surface must be clean and free of solder-mask residue.
Placement accuracy	Tight tolerances are not required. The QFN package self-aligns as long as the major portion of the leadframe is in contact with the solder paste covering the land areas on the board. Use the alignment marks on the PCB are to help verify correct placement of parts.
Solder reflow profile	The solder reflow temperature is dependent on the PCB design, PCB thickness and the peak reflow temperature according to the moisture sensitivity level (MSL) of components and the recommended profile of the solder paste being used. A reflow profile must be developed for each PCB type and HotRod QFN packages.
Solder volume	Solder volume is important to ensure optimum contact of all intended solder connections.

### 3 Stencil Vitals

Ti recommends stencil manufacturing by either, laser cut, electro polished or electroform.

#### 3.1 Solder Paste

Ti recommends the use of type 3 solder paste when mounting HotRod QFN parts. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder to the PCB land
- The adhesive properties of the paste hold the component in place during reflow
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the *No Clean flux* composition are preferred due to the difficulty in cleaning under the mounted components

The HotRod QFN series packages do not require underfill to be utilized.

Ti recommends controlled placement pressure in mounting the HotRod packages. Recommended force should be controlled to a 5-N maximum for static and a 2.5-N maximum for impact.

### 4 Printed Circuit Board (PCB) Design Guidelines

One of the key components in implementing HotRod QFN package on a substrate is the design of the land pads. The QFN has lead fingers exposed on the bottom side of the package. Electrical, thermal and mechanical connections between the component and motherboard can be made by soldering the part using screen printed solder paste and reflowing after placement. To ensure consistent solder joint geometries, it is critical to design the land pattern consistent with the exposed leadframe pattern.

#### 4.1 Land Pad Style

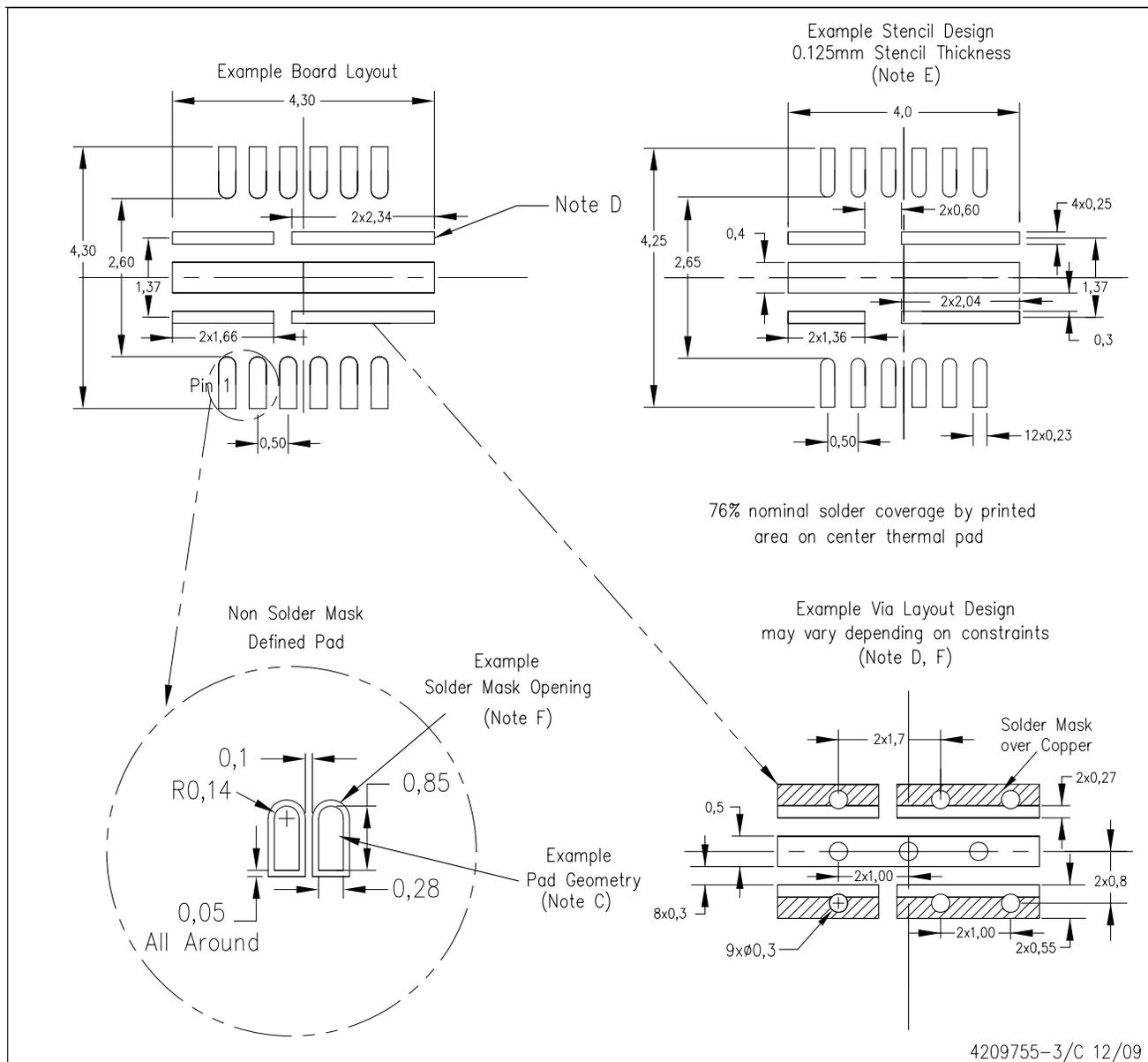
There are two basic designs for PCB land pads for the HotRod QFN package

- the copper defined or non-solder mask defined style (NSMD)
- and the solder mask defined style (SMD)

Either style is acceptable for use with the HotRod QFN package.

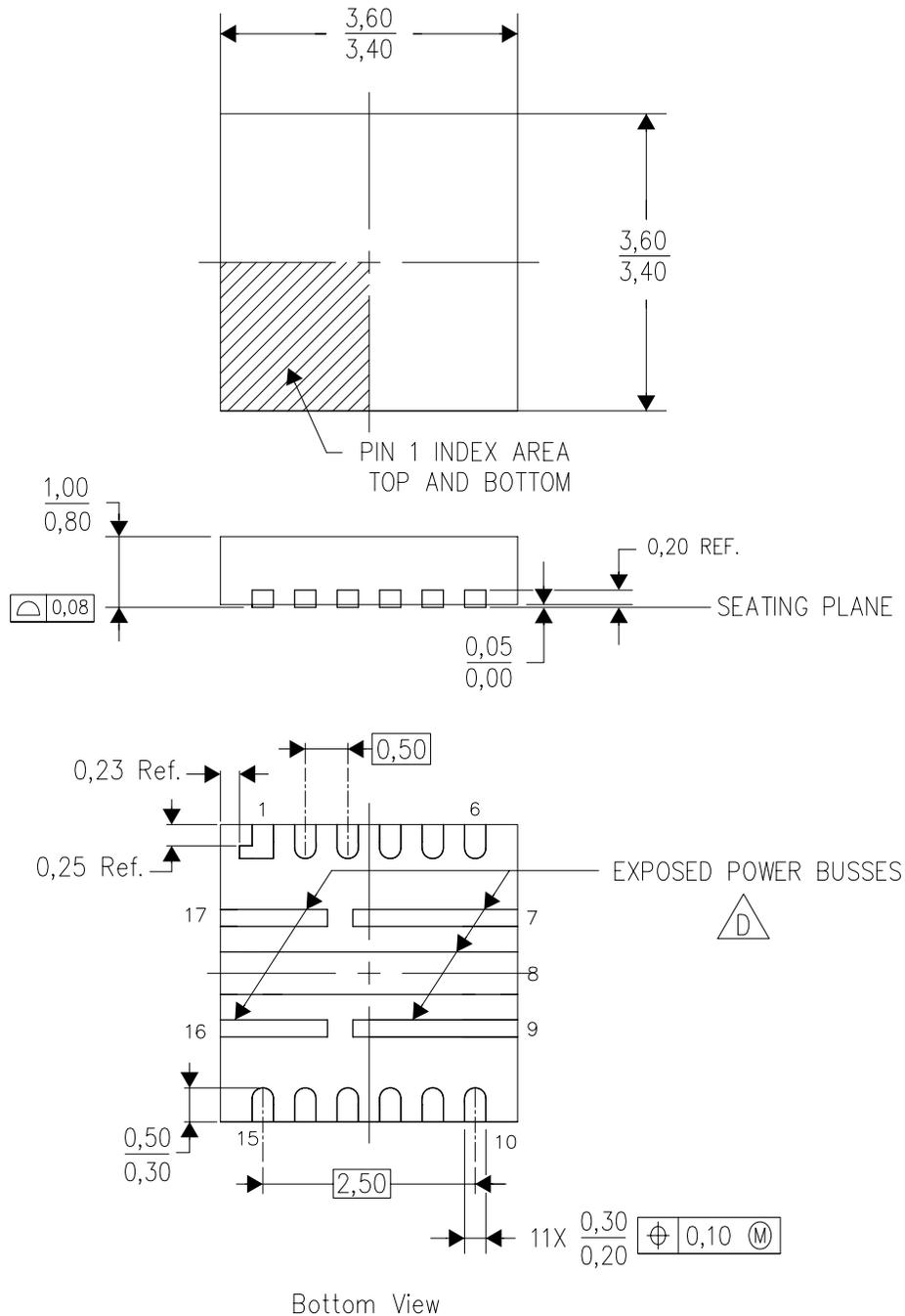
#### 4.2 Land Pad Design

Publication [IPC-7351](#) available from IPC (Association Connecting Electronics Industries®) is one of the industry standard guidelines for developing PCB pad patterns. Because the HotRod QFN package is a new style, this application report is intended as a guide and should be used with the IPC-7351 publication in designing an optimum PCB land pattern.



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

**Figure 4. PCB Land Pattern**



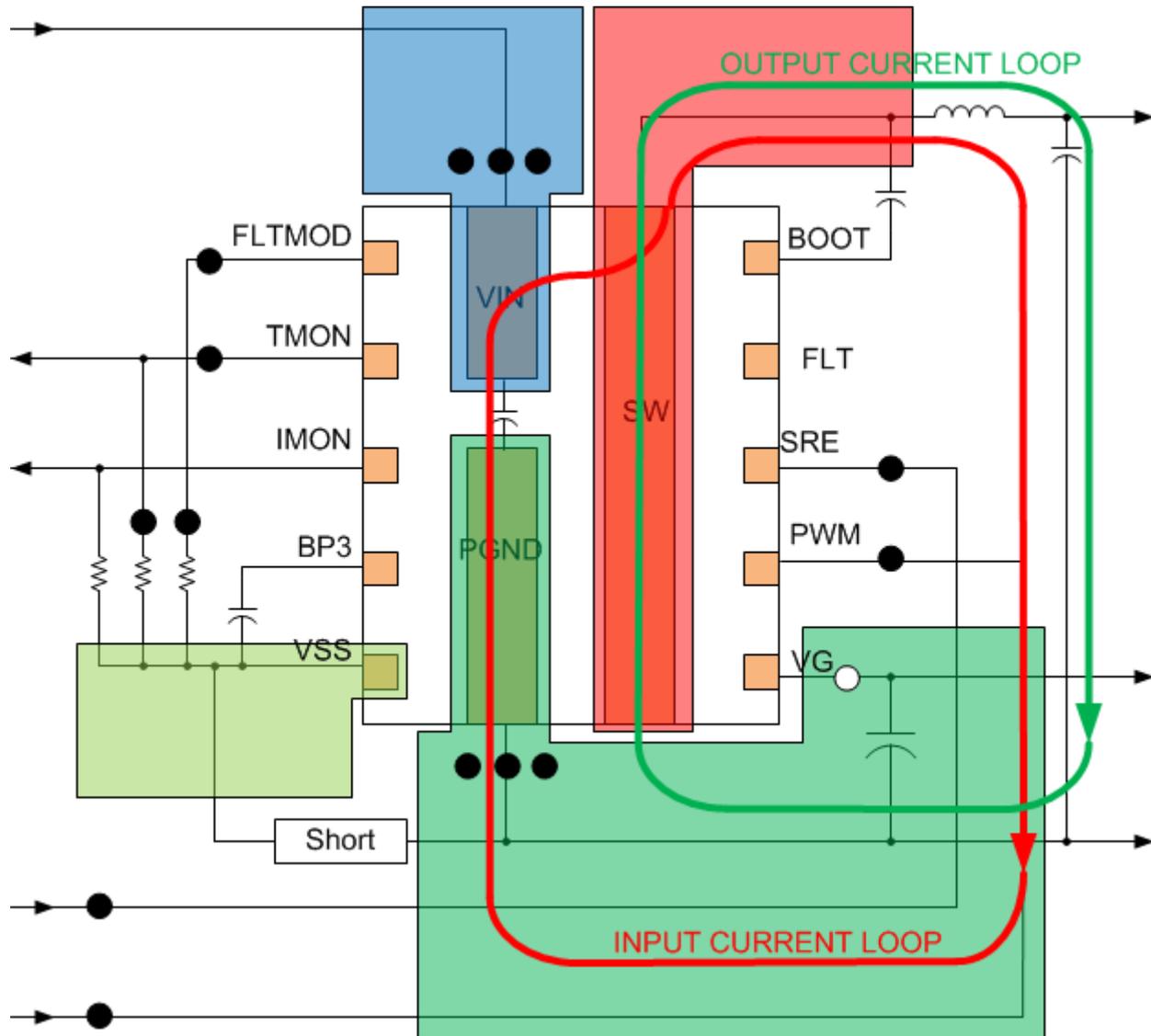
- A All linear dimensions are in millimeters.
- B This drawing is subject to change without notice. Click here to receive the latest drawing. (SLUS
- C Publication [IPC-7351](#) from the Association Connecting Electronics Industries (IPC) is recommended for alternate designs
- D This package is designed to be soldered to a thermal pad on the boards. Refer to [SLUA271](#) and the device-specific data sheet.
- E Laser cutting aperture with trapezoidal walls and also rounding corners offer better paste release. Customer should contact their board assembly site for stencil design recommendation. Refer to IPC 7525 the Association Connecting Electronics Industries (IPC) for stencil design considerations.
- F Customers should consult their board fabrication site to obtain metrics that describe the minimum solder mask web tolerance between signal pads

**Figure 5. HotRod QFN Outline Dimensions**

## 5 Layout Guidelines

The HotRod/QFN application applies mainly to the synchronous, half-bridge power stage and has two primary current loops.

- The input current loop that carries a discontinuous current with high AC content
- The output current loop that carries continuous current with high DC content.



**Figure 6. Application Layout Example**

The input current loop includes the input capacitors, the integrated main switching MOSFET, the inductor, the output capacitor and the ground path back to the input capacitor. It is a good practice to keep this loop as small as possible and place some ceramic capacitors directly between VIN pin and PGND-pin, see [Figure 6](#). On the PCB layout using HotRod/QFN package the best location for the input bypass capacitance is on the bottom side of the PCB, directly connected to and underneath the HotRod VIN-PGNG PCB landing pads.

To accomplish it the vias must be placed underneath the device package between the power pads and the signal pins or on the power pads directly. Additional vias can be placed outside of the package footprint for improved electrical and thermal conduction to inner layers of the PCB as shown in [Figure 7](#) and [Figure 8](#). The top-side placement for the VIN bypass capacitance is also available with similar performance to the bottom installation. The signal pins on the VIN-PGND side route through vias to the bottom or inner layer level of PCB to allow for the placement of VIN bypass capacitors.

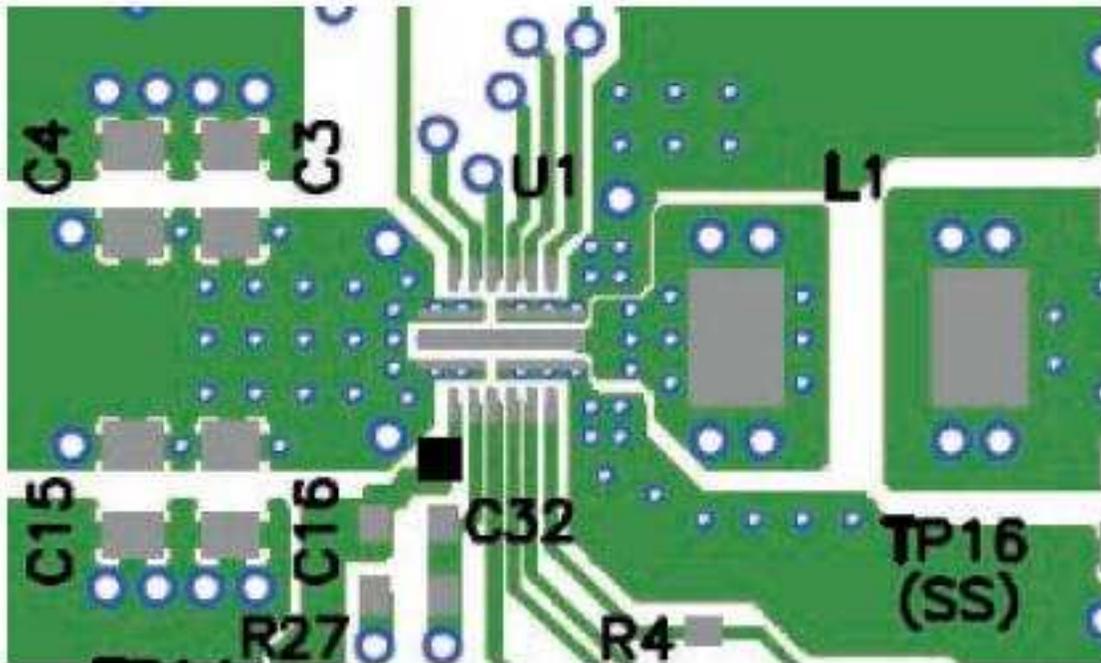
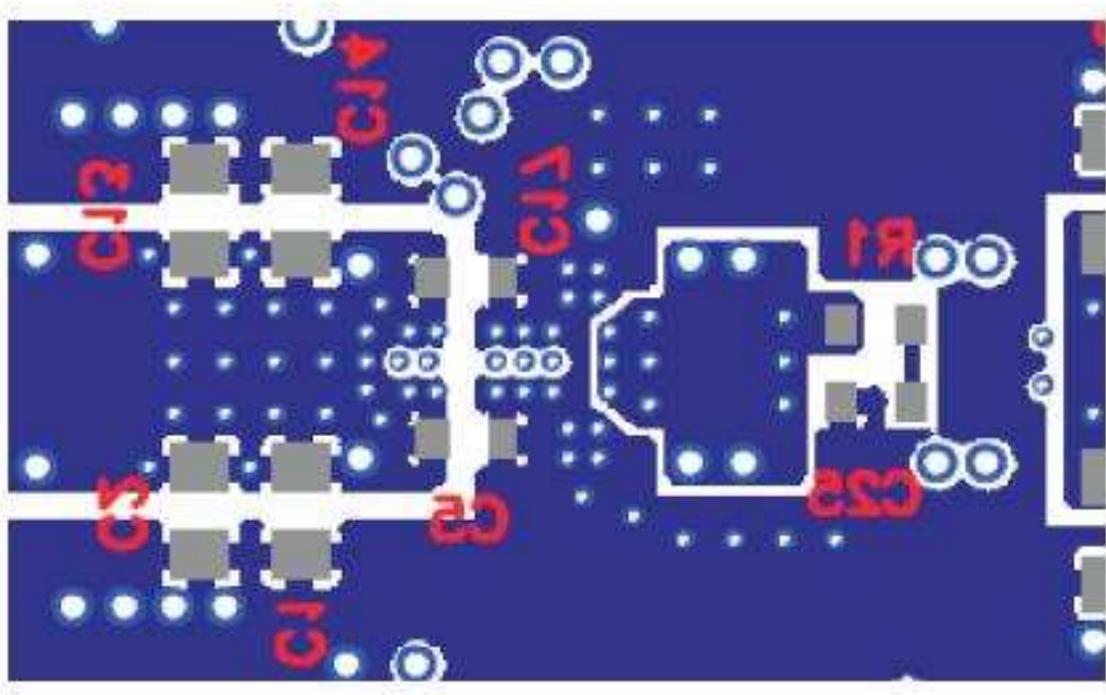


Figure 7. PCB Top Layer

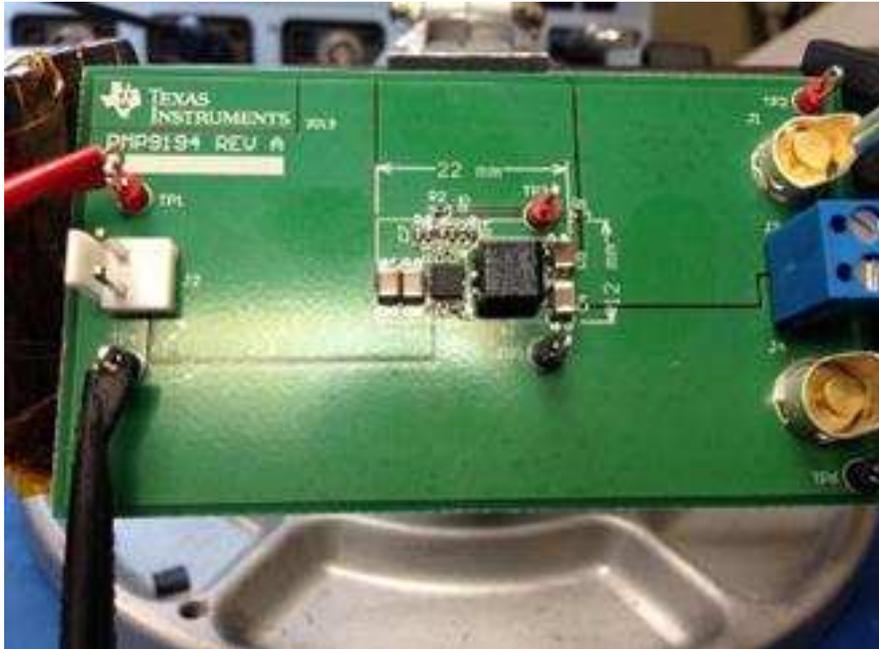


**Figure 8. PCB Bottom Layer**

The output current loop includes the SW pin, Integrated SR MOSFET, the inductor, the output capacitors and the ground return between the output capacitors and the PGND pins. As with the input current loop, maintain the ground return between output capacitor ground and PGND pin as short as possible. On the PCB layout, the best location for the output capacitance is on the top side of the PCB, directly connected to the output inductor.

Maintain the SW node area as small as possible to reduce the parasitic capacitance and minimize the radiated emissions.

HotRod/QFN allows for combining the MOSFETs and the control circuitry in a single package. It offers a high level of integration, the input and the output loop area can be minimized achieving low parasitic impedances, higher efficiency, higher power density, higher reliability (bond wires are eliminated), and reduced EMI. [Figure 7](#) and [Figure 8](#) show the example layout.



**Figure 9. TPS54020 PMP9194 with HotRod Package in Place**

A Reference Design for the TPS54020 device is available in the TI Designs section of our website. [PMP9194](#)

Follow these general guidelines for an efficient PCB layout.

- Separate the power and signal GND using 0- $\Omega$  resistor or a gap. Place it near the device GND terminal.
- Use traces as wide as possible on VIN, PGND and SW with some vias to improve thermal aspect of the layout.

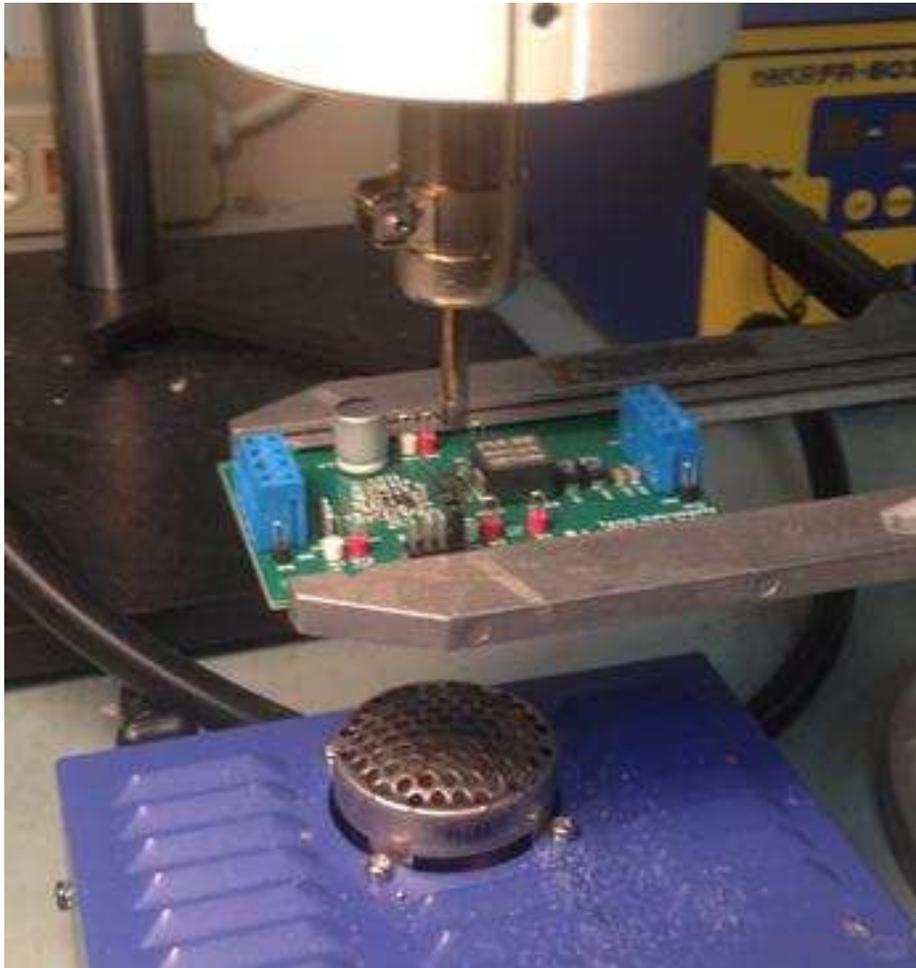
## 6 Rework Guidelines

After PCB assembly, the package should be inspected for the assembly defects such as voids, solder balling or other defects underneath the package. The HotRod QFN package offers the external side-fillet solder joint inspection and repair. To rework defects underneath the package on the power bus, the entire package must be removed.

### 6.1 Component Removal

The most simple method to remove the HotRod package from the PCB is to use the reflow profile for part removal similar to the component attachment.

Alternatively, the repair station uses the heating source from bottom of the board along with the top side hot gas nozzle to direct heat at the component to aid in its removal.



**Figure 10. Manual Rework Station for HotRod/QFN Package Devices**

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