Application Report
SLUA749A–July 2015–Revised May 2016

bq769x0 Family Top 10 Design Considerations

Battery Management Solutions / Monitoring and Protection

ABSTRACT

The bq769x0 family of battery monitor devices provides Analog Front End (AFE) and hardware protection functions for 3 to 15 cell lithium-ion battery systems. This document describes 10 design considerations for using the bq769x0 component in a battery circuit. These items should help a designer with decisions which must be made in their implementation of a battery using the bq769x0 family components.

Contents

List of Figures

Trademarks

1 Host Controller Choice

The bq769x0 is not a standalone protector and will require a host. The bq769x0 AFE will measure voltages and monitor voltage faults based on those voltages as well as monitor current faults. However, a host is required to set the registers for the protection thresholds and to turn on FET control outputs. If current measurement is desired, the host must read the values from the AFE. When faults occur, the host must clear the faults and recover when appropriate. While the AFE could be set and left to operate unsupervised, a fault would leave the battery disabled. The selection of the host will influence the appropriate AFE version.

The bq78350 is a gauge designed to control the bq769x0 AFE. It has pre-programmed behavior determined by the selection of available parameters. Protection limits can be set in the firmware. The gauging uses a Compensated End of Discharge Voltage (CEDV) algorithm which uses coefficients calculated from data collection runs with the pack design. Communication to the gauge is through SMBus. The gauge handles all communication to the AFE and does not share the I2C bus to the AFE or allow modification of the AFE registers. The bq78350 is a 2.5-V device and at its initial release supports the -00 and -01 2.5-V output AFEs, be sure to check the latest bq78350 information for options supported.

A customer provided MCU can be used with the AFE. This allows the MCU programming to provide special system behaviors for the battery. The MCU must set the protection registers, enable FETs, recover from faults, and provide a balancing algorithm, if desired. The MCU can implement a gauging algorithm and provide display or communication appropriate for the battery system. In addition to the cell voltage readings from the AFE the MCU may measure battery voltage for a real-time calibration as described in the bq769x0 datasheet and pack voltage, if desired. Any of the bq769x0 device options may be used as appropriate for the MCU.

Related to the MCU is the selection of a boot method for the AFE. The bq769x0 datasheet shows a simple concept of using a switch to boot the device when ready. If the MCU is powered from a separate regulator, it can put the AFE to sleep and boot the AFE as desired. With the bq78350, a circuit to provide a pulse is needed to boot the AFE and start the bq78350.

2 Cell Count

The bq769x0 family devices use a common register architecture to allow a host implementation to easily move across different cell count configurations. It would seem attractive to make a single board which could support any cell count supported by the AFE family. From the controller and firmware standpoint this should work well, however, there are hardware considerations which may make this unattractive. One is the inefficiency of having the board space for 15 cells when fewer cells are actually used. A second consideration is the package pitch difference between the bq76920 (0.65 mm) and the bq76930 and bq76940 (0.5 mm). A common footprint might be constructed with offset patterns similar to Figure 1, but this may have complications in component placement and routing. A third is the circuit structure differences resulting from the architecture of the family devices, details of this are described in following sections. A common board design between the bq76930 and bq76940 may be more practical; this was done on the bq76930 and bq76940 EVM boards. The cell count will generally indicate the device to use, see the datasheet for supported cell counts. In cases where there is an overlap in the cell count supported between devices such as 9 or 10 cells the selection might be based on the lower cost part or the desirability of an extra temperature sensor.

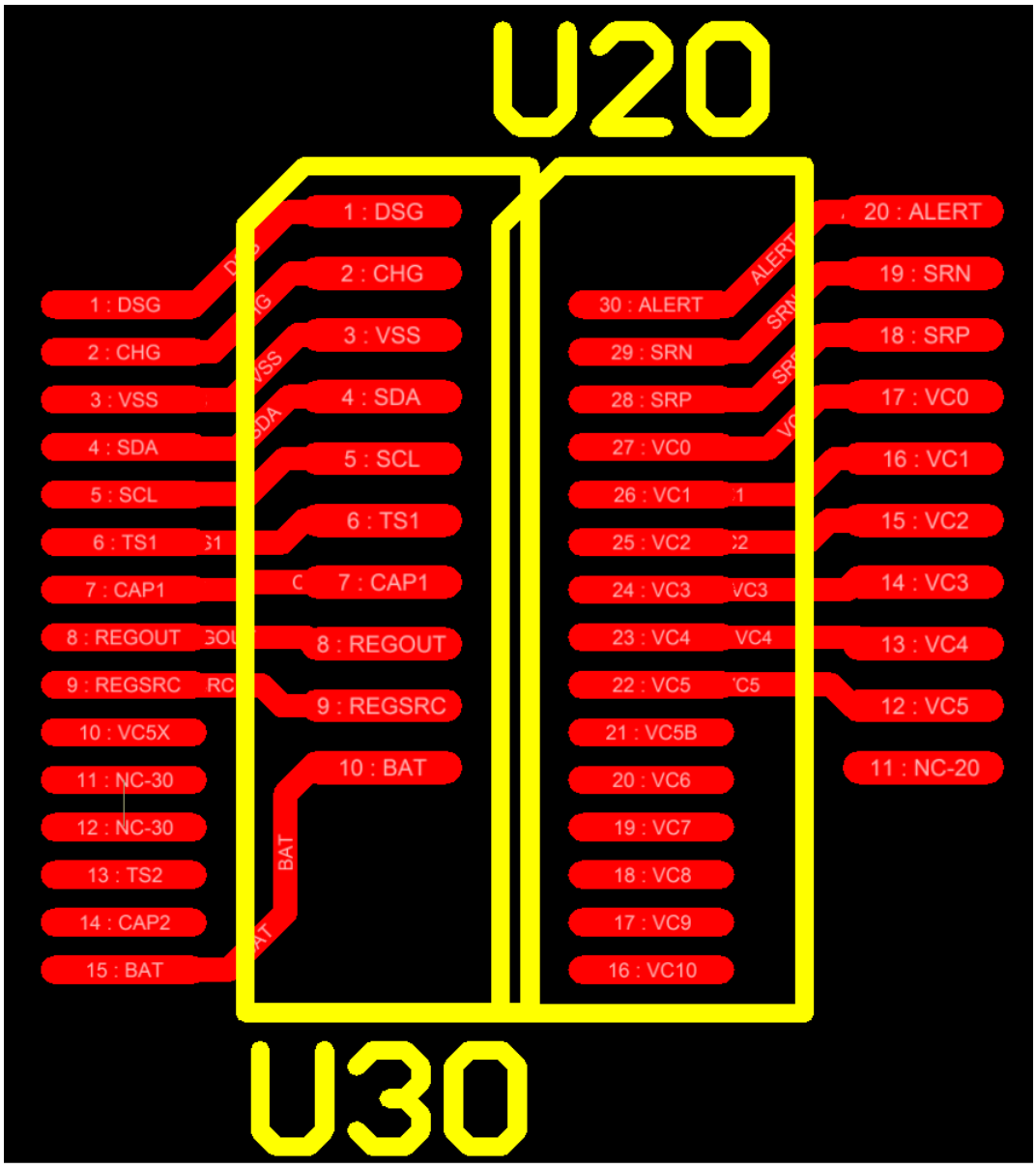

Figure 1. Common Footprint Concept

3 Device Architecture

The bq769x0 family devices are built with a 5 cell group structure. Each cell group can support 3 to 5 cells. Each group has a 14-bit ADC which supports its 5 cells and thermistor. Each group has an independent timeline. Voltage and temperature readings from the upper groups are communicated to the bottom group registers for access by the host. Power for the voltage and temperature circuit comes from the BAT pin. Current monitoring, FET drives, and user communication are provided only on the bottom group, power for these functions comes from the REGSRC pin.

The bq76920 uses a single cell group. Signals are referenced to VSS. The bq76920 BAT pin can be powered by a hold-up circuit so that a moderately sized filter capacitor can be used. A method to prevent excessive voltage on the pin should be provided; a discharge resistor across the diode may prove sufficient. In some cases a zener may be needed to limit the voltage on the pin. The zener should limit the voltage to a few volts above the top cell. The Rc and Cc input filter components used with the bq76920 can use a wide range of values.

The bq76930 and bq76940 stack 5 cell groups using 2 and 3 groups, respectively. The VSS of the upper group is connected to the BAT pin of the lower group. The supply current flows from the BAT pin through each group to VSS. Only a small offset current flows in the intermediate power pins (VC5X and VC10X), this is shown in Figure 2, values are shown in the datasheet. There is an offset current increase into VC5X when the ALERT signal is high, the accumulative effect of this current on the system can be minimized by the microcontroller clearing the status register as soon as the ALERT is set.

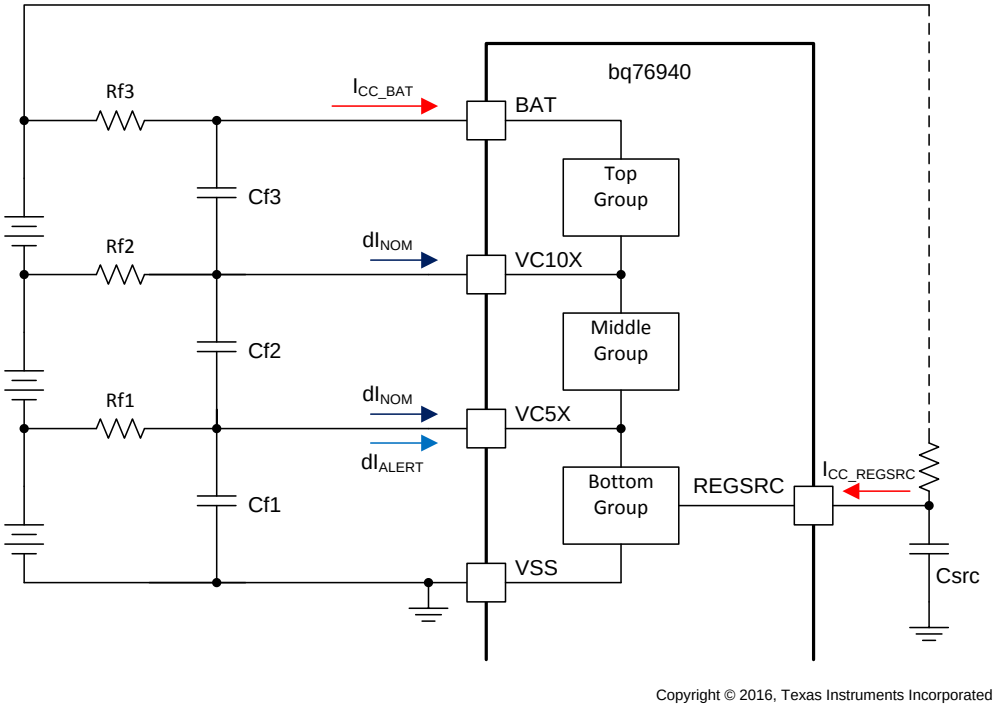

Figure 2. BAT Supply and Offset Currents

With this device architecture of the bq76930 and bq76940, when a heavy load such as a short circuit is applied to the battery, each cell voltage will drop to a low value. Current is drawn through each input filter resistor. Initially the filter capacitors discharge. On the lower group the inputs do not go below VSS. On the upper groups, the Cf power filter capacitors hold the group reference voltage above battery- and current continues to flow from the input resistors. After the input filter capacitors are depleted, current will flow from the device inputs continuing the discharge of the lower Cf capacitors as shown in Figure 3. This current flow is generally undesired in semiconductor devices but the family was designed with this architecture. The input voltage will drop below the group reference, but current is limited by the input resistors and no damage is expected. If needed for the individual implementation, Schottky diodes may be connected from the group reference to the group inputs to carry the current outside the device. These diodes are shown in Figure 4 and patterns were included on the EVM. The BAT pin filter resistor draws current through the stack of Cf capacitors. The upper group inputs draw current from the lower group's Cf capacitor. The upper Cf capacitor will discharge more slowly than the lower Cf capacitor. The lower group power must remain above the VSHUT level so that the device can time the short circuit event and turn off the DSG FET output.

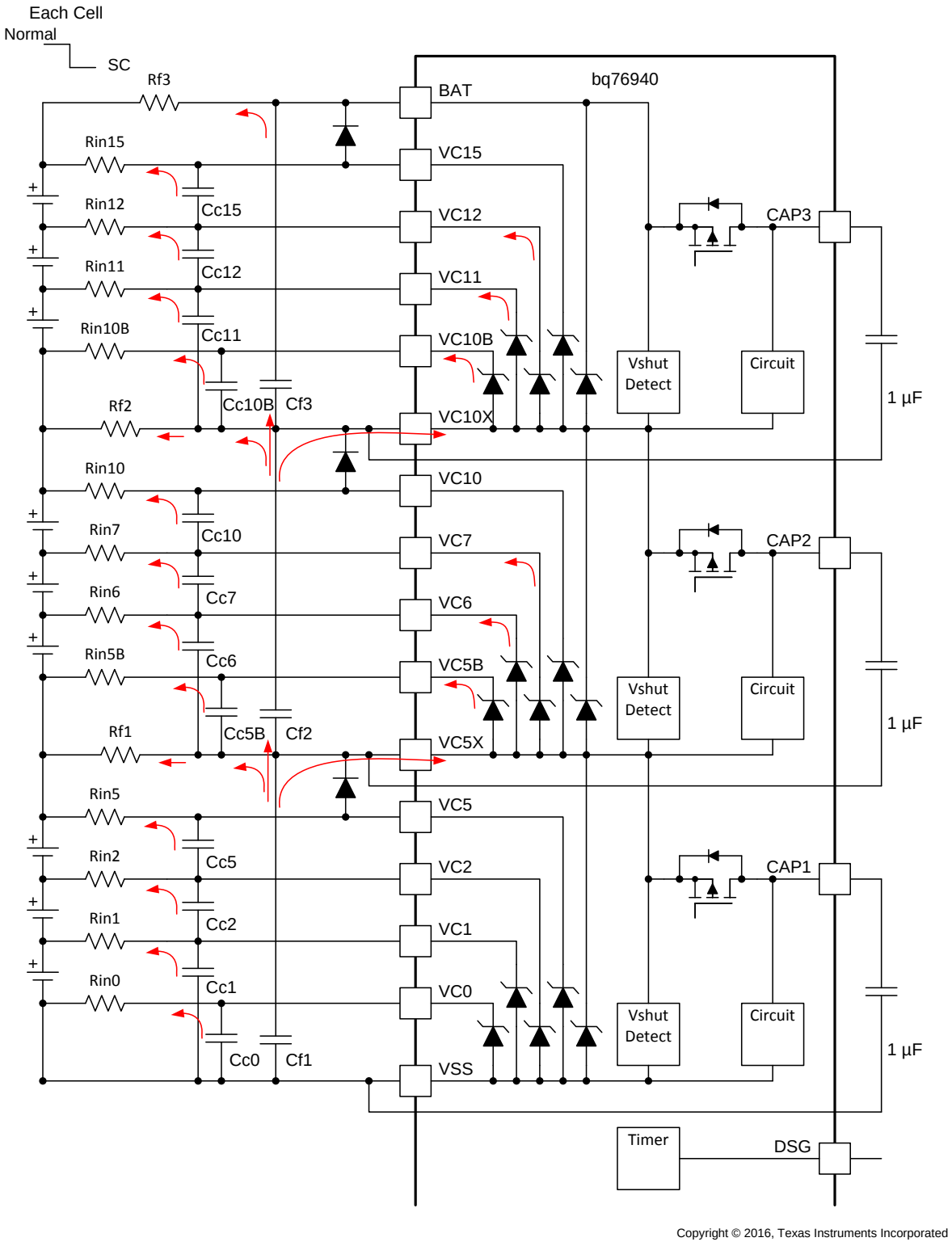

Figure 3. Current From Input Pins

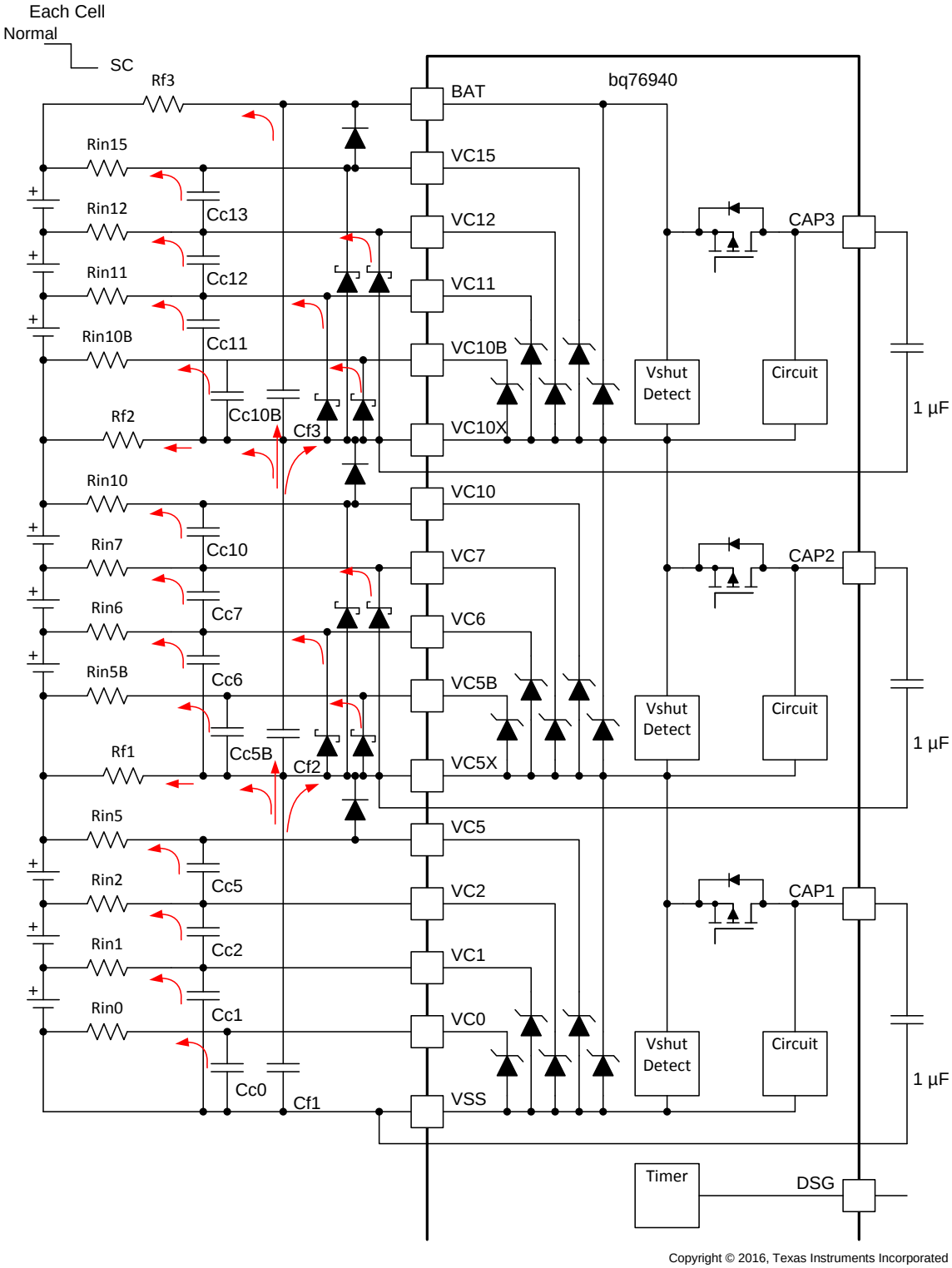

Figure 4. Avoiding Pin Current With Schottky Diodes

Because of the architecture of the bq76930 and bq76940, the Cf capacitors used should be large and the input filter resistors should also be large. Generally the Cf capacitors use the same value for all capacitors. A hold-up circuit with diodes should not be used on the power pins of the bq76930 and bq76940. The datasheet shows a large range of values, but the larger values should be used with these family members.

4 Cell Balance

The bq769x0 devices have internal balance FETs controlled by the host through registers. When enabled, the internal FET will pull the pins associated with that cell together drawing current through the input resistors for that cell. For the bq76920 the input resistors can be sized to select the balance current within the capability of the part. For the bq76930 and bq76940, the input filter resistors must be large due to the device architecture, so internal balance current is limited in these family members.

The 250 ms measurement timeline is divided into 12.5 ms intervals. When balancing, the balance FET is enabled for 14 of the 20 intervals. The balance FET is turned off for one interval before measurement starts on the bottom cell of the group. The cells are then measured in sequence. The input filter must settle within the 12.5 ms or there will be voltage error in the cell measurement. Since the cells are measured in sequence, the bottom cells will show the largest influence. The more cells are balanced, the more time will be required for the filter to settle. For the bq76920, the Rc input resistors are adjusted for the balance current and are typically in the smaller values of the datasheet range, and the Cc filter capacitors can generally be large. For the bq76930 and bq76940 the input resistors are large and the Cc capacitors may be smaller for improved measurement.

Since the cell inputs pull together during balancing, care must be used to prevent damage to the inputs. If all cells in a group are enabled to balance at the same time, the inputs will pull together and some of the maximum limits will be exceeded, the part is likely to be damaged. Balancing every other cell in a group will double the voltage on the unbalanced cell and is typically OK, check the voltage limits for the cell voltages used in your design.

External cell balancing can be used with the bq769x0 family. An external FET is switched to draw current from the cell through a resistor. Control for the FET comes from the voltage across one of the Rc input resistors. When P-channel balance FETs are used the upper resistor is used, see Figure 5. When N-channel balance FETs are used, the lower resistor is used, see Figure 6. A FET with a defined $R_{DS(ON)}$ at approximately ½ the cell voltage is desired. These FETs will typically have a low maximum V_{GS}, so the gate voltage will usually need to be protected by a zener diode. The gate voltage should be connected through a resistor to limit the current when the diode conducts. During normal operation the zener will not conduct. During a heavy load event such as a short circuit, the cell inputs will drop near battery- while the IC VCn pins will initially be at their normal voltage as shown in Figure 7. The zener diodes will prevent the high voltage from reaching the gate and most of the input resistor voltage will be dropped across the gate resistor. The gate resistor current will contribute to the drop of the Cf capacitor voltage, so the gate resistors should be large. When the short circuit is released, the voltage will reverse on the input filter resistors and gate protection zeners will conduct in the opposite direction.

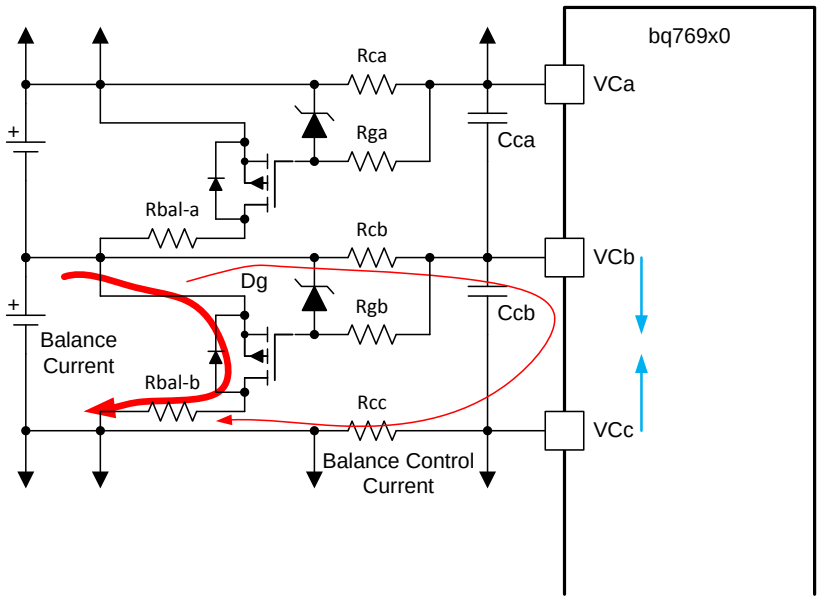

Figure 5. P-Channel External Balancing

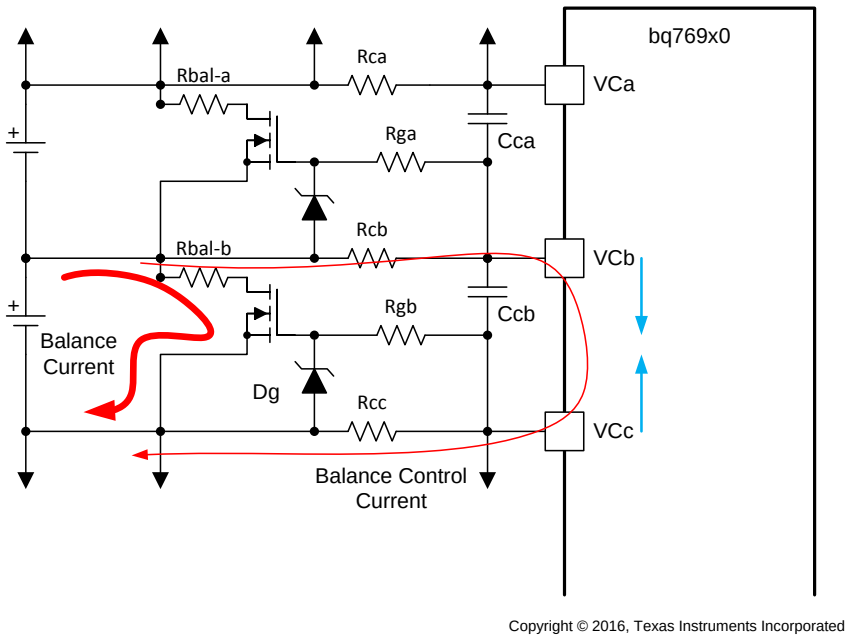

Figure 6. N-Channel External Balancing

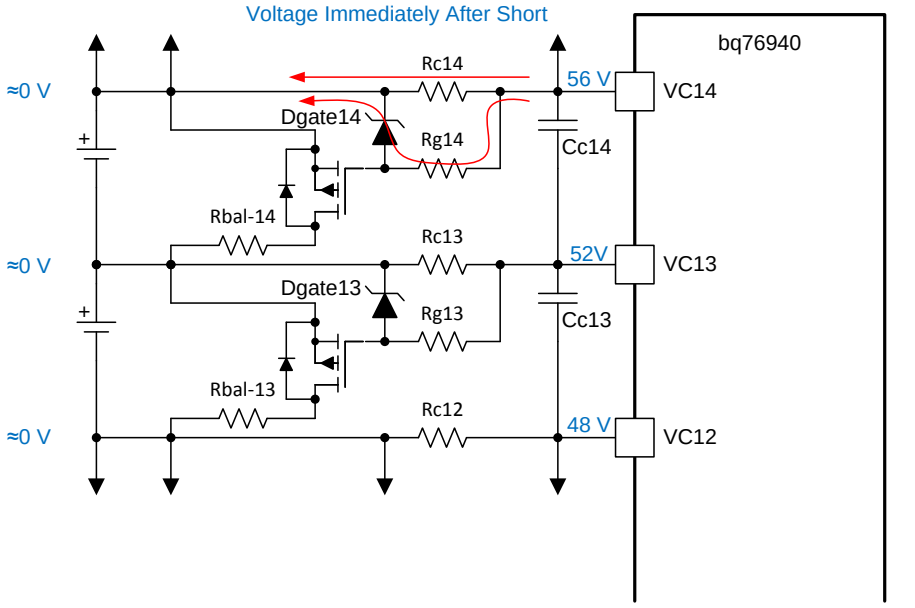

Figure 7. External Balance FET Gate Protection

P-channel vs. N-channel balance FET selection may also be influenced by cell connection. During cell connection, inrush current through the filter resistors will turn on P-channel balance FETs and pull up the lower input. This effect can continue down the cell stack. N-channel FETs do not turn on during recommended connection and may be preferred. See the discussion in the random cell connection section for these considerations.

The timelines of the cell groups in the bq76930 and bq76940 are independent, so one group may be balancing while the next group is measuring. At the cell boundary between groups, the adjacent cell may measure a voltage from the balance current in any common path. Keeping the common path resistance low, using wide traces or returning the current as close to the cell as possible will reduce this effect (see Figure 8).

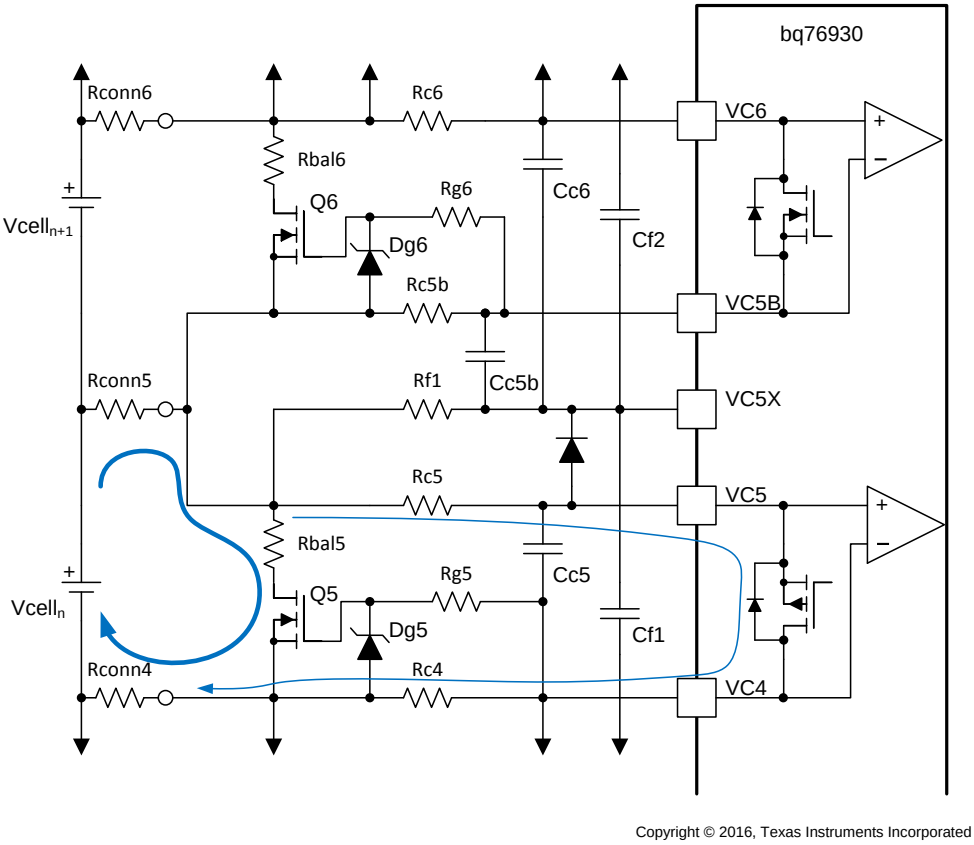

Figure 8. Balancing at Group Boundary

The system designer must determine how much balance current to provide. This is sometimes not an easy question. The self discharge rate of the cells may vary cell-to-cell, and with the environment in which they are operated. Cells which are at a higher temperature in the system may discharge faster. Where the cells and their environment are well matched, the electronics may contribute to an imbalance. The dI_{NOM}, dI_{SHIP} and dI_{ALERT} currents in the bq76930 and bq76940 will cause different loads on the cell groups and may eventually need to be balanced out. A pack which is charged every day may need lower balancing current than a pack which is charged monthly, or a pack which is charged infrequently may need to balance longer than a frequently charged pack when using the same balance current.

5 XREADY

The bq76930 and bq76940 family members communicate balancing commands from the registers in the bottom group to the upper groups and voltages from the upper groups to the lower group register. The internal communication is monitored by an internal watchdog function. If too many of the communications have errors, the device sets the DEVICE_XREADY fault indicating it does not trust the voltages available from the upper groups. Since the voltages are not known, the device sets the DSG and CHG FET control signals off. The host can recognize the event, clear the fault and re-enable the FETs, but it cannot disable the watchdog feature. The minimum time that the FETs will be off may be approximately 100 ms. XREADY may be avoided by locating the power filter capacitors near the IC and careful board design, but operation of the feature cannot be prevented. XREADY is expected if the AFE is booted without cells connected to the upper groups. XREADY does not occur in the bq76920 since there is a single group.

6 FET Drive

The bq769x0 family has FET control outputs referenced to VSS as described in the datasheet. The CHG and DSG outputs are powered from a 12-V supply regulated from the REGSRC supply. When high, the outputs will be 12 V nominal when the REGSRC supply voltage is sufficient. If the voltage drops below the regulation point the CHG and DSG output voltages will also drop. These outputs may be used to drive small to medium low-side protection FETs. A typical circuit is shown in Figure 9. When large FET arrays are used, a driver will be needed, the ground referenced CHG and DSG outputs should be easy to interface to a driver. A high impedance driver is recommended for the charge driver due to the high resistance pulldown of the CHG pin.

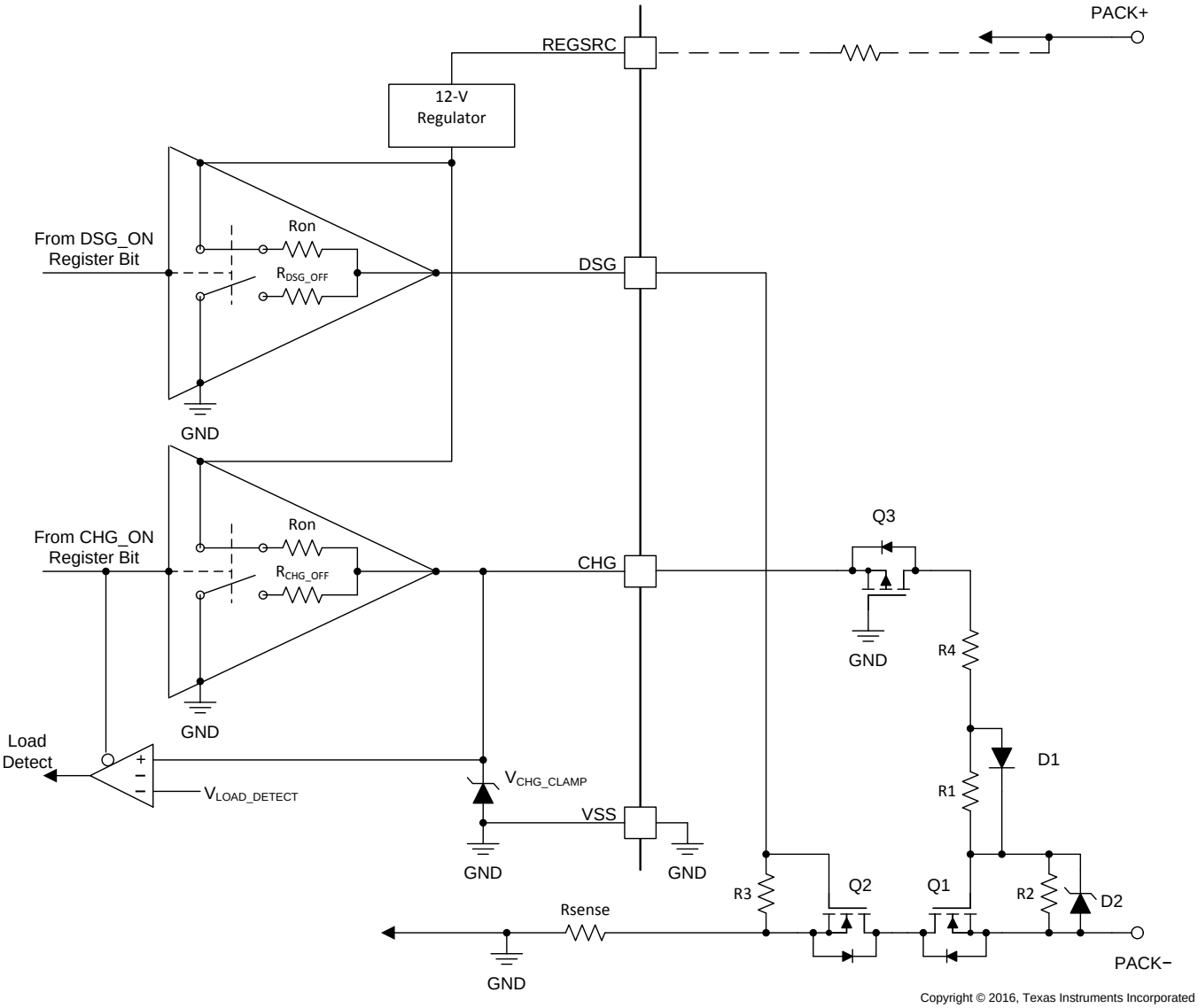

Figure 9. Typical Low-Side FET Connection

The DSG output can connect directly to the low side N-channel FET gate when it is suitable since the driver has an internal resistance to limit the switching speed of the FET. Pull-down resistance of the DSG output is shown in the datasheet and is typically 2.5 kΩ. The pull-up resistance may be calculated from the rise time conditions in the datasheet and is approximately 5 kΩ. Increasing the load current or the FET gate capacitance will cause the driver to switch more slowly. In some cases an additional resistance may be desired between the DSG pin and the discharge FET gate, this will slow the discharge gate switching. When multiple FETs are used, a small resistor to the gate of each FET may be desired, check with your FET supplier. Switching speed will slow with multiple FETs due to the added capacitance. When faster switching is needed a driver will be needed for the FET gate.

The CHG pin must be connected to the charge FET gate through a circuit to allow the charge FET to operate properly in several phases of operation. The typical circuit is shown in the datasheet and in Figure 9. CHG pin pull-down resistance is 1 MΩ nominal, pull-up resistance can be calculated from the rise time and is approximately 5 kΩ.

When the battery is in a normal state and has both the Q1 and Q2 FETs ON, it is desirable to have most of the CHG pin voltage available on the gate of Q2 to maintain a low resistance in the FET. Q3 will be on with a low resistance. D1 will provide a fixed drop 'shorting' R1. A voltage divider will be created by R4 and R2. R2 should be large and R4 small so that most of the CHG pin voltage is applied to the gate. R2 may be 1 MΩ typical while R4 may be 1 kΩ.

When the CHG pin turns off, it will pull down the Q1 charge FET gate through Q3 body diode, R4, and R1. R2 also pulls down the gate and when the charger pushes the PACK- voltage below battery-, R2 keeps Q1 off. Q3 is off and allows the Q1 gate and source to fall to a large voltage below the IC VSS at the battery- voltage.

When the CHG output turns on CHG and Q3 drain will try to go to approximately 12 V. If the battery had been discharged 15 V below the charger voltage, there would be a 27 V difference between the Q1 source and the Q3 drain voltage. D2 avoids a damaging voltage from being applied to the Q1 gate if the FET does not turn on fast enough to limit the gate voltage. R4 will drop some voltage but may be considered optional since Q3 would limit the current when the CHG pin voltage pulled down sufficiently. D2 should be selected so that it does not conduct when Q1 is on with PACK- at the battery- voltage but protects Q1 against transients exceeding the V_{GS} maximum limits. For low voltage batteries, D2 may not be required.

When the discharge FET is off and a load is applied to the battery, PACK- will pull up toward PACK+. Normally in this situation the system will also turn off the CHG driver. In this condition the circuit behavior may be easier to visualize if re-drawn with the power FETs removed as in Figure 10. PACK- may be the same voltage as PACK+ if R_{LOAD} is small. D2 conducts and protects the Q1 gate from excessive voltage. The CHG pin voltage will rise to the V_{CHG_CLAMP} voltage. D1 blocks current flow so the voltage between D2 and the CHG pin is dropped across R1 and R4. R4 is small, so R1 must be large to limit current into the CHG pin. Q3 will be on in this condition. The designer may note that the datasheet test current CHG sink current is 500 µA, but the maximum V_{CHG_CLAMP} at this test current is 22 V maximum and would exceed the V_{GS} maximum of most FETs used for Q3. With a 50-V difference between the PACK- and CHG and a 1-MΩ resistance the current into CHG would be approximately 50 µA. The V_{CHG_CLAMP} is lower at lower current as shown in Figure 11, however, without a maximum voltage at a similar test condition designers may chose to implement their own known clamp as shown at D3. The D3 clamp value may be in the 15- to 18-V range so that it protects the Q3 V_{GS} maximum limit but does not conduct at normal CHG output levels. As noted in a previous paragraph, a low voltage battery pack may not need a D2 zener to prevent excessive positive V_{GS} on Q1. The same pack low-voltage pack may not need D2 to prevent excessive negative V_{GS}. Current may be further reduced or the designer may consider removing R1 and D1 since R2 could provide sufficient current limit. R1 and R2 should generally be large to limit the leakage current when the load remains on the PACK with the FETs off.

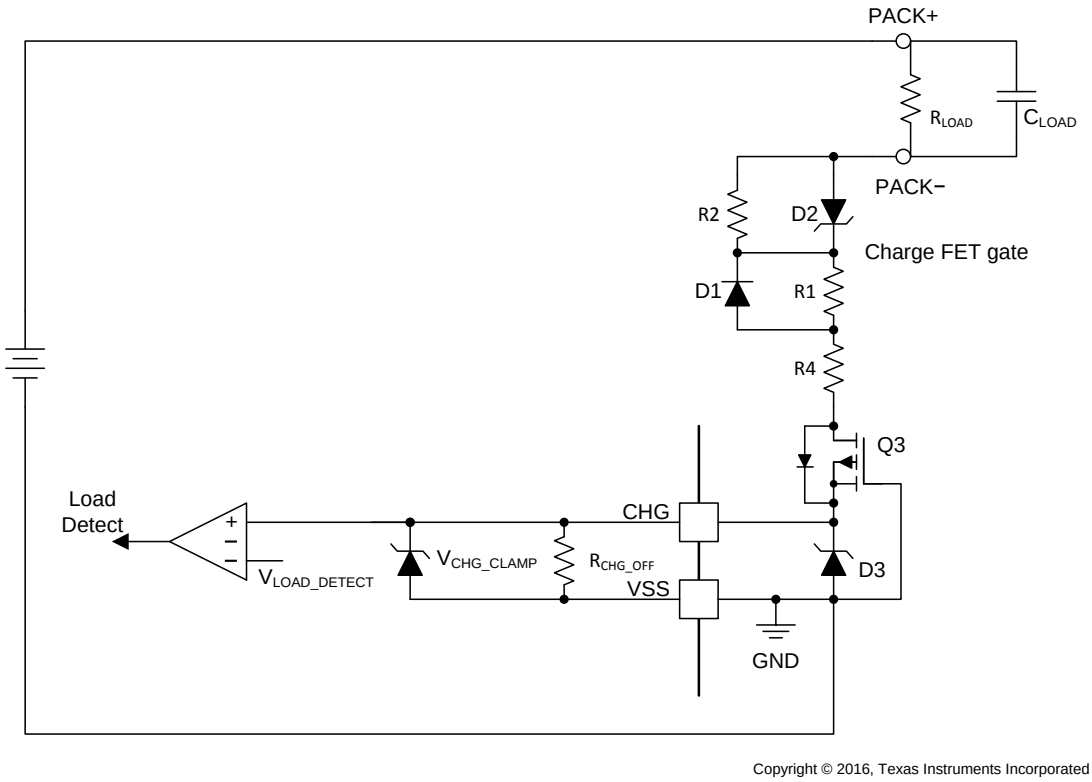

Figure 10. CHG Circuit With Load Applied

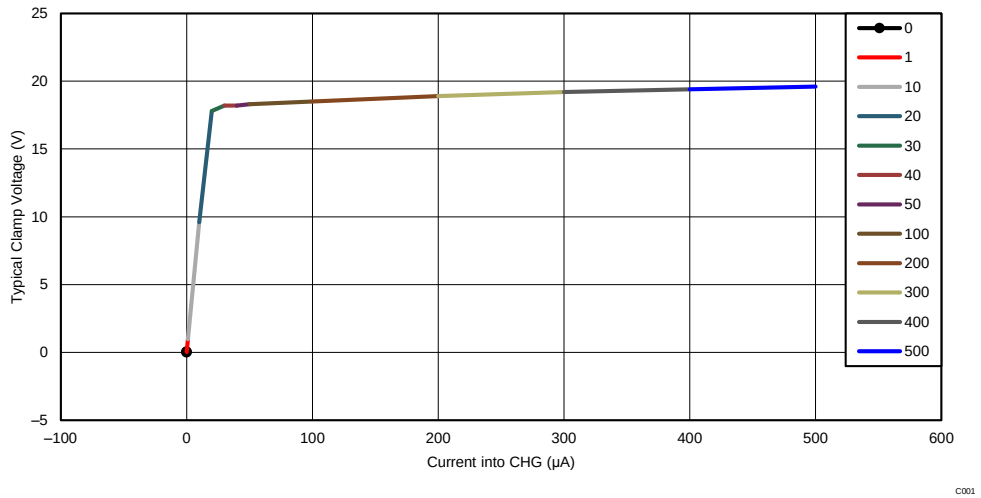

Figure 11. CHG Pin Typical Clamp Voltage

Turn off of the CHG FET will be slow with the high resistance of the CHG pin, its path resistance and the gate-source resistor. For many systems the charge current is much lower than the discharge current and the slow switching from this high resistance allows the charge FET to switch within the safe operating area of the FET. Systems which have higher charge currents or parallel FETs may require a driver. As with the circuit described above, the driver will need to float from possibly a large negative voltage up to the PACK positive voltage and limit current into the CHG pin when high. It will need a power supply, a level shifter and should reference PACK- to keep the FET off when the charger voltage is greater than the battery voltage.

7 Load Detect

As described in the datasheet and shown in Figure 9, a load detect feature is built into the CHG pin and enabled when the CHG output is low. When using low side switching the CHG pin will be pulled up by a pack load through the gate drive network when the discharge FET is off. From the simplified circuit in Figure 10, it can be observed that the load must be a high impedance before the comparator will release. With common resistor values CHG may be approximately half the PACK- voltage less a couple diode drops. PACK- may need to be in the 3 to 5V range to remove the load detect condition. A load capacitance will take some time to discharge due to the large R_{CHG_OFF} and series resistances. When a buffer is used for the charge FET drive, check its topology to see if the buffer circuit will provide a signal back to the CHG pin for load detect before relying on its operation.

8 Low-Side Switching Considerations

Communication with a battery over a ground referenced interface such as SMBus is typically connected to PACK-. When low side protection FETs are used, PACK- is disconnected and reference for the communication lines is lost. The communication interface will not likely work and the signals may present an un-protected leakage path for charge or discharge. Common solutions are to isolate the current paths if appropriate, switch the interface as well as the power path, isolate the interface or use high side protection FETs. The appropriate selection may vary with the application, the designer should be aware that the typical circuit or EVM schematic is not a complete product.

9 REGSRC Supply

REGSRC is a power supply pin separate from the BAT pin which is used to provide power for the FET outputs, and internal circuits such as the coulomb counter and I2C interface as well as any external load through the REGOUT regulator. The FET outputs and REGOUT are provided by internal linear regulators, so the available voltage for the FET drive will be limited by the applied REGSRC voltage. Low voltage packs should use appropriate low gate voltage protection FETs. Power dissipation in the part will also depend on the REGSRC voltage, the REGOUT voltage option and the applied REGOUT load. Figure 12 shows the available FET voltage and nominal dissipation in the IC with a 3.3V REGOUT option and a continuous 20mA load over the recommended input voltage range for REGSRC is 6 to 25V. Dissipation for the 2.5V device output would be higher. Average dissipation with a duty cycled load would be lower. For best FET performance, a higher voltage is desired, for low internal dissipation a low voltage is desired. The best compromise for the device may be to provide a constant supply at approximately 13 to 15V, but this will not typically be available in the battery. Where the power dissipation excessively heats the part or high efficiency is required in the battery, it may be desirable to provide the low voltage load through a separate regulator. REGOUT is used internal circuitry also so it must have a capacitor even if it is not used for external loads.

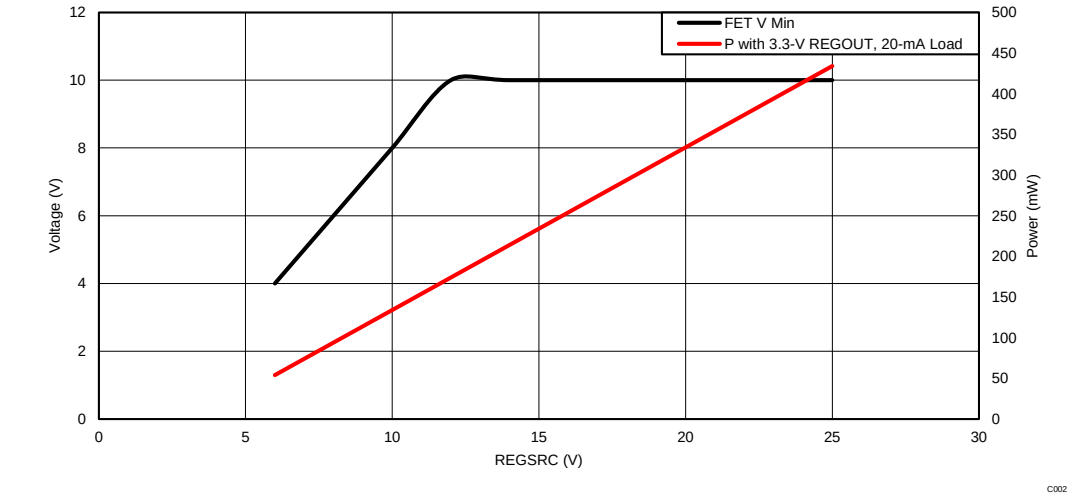

Figure 12. Minimum FET Voltage and Device Dissipation vs. REGSRC

With the bq76920, the REGSRC pin has the same recommended range as the BAT pin. These pins can generally be tied together to share the same power filter as shown in Figure 13. When a heavy load or short circuit is applied the diode prevents rapid discharge of the BAT and REGSRC pins so that the IC can continue to operate to time the load or short circuit event and with sufficient REGSRC voltage to maintain the FET drive outputs for a good V_{GS} and low resistance from the FETs. While there is not a value in the recommended operating conditions table, it is expected that the BAT pin voltage is normally approximately the same value as the top cell. When the load on the REGOUT pulls the REGSRC pin down significantly, a separate filter can be used on the REGSRC pin to avoid pulling down BAT. As discussed with the BAT pin voltage a zener may be required from the REGSRC pin to VSS to avoid over voltage in some cases.

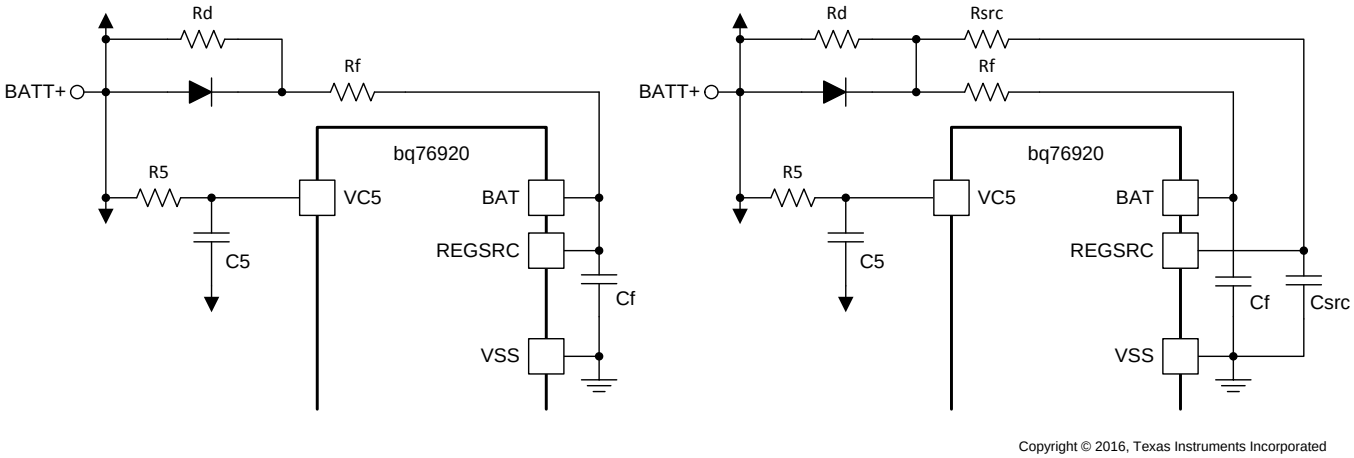

Figure 13. bq76920 REGSRC Power Option

With the bq76930 and bq76940, the BAT pin voltage may be significantly higher than the maximum acceptable voltage for REGSRC. The datasheet shows using a FET referenced to the VC5X voltage as a source follower. This topology allows REGSRC to operate approximately V_{GSTH} of the FET below the VC5X voltage. FETs are voltage controlled, so the cell stack is not imbalanced by the connection. Current for REGSRC comes from the top of the cell stack, voltage is dropped across the source follower FET. A diode is desired in the path to prevent REGSRC from dropping during heavy load or short circuit as shown in Figure 14. A resistor across the diode will help discharge any transient detected by the diode. The source follower and any dropping components will create an offset between the gate reference and REGSRC voltage. The reference voltage will vary over the dynamic range of the battery, and while that may keep REGSRC in the recommended operating range, it may have an effect on the available FET drive voltages, see Figure 15 If the diode-resistor pair is placed in the source path the voltage drop on the diode with load will reduce the voltage at REGSRC and power dissipated inside the IC, but the REGSRC voltage drop at low cell voltage may have an undesired effect on the FET drive voltages. Placing the diode-resistor pair in the drain path will allow a higher voltage on REGSRC at lower cell voltages. The drain resistor will isolate the FET from ESD on the PACK+ and will reduce power in the FET, but should not be so large that it causes FET source and REGSRC to drop.

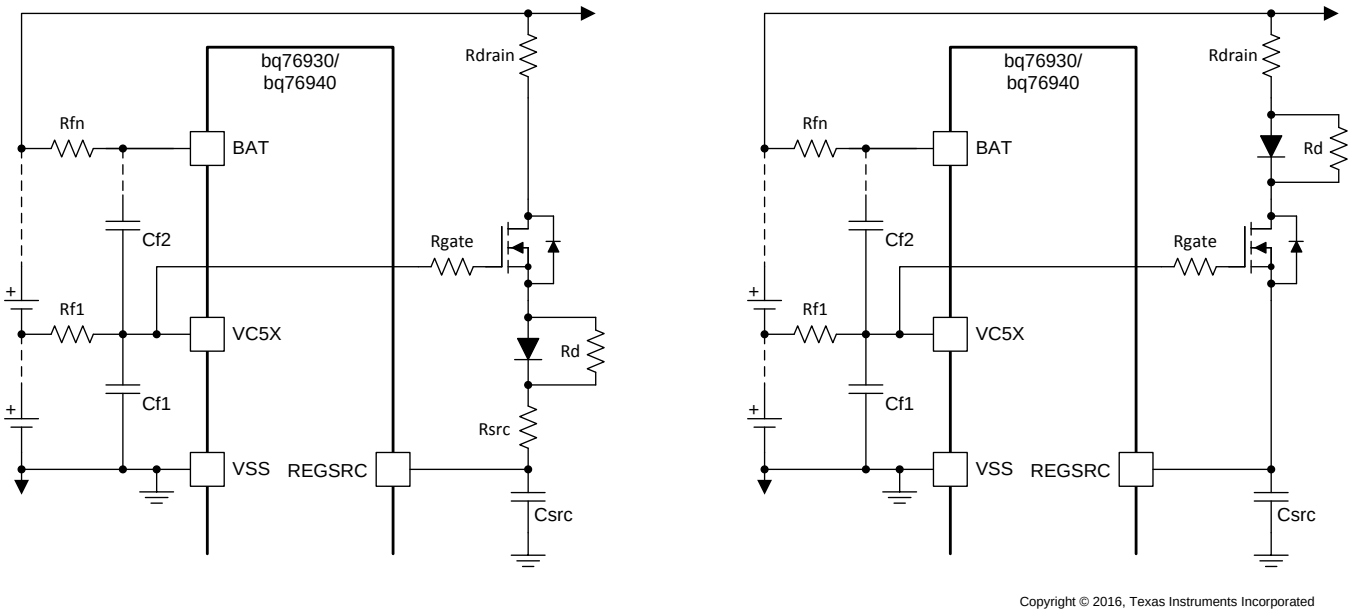

Figure 14. REGSRC Source Follower

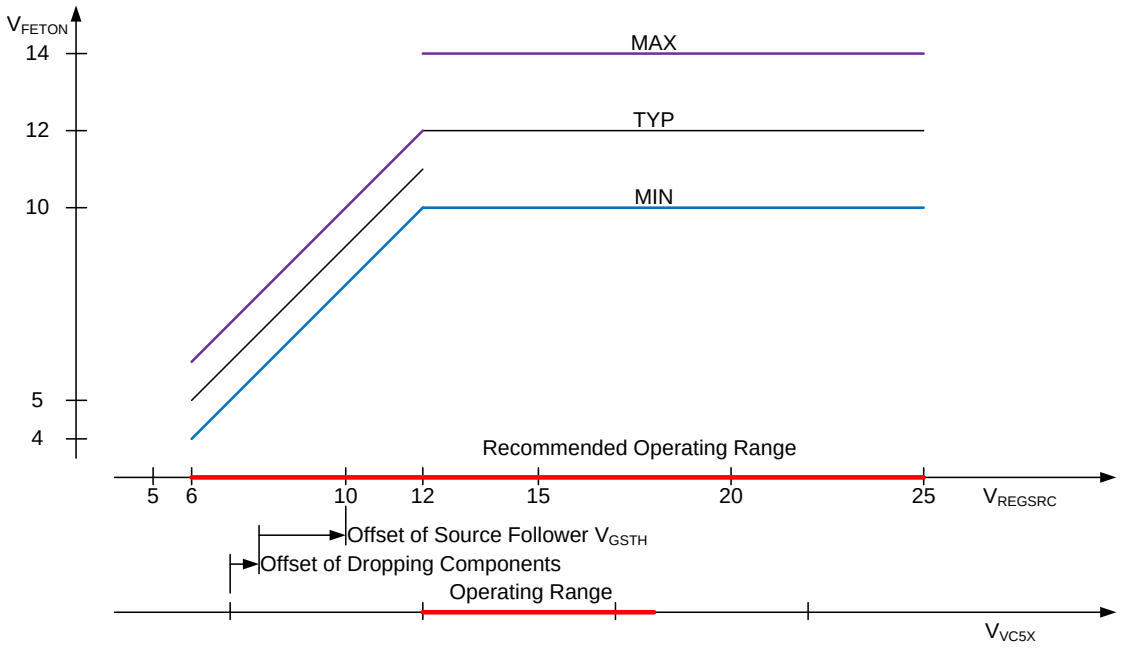

Figure 15. FET Voltage Variation With REGSRC Offset

For low cell voltages and low cell counts, it may be possible to filter the PACK voltage directly for REGSRC as shown in Figure 16. For the bq76940 there may be cases where using the VC10X as a reference for the source follower gate reference may be suitable. A zener reference would provide a stable voltage reference for the source follower, but would generally be undesired in a battery due to the continuous bias current for the zener. VC5X and VC10X are already heavily filtered and attractive references, but in some cases filtering another cell to provide the gate reference might better fit the needs of REGSRC over the dynamic range of the battery. When the reference voltage for a source follower is at a voltage potential greater than the V_{GS} limit of the FET, protecting the gate with back to back zener diodes may be desired such as shown in Figure 17.

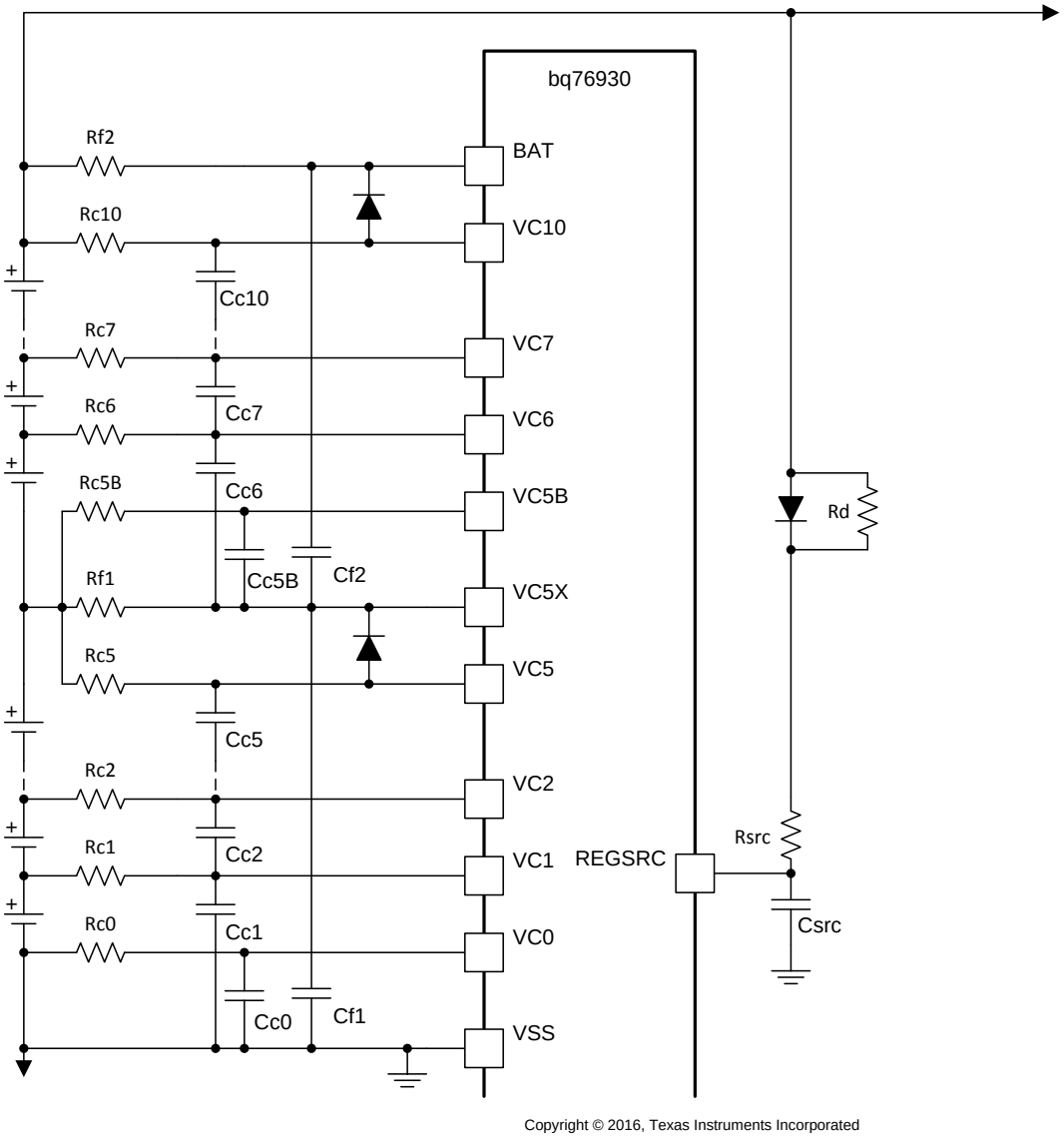

Figure 16. REGSRC From BAT With 6 Cells

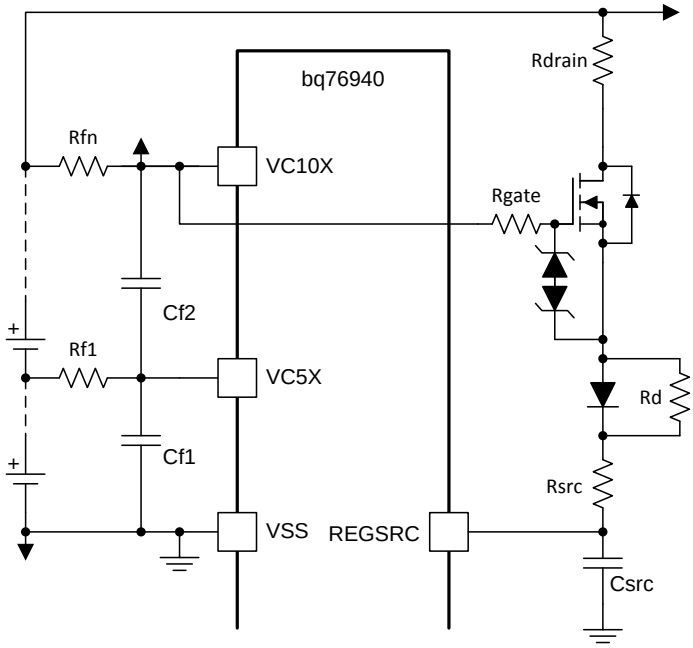

Figure 17. bq76930/bq76940 REGSRC

10 Random Cell Connection – Within Limits

The bq769x0 datasheet feature list includes “Random cell connection tolerant”. The user may be left wondering what this means since there are no specifications related to the cell connection. Basically the part was designed to not have pins excessively sensitive to transients during cell connection if the currents into the pins are limited by appropriate resistances. This does not mean that the abs maximum limits can be completely ignored or that the part can take unlimited abuse. Differences in implementations may vary the stress on the IC during cell connection and tolerances may also result in differences between successful assembly and damage. The bq76920 is typically more durable in connection than the bq76930 or bq76940 since all cell inputs are in one group and bounded by the power pins.

Connection of the cells assumes connection of the device VSS first since signals in the IC are referenced to VSS. VSS will typically be connected to the high current path of the board and would be connected to battery-. In some cases VSS is connected to battery- through a low current ground.

Generally a bottom-up cell connection sequence is preferred since the voltage step applied to the board with each connection is small. The voltage on the input will charge the filter capacitor for that cell. The differential filter capacitors will push up the unconnected upper cells. Additionally the body diodes of the IC’s internal balance FETs will push up the unused input if they conduct. If external balance FETs are used their body diode will also push up the upper cell terminals through the cell balance resistors. Another cell connection method which is sometimes preferred is to connect the VSS followed by the cell which provides the group power, cell 5 for example in a 5 cell battery. This provides a large voltage step size to the board but defines the power for the group, the differential input filter capacitors divide the voltages to the intermediate pins. Connecting a cell in the middle of the group after the connection of the power will provide a slight correction of the IC pin voltage from the value resulting from the capacitor divider. Unconnected cell inputs are free to drift based on IC pin and capacitor leakages. As with any assembly technique, care should be taken to be sure unconnected inputs do not contact damaging voltages before their connection. This connection of the group power second (after VSS) may be preferred when there is a heavy load on the power such as may be the case with a bq76920 where there is a regulator running on battery+ which might push a high current through the balance FETs during a bottom up sequence. When a cell in the middle of the group is connected after the VSS, a combination of the two effects described above will occur: inputs for unconnected cells above will be pushed up, inputs for unconnected cells below will be divided by the differential capacitor divider.

The external balance circuit used can have an effect on the inputs during cell connection. When P-channel FETs are used for balancing, the inrush current through the input filter resistor will turn on the balance FET. If the cell input below is unconnected, the balance FET will pull up the lower unconnected input. This sequence will continue down the input filter as shown in Figure 18. If the VC0 input is not connected to battery-, it can be pulled to a high voltage. While no damage was observed at TI from this condition in limited testing, connecting the bottom of cell 1 input to VSS on the board at least during cell connection is recommended. N-channel balance FETs do not turn on with a higher-input-after-VSS connection since current into the input resistor raises the upper balance FET source voltage above its gate voltage, see Figure 19. These may be preferred for random cell connection since they do not pull unconnected inputs up. If the N-channel FETs were triggered during connection they would pull an input down, this is generally considered safer than a pull up since single ended abs max limits are referenced to VSS, as long as differential limits are not exceeded.

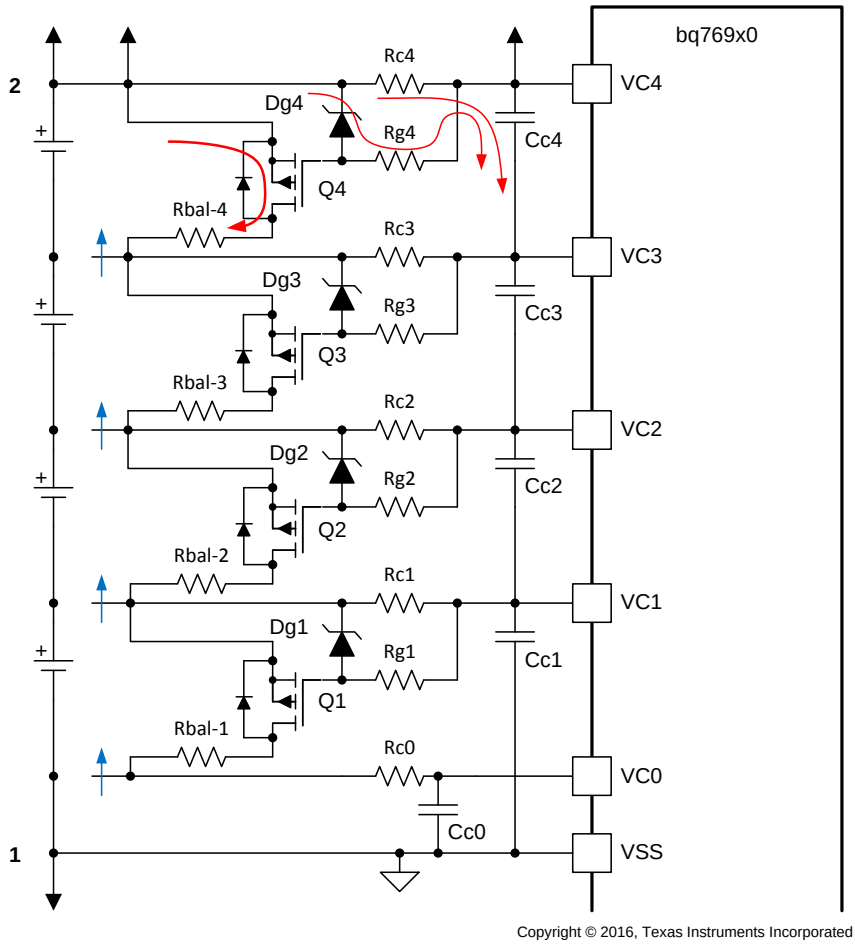

Figure 18. Connection With P-Channel Balance FETs

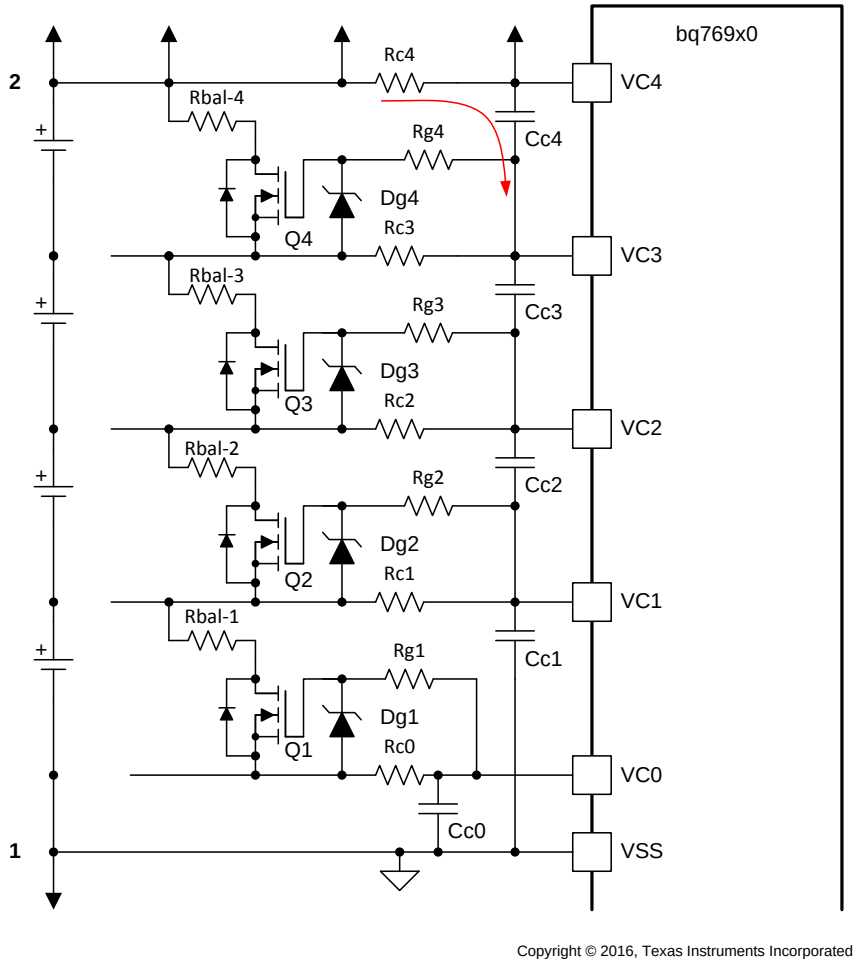

Figure 19. Connection With N-Channel Balance FETs

The typical application schematics in the datasheet for the bq76930 and bq76940 show diodes from the top input of each group to the group power pin. These diodes are important to prevent damage during random cell connection. Without the diode connection of a cell in an upper group will quickly bring that input to a high level while dividing the input voltages to the group power reference pin. The group power reference pin would not move much due to the large Cf required for the architecture and the connected pin may easily exceed its abs max value to the group reference, see Figure 20. Typical damage to the part from this condition leaves the top cell unable to measure high voltage. The diodes hold down the input force current to charge the power filter path as the input rises. Standard signal or switching diodes are suitable for this application. The peak current in the diodes will be limited by the input resistors. With a 1-kΩ Rc resistor with the maximum recommended 5V/cell on VC15, the current would be 75 mA. Current into Cell 10 with a similar condition would be 50 mA

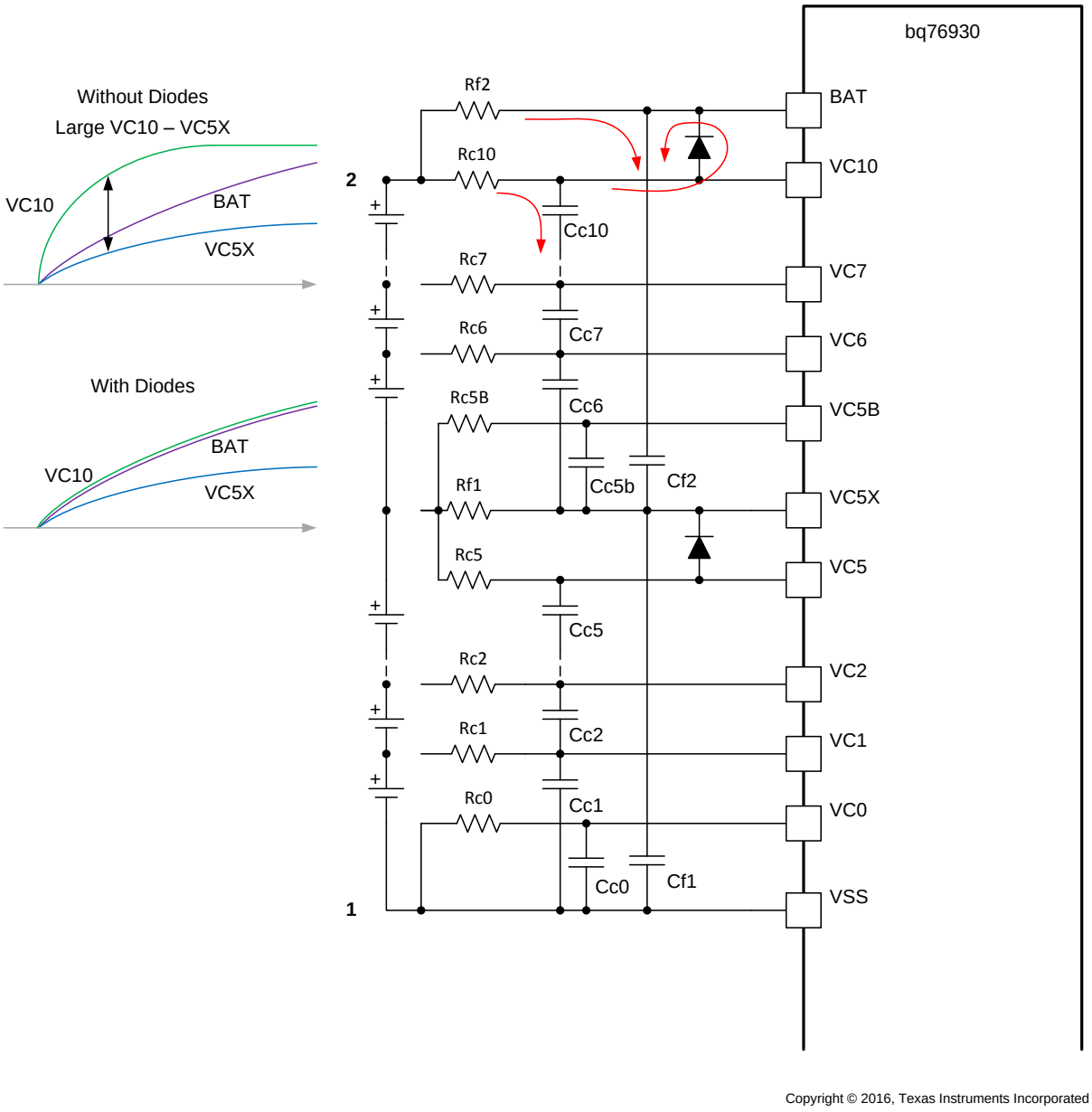

Figure 20. Top Input to Group Power Diodes

The lower cell input pins on the cell groups have the lowest single ended abs max limits at 3.6 and 7.2 V. The internal balance FET on the bottom cell is necessarily different from the top cell since it must operate at the group reference (ground) while the upper cells operate well above the reference. The bottom internal balance FET meets the same specifications as the other internal FETs but is different and may tolerate transients differently. When a connection is made to a bottom cell input of an upper group, the input will rise quickly from the Rc and Cc filter values, the power reference will rise more slowly through the charge path of the upper cell input filter capacitors and power filter capacitors. The bottom of the group sense pin (VC5B, VC10B) could be 6 diode drops above the group power pin, the lower cell sense pin (VC6, VC11) could be 5 diode drops above the group power pin. The reference for the group would be divided from the group power pin by the power filter capacitors. While TI has not experience damage from cell connection in limited testing, the potential voltage could be large and results may vary with different filter capacitors. Some pack designers have found value in zener diodes on the bottom inputs of the group to the group reference or a zener across the inputs. An example is D11 and D10B shown in Figure 21

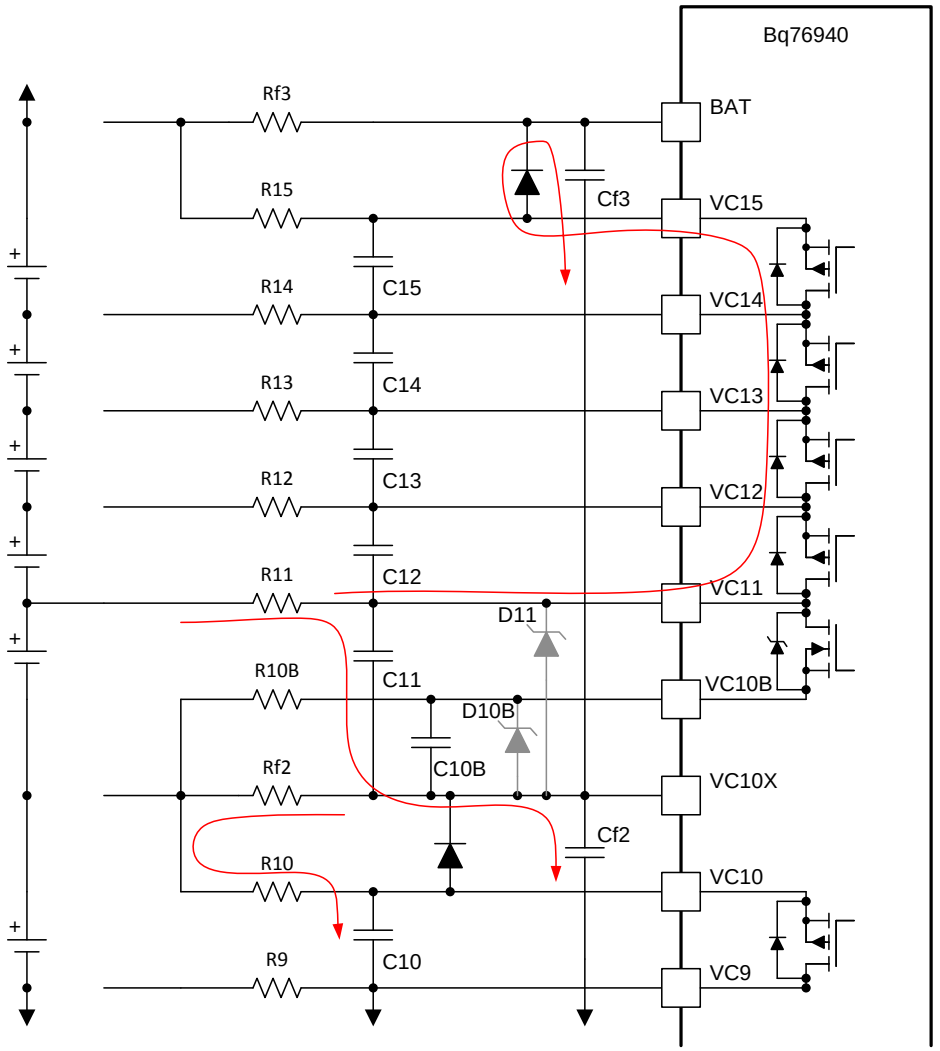

Figure 21. Limiting Lower Group Pin Voltages

One possibility to help protect the pack inputs is to provide a zener across each cell input. Such zeners can help but may not prevent all issues. Zeners placed at the board inputs must have a nominal breakdown above the cell maximum value and will have a tolerance. These zeners can keep the board differential inputs from an excessive value, but If there is a 0.5V allowance between the maximum cell voltage and the zener conduction point, and if the cells are connected at 0.5V below maximum voltage, each input could accumulate a 1V error. Also realize that with the filter the IC input pins can have a different voltage than the board inputs. Placing zeners at the IC inputs is also possible and can help control voltage swings, however the voltages at the IC inputs will be approximately 1.5 to 2 times the cell voltage during cell balancing depending on the algorithm used.

When possible, connecting zeners to the board in an assembly fixture during assembly may allow a tighter tolerance during connection which would be unacceptable if left in the product during operation while avoiding the cost of the parts in the product. Resistors can also be used to divide the voltage during connection. Resistors would be unacceptable in a product and must be used carefully in a fixture. If the connection to the top cell of a resistor divider is broken, the divider may hold the next to top cell at 0V while the top input goes to the full pack voltage.

Related to the random cell connection, the placement of the IC "ground" may affect the signals on the pins. Parasitics in the high current connection to battery- can cause transients against which the IC may need protection. A resistance between the sense resistor and battery- can cause a voltage drop. If the value is too large, the IC could be damaged. If VSS is referenced near the sense resistor, VC0 will tend to go below ground if connected to the cell and may need protection such as DVC0 in Figure 22. If VC0 is connected on the board, it will not vary significantly from VSS, but the parasitic effect will be included in the bottom cell measurement and VC1 may need protection, see Figure 23. If VSS is referenced to a low current cell 0 connection, the SRP and SRN sense inputs may rise above VSS and transient protection may be required as shown in Figure 24. Note that the recommended operating range of the SRP pin is small, a large path resistance in the will increase the common mode voltage at the SRP and SRN pins.

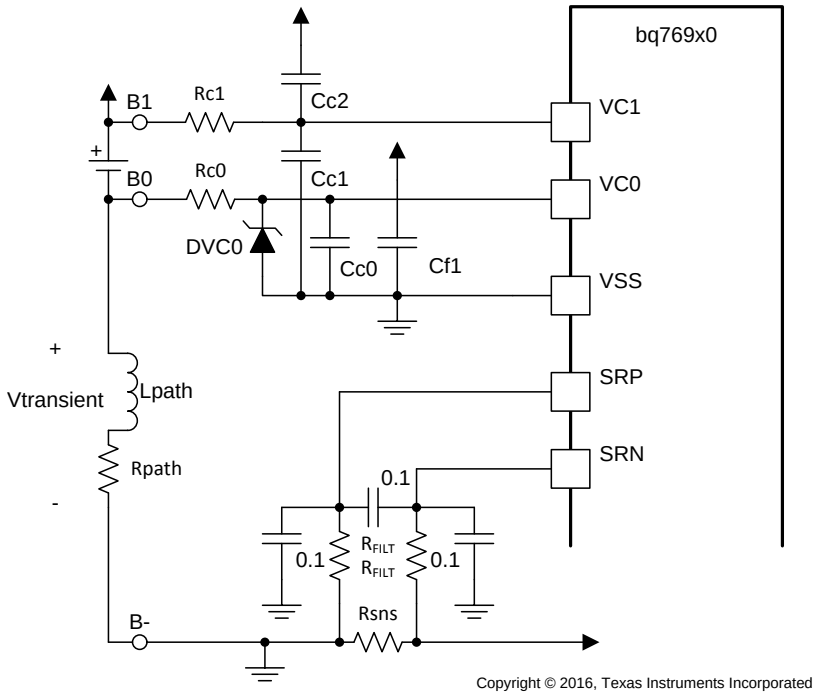

Figure 22. Ground at Sense Resistor and Remote Cell Sense

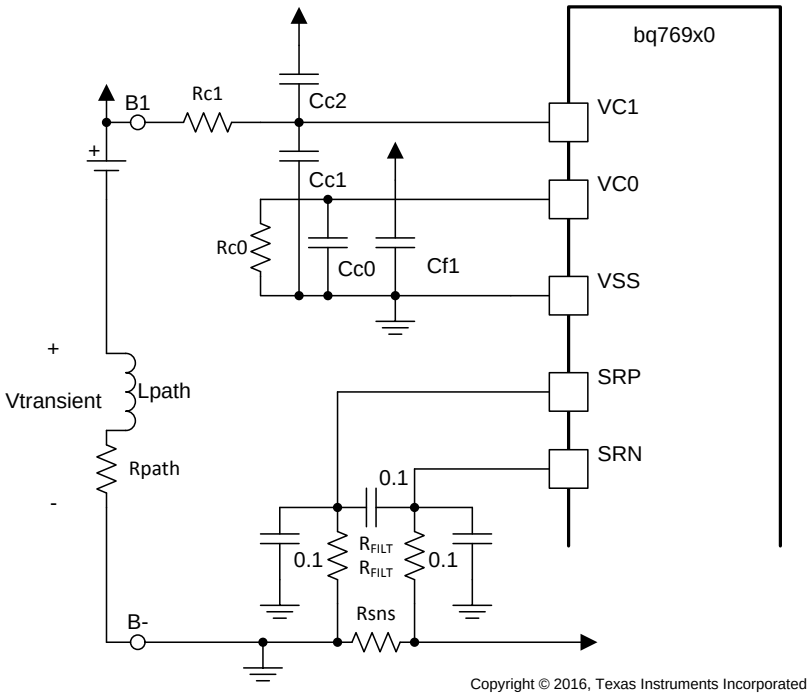

Figure 23. Ground at Sense Resistor and Local Cell Sense

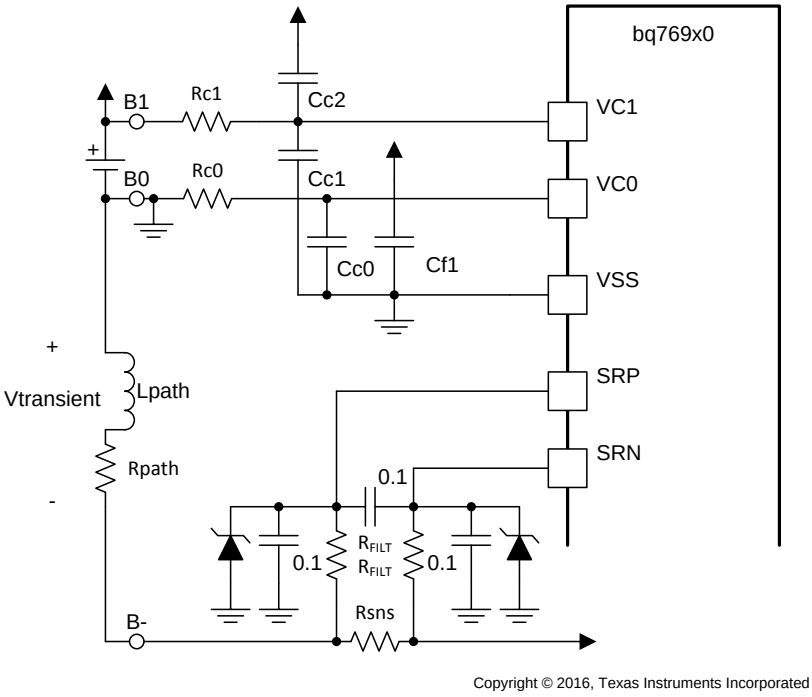

Figure 24. Ground at Remote Cell Sense

11 References

The documents may provide additional information on the bq769x0. Documents are available on www.ti.com or check with your local sales office. Check in the website product folder for additional documents.

1. *bq769x0 3-Series to 15-Series Cell Battery Monitor Family* data sheet (SLUSBK2)
2. *bq76920 EVM User's Guide* (SLVU924)
3. *bq76930 and bq76940 Evaluation Module* user's guide (SLVU925)
4. *bq78350 CEDV Li-Ion Gas Gauge and Battery Management Controller* data sheet (SLUSB48)
5. *bq76920, bq76930, bq76940 AFE FAQ* (SLUUB41)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2015) to A Revision	Page
• Changed Figure 19, Rg1 to VCO connection	19

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265