Application Report

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THD Reduction of DCM PFC With UCD3138

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ABSTRACT

An active PFC stage is an indispensable part to reduce the harmonic content of input currents. In order to reduce the total cost, the inductance of the PFC choke is made extremely small in more and more practical designs. However, in existing UCD3138 single-phase PFC solutions, the input current distortion in DCM (discontinuous conduction mode) is greater than that measured in large choke-inductance PFC designs. Thus, in small choke-inductance PFC designs, it is difficult to meet the THD (Total Harmonic Distortion) specification at light load levels. This paper analyzes the root cause of the significant input current distortion in DCM and proposes a simple method to reduce THD at light load levels.

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1 Existing Solution, Introduction

The existing single-phase PFC solution based on UCD3138 is shown in Figure 1.

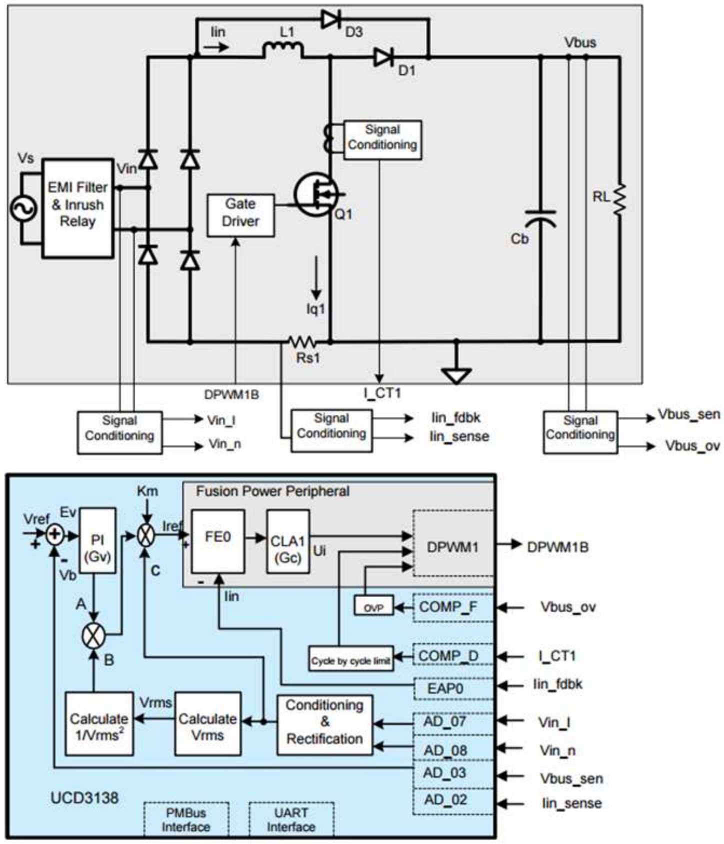

Figure 1. UCD3138-Controlled Single Phase PFC Block Diagram

Average-current mode control is employed to force the input current to track the input voltage. Figure 2 shows the block diagram of the current loop. I_reference is calculated by firmware and follows the product of input voltage and the output of the outer voltage loop.

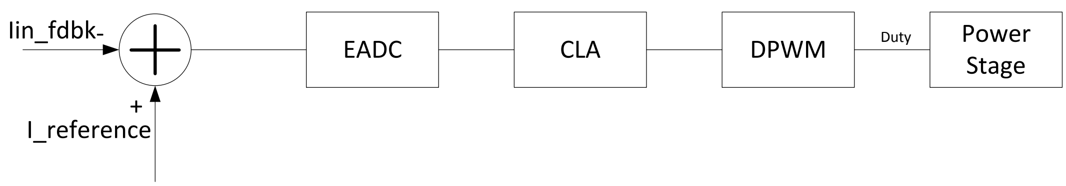

Figure 2. Current Loop Diagram of UCD3138 PFC Solution

The input current sensing result, Iin_fdbk, is from current shunt Rs1 and the signal conditioning circuit which is formed by an operational amplifier used to amplify the current signal to a level suitable for the PFC control circuit. The error between I_reference and Iin_fdbk is the analog input of EADC (Error ADC) which converts its analog error input into a digital form used for duty-cycle calculation by Control Law Accelerator (CLA). Since the current signal conditioning circuit does not provide sufficient attenuation of the input current ripple, the ripple still appears at the input of the EADC. The existing solution utilizes an oversampling mechanism (refer to SLUA709) to average out the ripple. In the oversampling mechanism, as shown in Figure 3, the instantaneous input current is sampled 8 times, distributed equally in time, per switching cycle. The average value of 8 samples is used for the duty cycle calculation.

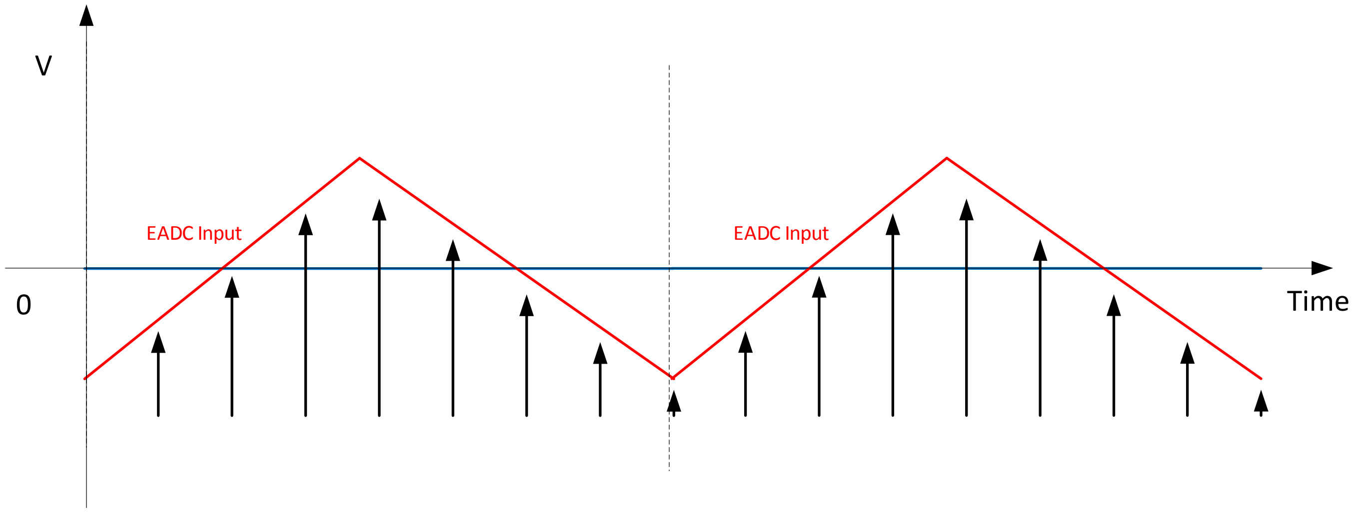

Figure 3. Oversampling Mechanism for Average Input-Current Measurement

In order to avoid EADC saturation, the EADC input at the sample instant which is indicated by an arrow must be within the EADC measurement range, –255 mV to +255 mV. Otherwise, the conversion result is clamped to either the maximum or minimum value. When the inductance of the PFC choke is so small as to cause the pk-pk magnitude of Iin_fdbk to exceed 512 mV, then EADC saturation is unavoidable. But the correlation between EADC saturation and input current distortion depends on the convertor's operation mode, CCM or DCM.

1.1 EADC Saturation Does not Cause Input Current Distortion in CCM Operation

In steady-state CCM operation, the average error between I_reference and Iin_fdbk per switching cycle, is very close to 0 due to the closed-loop control of the current loop. The analog input of EADC is shown in the left side of Figure 4. The positive and negative peak values are equal. The solid line in the right picture represents the EADC conversion result and the zones A, A', B, and B' represent truncation error due to EADC saturation. It is obvious that the area of A and B is equal to that of A' and B', so it is clear from a mathematic perspective that the truncation error makes no difference between the actual average EADC input in one switching cycle and its digital conversion result which is important for the calculation of duty cycle. That is why there is no input current distortion in CCM operation even though the small inductance of the PFC Choke causes EADC saturation.

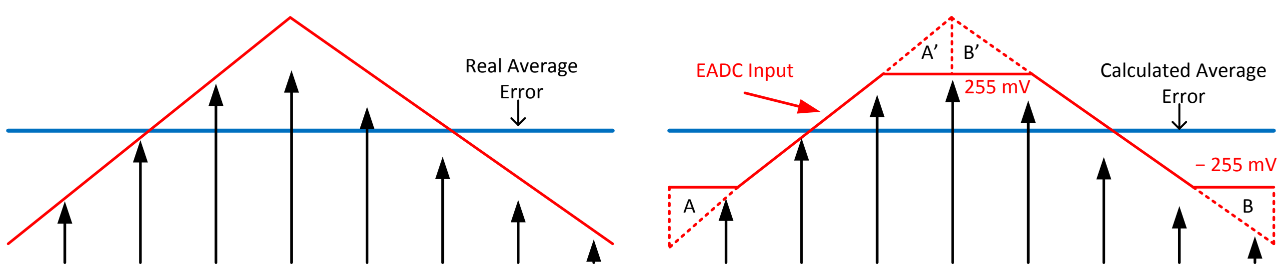

Figure 4. Current-Error Sensor Saturation Analysis in CCM Operation

1.2 EADC saturation does cause input current distortion in DCM operation

As in CCM control, the average error between the scaled input current (Iin_fdbk) and I_reference per switching cycle is also close to 0. However, the peak value of the positive error is much higher than that of the negative error in the same switching cycle as shown in Figure 5. Hence, the truncation of positive and negative in one switching cycle is unbalanced and the conversion result of the average error per switching cycle is not equal to the actual average error, which causes input current distortion in DCM operation and large THD at light-load levels.

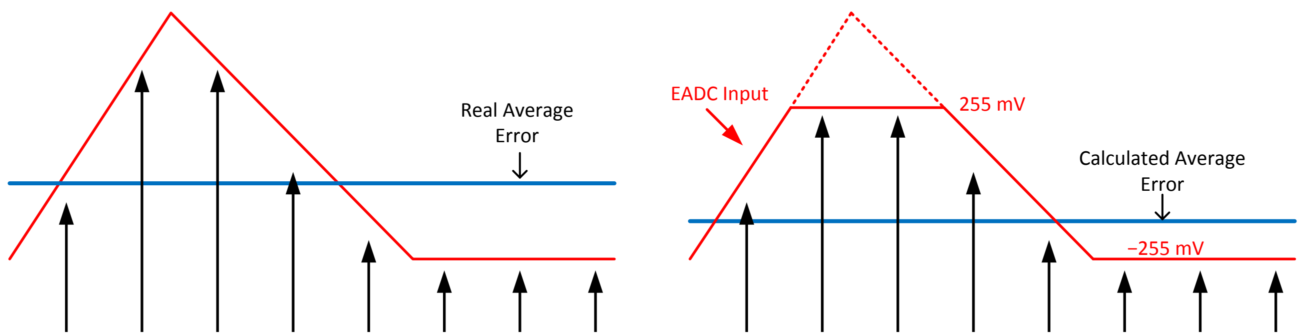

Figure 5. Typical Input Signals of DCM PFC Current Loop

2 Proposed Solution

As previously discussed, EADC saturation must to be avoided in order to eliminate the input current distortion in DCM operation. Oversampling is not suitable for the current loop error sensing in small choke-inductance PFC applications. A single-sample-per-switching cycle is the best way to address the EADC saturation problem. At the same time, in order to get good THD, the instantaneous current at the single sample instant must represent the average current of the whole switching cycle. Refer to SLUA712, the best sample location is at the middle of the PWM on time. Since the closed-loop control is able to force its input error to be 0 at steady state operation, the input of EADC at sample instant is always close to 0 for both CCM and DCM operation.

3 Implementation of Proposed Solution

This section describes in detail the method to reduce THD in DCM PFC. THD in DCM PFC is reduced significantly by following the method step by step.

3.1 Configure DPWM Mode to Triangle Mode

3.1.1 Introduction of Triangle Mode of DPWM

There are many DPWM modes in the UCD3138 DPWM module. In triangular mode, the PWM pulse is centered in the middle of the period, rather than starting at one end or the other. In triangular mode, only the DPWMB output is available. Figure 6 is a diagram for triangular mode.

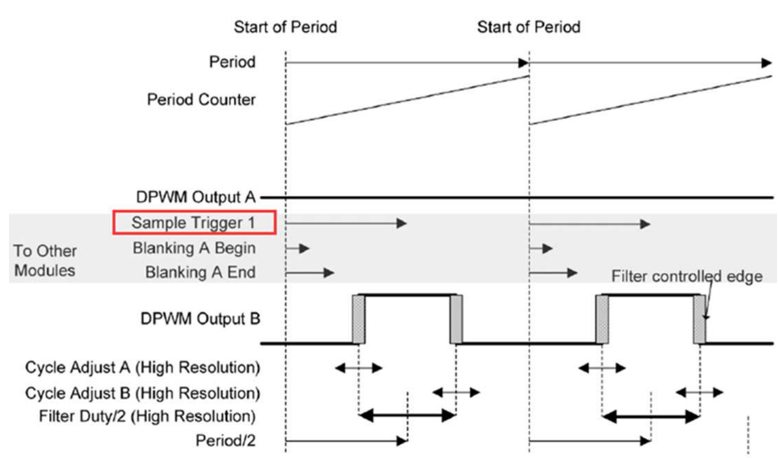

Figure 6. Diagram for Triangular Mode

3.1.2 Firmware Configuration of DPWM Mode

Configure the PWM mode to triangular mode as in the following:

```
Dpwm1Regs.DPWMCTRL0.bit.PWM_MODE = 3;
```

3.2 Disable Oversampling

The EADC converts the analog error signal only once per DPWM period if oversampling is disabled. In this application note, oversampling must be disabled, the configuration of oversampling in firmware follows:

```
Dpwm1Regs.DPWMCTRL2.bit.SAMPLE_TRIG1_OVERSAMPLE = 0;
```

3.3 Configure Sample Trigger Point to ½ Period

3.3.1 Introduction of ½ Period

Since DPWM mode is configured to triangular mode, the PWM pulse is centered in the middle of the period. If the sample trigger point is set to ½ of the period, then the sample trigger point is just at ½ PWM on time, as shown in Figure 7. Since the input signal is not saturated at this time, the calculated error used for the duty cycle calculation is accurate enough for good THD.

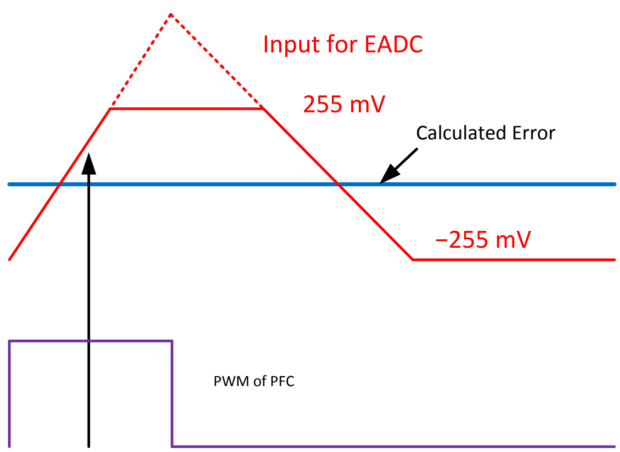

Figure 7. Proposed Sample Trigger Point in DCM PFC

3.3.2 Firmware Configuration of Sample Trigger Point

The current sample trigger point is configured for the middle of the period, the configuration of the sample trigger point in firmware follows:

```
Dpwm1Regs.DPWMSAMPTRIG1.all = (iv.switching_period >> 1) + (iv.sample_trigger_offset * 4);
```

iv.switching_period is the value of the switching period register, the resolution is 4 ns
iv.sample_trigger_offset is the delay compensation of driver circuit, the resolution is 250 ns

3.4 *Configure the Calculation of Current Reference to CT Method*

The current target calculation for the current loop for DCM PFC without oversampling, shown in the following image, is the same as the CT method used on the UCD3138PFCEVM. For the principle used by the CT method to calculate current target of current loop, please refer to SLUA712.

Firmware for calculation of the current reference follows:

```
int32 pointer;

//for EMI CAP compensation
iv.cir_buff[iv.cir_buff_ptr] = iv.vin_filtered;
pointer = (iv.cir_buff_ptr - iv.cir_buff_delay) & 0x3f; //get pointer to delayed signal
iv.cir_buff_ptr = (iv.cir_buff_ptr + 1) & 0x3f;

iv.vbus_scaled = (iv.adc_avg[VBUS_CHANNEL] * VBUS_TO_VAC_SCALING) >> 15;
//scale vbus to match scale of vrect  Q12 * Q15 >> 15 = Q12

if(iv.vbus_scaled > iv.vin_filtered)
{
    iv.numerator_1 = iv.vbus_scaled - iv.vin_filtered; //Q12
}
else
{
    iv.numerator_1 = 0; //if vrect greater than vout, don't need any boost.  shouldn't happen often
}

iv.numerator_2 = (iv.i_target_average * iv.numerator_1) >> 8; //Q14 * Q12 >> 8 = Q18

iv.numerator_3 = (iv.cir_buff[pointer] * iv.numerator_2); //Q12 * Q18 = Q30

iv.cla1_output_filtered = (Uint32)Filter1Regs.FILTERYNREAD.bit.YN + iv.cla1_output_filtered -
                                      (iv.cla1_output_filtered >> 2);//Q25

iv.denominator = ((iv.cla1_output_filtered >> 6) * iv.vbus_scaled) >> 11; //Q19 * Q12 >> 11 = Q20

iv.i_target_sensed = (iv.numerator_3 / iv.denominator) + iv.i_target_offset; //Q30/Q20 = Q10

if(iv.i_target_sensed > 0x3ff) //saturate current target at maximum current
{
    iv.i_target_sensed = 0x3ff;
}

FeCtrl0Regs.EADCDAC.bit.DAC_VALUE = iv.i_target_sensed << 4;//1211
```

4 Test Results With Different Current Sample Methods

Change the PFC inductance to 180 µH from 330 µH on UCD3138PFCEVM to make the PFC work in DCM. By using the middle current sample PWM method and disabling oversampling of the EADC, the THD is significantly reduced, as shown in Table 1.

Table 1. Test Results With Different Current Sample Methods

Shunt+ Oversampling		Shunt+ Middle Point Sample	
UCD3138PFCEVM With 180 µH PFC inductor			
115/60 Hz		115/60 Hz	
Load	THD	Load	THD
390 V × 0.1 A	10.47	390 V × 0.1 A	2.83
390 V × 0.2 A	7.62	390 V × 0.2 A	1.82
390 V × 0.3 A	6.93	390 V × 0.3 A	1.28
390 V × 0.4 A	5.43	390 V × 0.4 A	1.26

5 Conclusions

This application note shows a simple method to reduce THD in DCM PFC. It only needs a modification of the firmware, hardware modification is not needed. This document also shows that THD in DCM PFC is significantly reduced with this new method.

6 References

1. *Design a UCD3138 Controlled Interleaved PFC* (SLUA712) — Bosheng Sun
2. *UCD3138 Digital Power Peripherals Programmer's Manual* (SLUU995A)