Application Report
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bq76PL455A-Q1 Design Recommendations

Roger Hwang *Battery Management Solutions / Monitoring and Protection*

ABSTRACT

The bq76PL455A-Q1 is 16-cell battery monitoring and protector device, for automotive and industrial applications. This document provides design considerations and a checklist for using the bq76PL455A-Q1 in a battery system. For best performance, use the design recommendations in this application report. This document provides some of the specific recommendations which must be implemented for a successful battery system using the bq76PL455A-Q1

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Trademarks

1 NPN LDO Supply

The bq76PL455A-Q1 is powered from the same cells it monitors. The bq76PL455A-Q1 generates the additional VP and VDIG supplies used in operation from this input.

VP1 is the input for the external LDO supply for the bq76PL455A-Q1. Figure 1 shows the typical circuit.

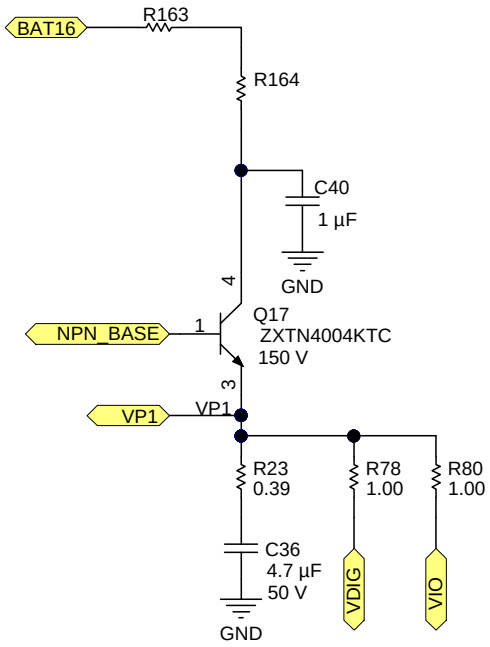


Figure 1. Power Supply Schematic

Select the NPN Transistor based on the following criteria:

1. *Collector-Emitter Breakdown Voltage* (BV_{CEO}) > 100 V (or the module voltage, plus any derating)
2. DC gain (β, or approximately equal to hfe (AC gain)) > 100 at the expected load current
3. Collector-based capacitance < 35 pF at typical base-voltage range
4. Power handling > 500 mW (this assumes a 1-kΩ resistance in series with the collector)
5. Current handling > 100 mA

The series resistors R163 and R164 in Figure 1 serve several purposes:

1. Limit the current in the event of a fault
2. Shift some constant power dissipation in the regulator away from the transistor onto the resistor
3. Combine with the input capacitor on the transistor collector to serve as a filter

To calculate the required resistance, use :

$$R_{MAX} = \frac{\left(V_{MODULE(min)} - \left(VP_{MAX} + V_{CE(SAT)}\right)\right)}{31\,mA + I_{LOAD}}$$

where

- $V_{CE(SAT)} = V_{CE}$ min at $V_{BE(on)}$, from transistor datasheet
- 31 mA is the bq79PL455A maximum inrush current at startup
- I_{LOAD} is the expected current for any non-bq76PL455A external loads applied to the VP pin

1. The R78 and R80 series resistors in the VDIG and VIO supplies, respectively, isolate large load capacitance from the voltage regulator to help with loop stability.
2. Connect a filter on the VP supply (R23 and C36) for stability. Use R23 = 390 mΩ and C36 = 4.7 µF.

Design Considerations

1. Select R163 and R164 from the R_{MAX} formula. R_{MAX} is calculated based on the minimum module voltage but should consider the thermal heat of resistors with the maximum module voltages. The resistor can be in series and parallel to spread out the heat, if board space permits.
2. A capacitance of 1 µF is recommend for C40 but it can be up to 2.2 µF, if R_{MAX} is reduced to 200 Ω. It is a good practice to have 2 capacitors in series, in case one capacitor gets shorted. There could be hundreds of mA depending on the number of cell counts if C40 is damaged and shorted to GND.
3. The Q17 transistor must meet bq76PL455A-Q1 requirements
4. The VP filter is critical, TI recommends using R23 = 390 mΩ and C36 = 4.7 µF
5. A 1-Ω resistance of R78 and R80 series resistors in the VDIG and VIO (respectively) supplies is a **must have** for isolating large load capacitance from the voltage regulator to help with loop stability

2 TOP and VSENSE16

To ensure that the voltage between Top and VSENSE16 do not violate the absolute maximum rating and operating condition during hot-plug, connect the VSENSE16 input or highest sense input to the TOP pin.

Design Considerations

1. Top input must include a low-pass filter with 100 Ω and 0.1 µF. R1 should be in the range of 100 Ω to a maximum of 300 Ω to avoid voltage stress during hot-plug.
2. Back-to-back diode D1 and D2 should be able to withstand the continual current in the event of an open wire on VSENSE16 and also to withstand inrush currents during the hot plug. Use a diode that has a higher Vf, not a Schottky diode which has low Vf. The 1N4148W is used on the reference design.
3. Connect a TVS diode, Z1, to TOP to clamp the voltage below 88 V and prevent an overvoltage condition on TOP during hot-plug and other transient event
4. Connect VSENSE pins to VSENSE16 as Figure 3 shows

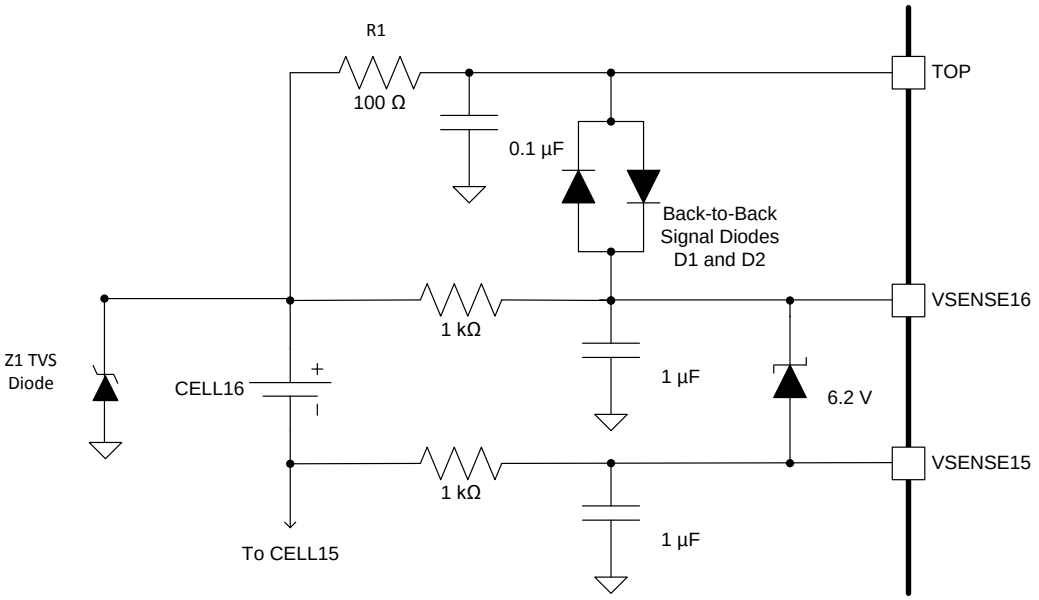


Figure 2. Connecting TOP and VSENSE16

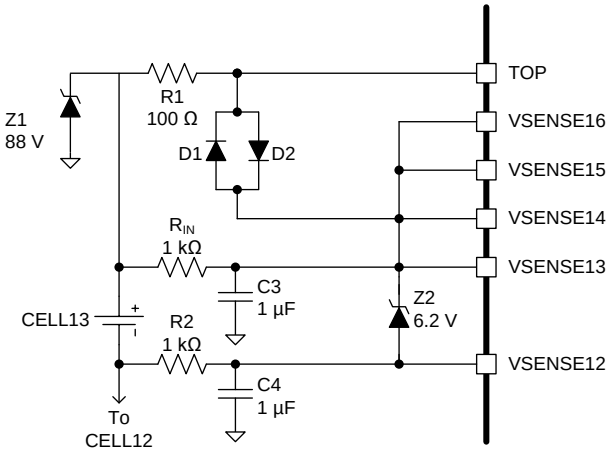


Figure 3. Connecting Less Than 16 Cells

3 VREF and V5VAO

VREF output filter pin. Decouple with parallel 0.1-µF and 1.8-µF (25 V+) capacitors to the ground plane. Locate decoupling capacitors as close to the pin as possible. To maintain measurement fidelity, do not place external loads on this pin.

V5VAO is connected to an internal 5-V always-on supply. Decouple with a 4.7-µF capacitor connected to the ground plane. Place the decoupling capacitor as close to pin as possible. Do not use this pin to supply external circuitry.

Design Considerations

1. Both VREF and V5VAO are used for very sensitive internal circuits and **should not** be used to supply external circuits.
2. Decouple a 4.7-µF capacitor on the V5VAO pin to the ground plane. Put the capacitor as close to pin as possbile.
3. A good temperature coefficient for VREF is needed.
    1. All capacitors are X7R or better

2. Must be up to, but not exceed 2 µF
3. The best option is 1.8 µF + 0.1 µF, but 1.8-µF capacitors are only available from a few vendors

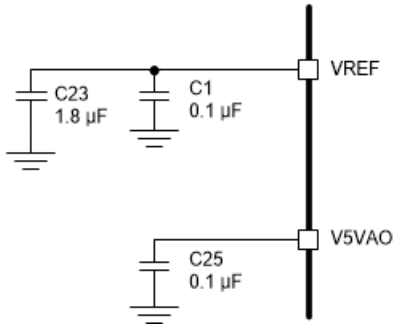


Figure 4. Connecting VREF and V5VAO

4 CHM, CHP, and VM

VM is an internal –5-V charge pump output. It requires an external flying capacitor connected between the CHP and CHM pins plus a storage capacitor on the VM pin to generate a rail of –5 V for internal use. The charge pump (VM) is always on in IDLE and off in SHUTDOWN. VM requires the oscillator to be running and stable and does not start until the other supplies are above their POR thresholds. The VM charge pump will start ramping at the start of the WAKEUP tone on COMH.

Design Considerations

1. Connect a 22-nF *flying* capacitor between CHP and CHM
2. Decouple with 4.7-µF and 0.1-µF capacitors to VM pin and locate them as close to VM pin as possible.

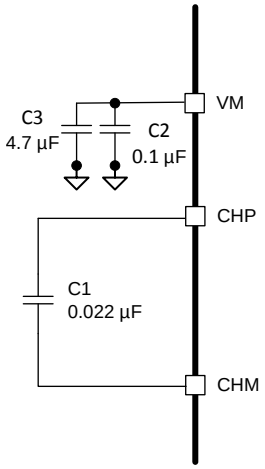


Figure 5. Connecting VM, CHP and CHM

5 AGND and VSENSE0

To ensure that the voltage between VSENSE0 and AGND1 does not violate the absolute maximum and recommended operating conditions during hot-plug or other unusual conditions, connect the VSENSE0 input to the AGND1 pin using two back-to-back signal diodes. Select diodes with a high enough current rating to withstand the continuous currents during a wire disconnect and the inrush currents during hot plug. Use diodes that have a higher Vf, such as an ultra-fast or fast diode. Low Vf diodes, such as Schottkey diodes, must not be used because noise on AGND may couple onto the VSENSE0 input. Additionally, connect a 1-µF capacitor between VSENSE0 and AGND1. Figure 6 illustrates the correct VSENSE0-to-AGND1 connection.

Design Considerations

1. Connect back-to-back diodes between AGND to VSENSE0. The 1N4148W is used on the reference design.
2. Connect a 1-µF capacitor between VSENSE0 and AGND.

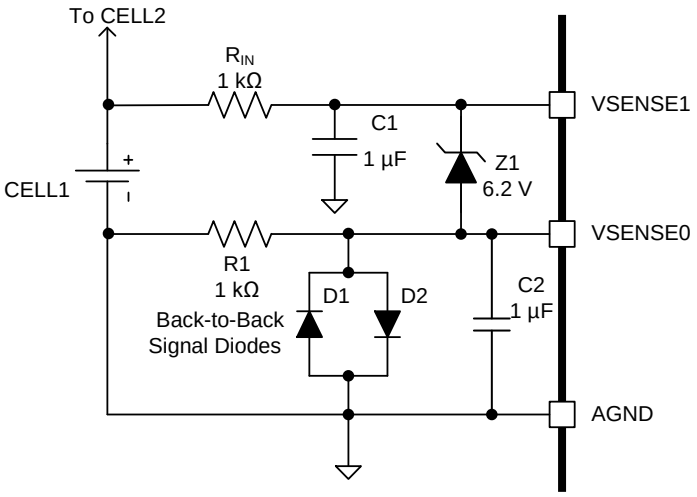


Figure 6. Connecting AGND and VSENSE0

6 VSENSE to VSENSE Connections

To ensure that the voltage between the VSENSE_ inputs (VSENSE0 to VSENSE1, VSENSE1 to VSENSE2, and so forth) does not violate the absolute maximum rating and recommended operating condition during hot-plug or other unusual conditions, Zener diodes must be connected between the VSENSE input pins, as close as possible to the inputs. One Zener diode across every input is advised. The Zener diodes provide overvoltage protection and a path for inrush current during a hotplug event. Figure 7 illustrates the correct VSENSE-to-VSENSE connection.

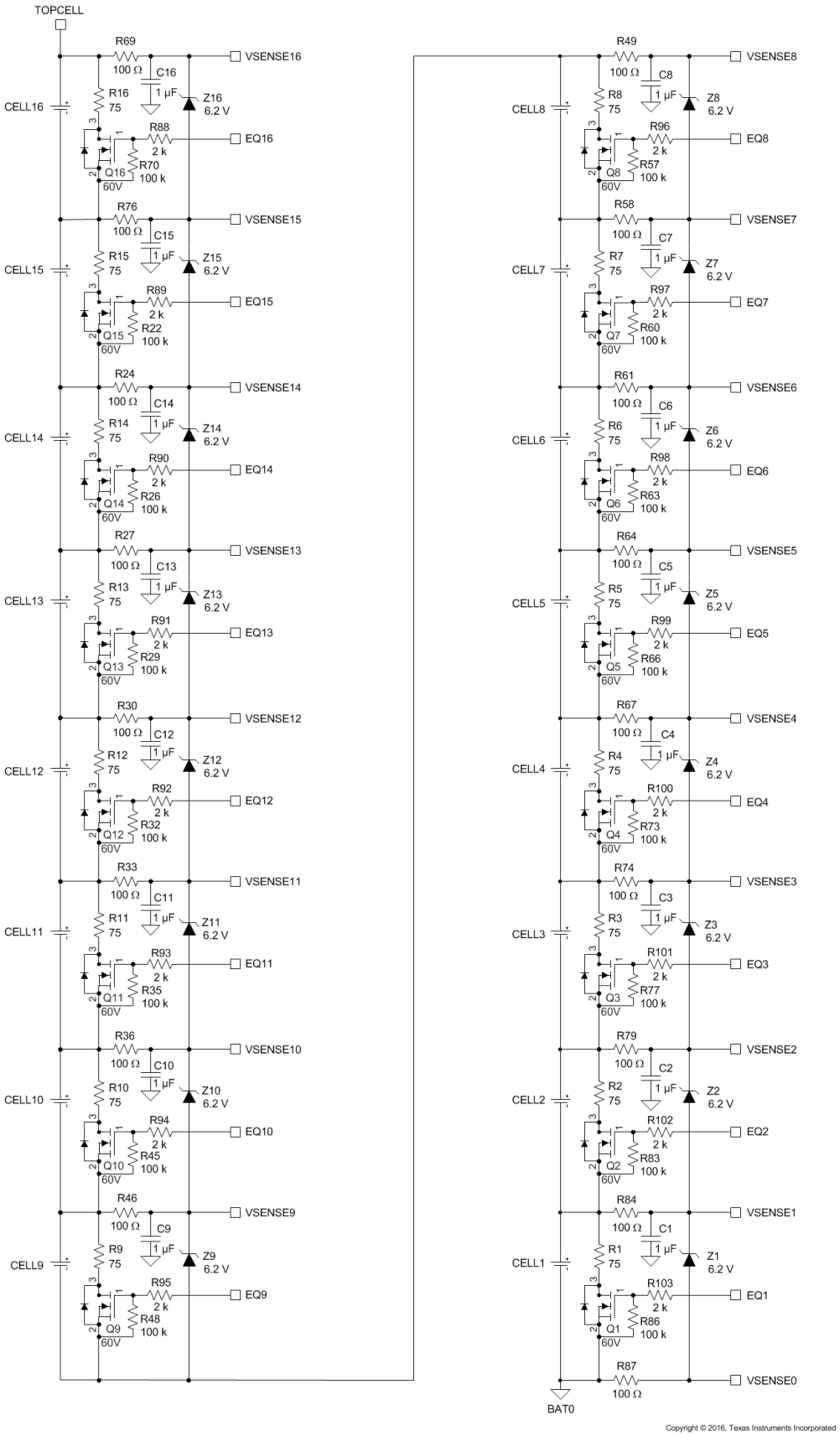


Figure 7. bq76PL455A-Q1 Front-End Circuit

Selecting Zener diode for VSENSE(Z15, Z16):

1. The bq76PL455 inputs are protected from input voltage transients greater than 5.5 V. Any transients greater than 5.5 V must be clamped to less than 6.5 V for an accumulative time duration not to exceed 0.1% of the device 10-year lifetime.
2. The Zener diode maximum reverse current (I_z) at normal battery-cell voltage levels are as low as possible to keep the quiescent system-current draw low. Additionally, any leakage through the Zener diode affects the total channel accuracy measurements as it adds to the voltage drop across the filter resistor.
3. The Zener must be capable of withstanding instantaneous or continuous currents that the bq76PL455A-Q1 experiences during fault events. These events can include cable connect or disconnect, inrush, or reverse battery voltage. Depending on the fault and the direction of current flow, the maximum power dissipation for the Zener diode must not be exceeded, to stay within maximum operating conditions.

A series resistor and bypass capacitor are required for each of the VSENSE inputs. The series resistor (R69 and R76 in Figure 7) serves four functions:

1. They protect the AFE inputs from in-rush currents during hot plug-in. This requirement limits the input series R to a minimum of 100 Ω. Keep this resistance as low as possible to minimize input voltage offset, which is also subject to drift over temperature. These requirements limit the maximum value to 1 kΩ. Error due to input bias currents on the front end of the AFE, is directly proportional to the value of the resistors. The voltage measurement error can be calculated as:

   voltage measurement error = $2 \times R \times I_{SENSE}$ (1)
2. The resistor and capacitor (R69 and C16 in Figure 7) provide an RC filter for high-frequency noise on the AFE inputs. The tuning of this filter cutoff is adjustable and depends on the expected frequency of noise in the system. Calculate the cutoff frequency using the following equation:

$$fc = \frac{1}{2\pi R1C1}\ Hz \quad (2)$$

3. Ensure that the RC-filter components are as close to the device as possible. The capacitor location is extremely important and must be given priority for optimum performance.
4. For applications that require a very low filter cutoff frequency, connect a differential capacitor between the VSENSE lines to provide the bulk of the AFE input filtering. The bias voltage on these differential capacitors are the same (or very close), therefore, anti-aliasing is improved.

Design Checklist:

1. Select a Zener diode with the lowest reverse current and that meets the criteria described in this section.
2. R69 and R76 should not exceed 1 kΩ and the filter should be as close to the device as possible.

7 Balancing Circuit

Balancing FET

Select the Balance FET (Q15 and Q16) based on the following criteria:

1. The V_{DS} must be selected based on derating requirements determined by the stack voltage.
2. V_{GS} must be as large as possible and preferably have ESD protection from gate to source. This protects the part during hot plug.
3. The V_{GS} threshold is of concern only if the discharge resistors are going to be turned on at low-battery voltages.

The 2V7002K is recommended because of its 60 V_{DS}, ±20 V_{GS}, and the gate is ESD-protected with an internal Zener diode.

The R_{DS} value is of little consideration with the discharge currents for this application.

The V_{GS} resistors (R70 and R22) ensure that the gate of the FET is turned off and does not float into a linear or on state causing excessive leakage currents on that cell in case of FET failure or PCB open.

A series resistor between the EQ pin and the FET gate limits current going into the FET during hot plug or other transient events.

Balancing Resistor

The balancing resistors (R15 and R16) set the required balance current. If used, the resistors in series with the cell connections (top and bottom, in front of the Zener diode) must be included in this calculation. These resistors must be sized appropriately to handle the thermal dissipation of continuous cell balancing.

Balancing Zener

The balancing Zener diode is not required if the 60 V_{DS}, ±20 V_{GS} requirement is satisfied. If the balancing FET does not meet the requirement, then a Zener diode is necessary to protect the device during hot plug.

Design Checklist:

1. Select proper FETs for Q15 and Q16.
2. Consider thermal for R16 and R15. They set the balancing current.
3. R70 and R22 are needed to make sure the FET does not float when it is turned OFF.
4. R89 and R88 limit current in hot-plug.

8 OUT1,2

OUT pins are the connection between the analog front end (located on the analog die) and the ADC (located on the digital die). A 390-pF capacitor type C0G or NP0 between OUT pins to GND is strongly recommended with ADC settings for best ADC measurements.

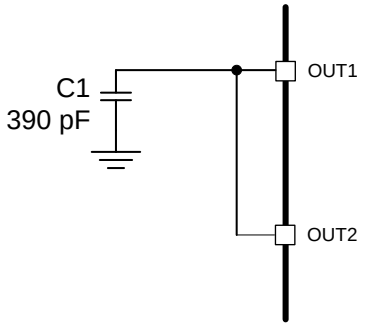


Figure 8. Connecting OUT1 and OUT2

9 AUX Input Channels

Typically, 8 AUX ADC inputs are used to monitor externally-supplied temperature sensors and other sensors with an input voltage range of 0 V to 5 V.

For best performance, the AUX inputs require a series of resistor and bypass capacitors for filtering. Recommendation is to connect a 1-kΩ and 1-µF filter as Figure 9 illustrates.

A differential AUX measurement is recommend for extremely noisy environments as shown in Figure 9.

Unused AUX inputs can be allowed to:

1. Float
2. Tie to local GND
3. Pull up to VP/VDIG with a 100-kΩ pullup

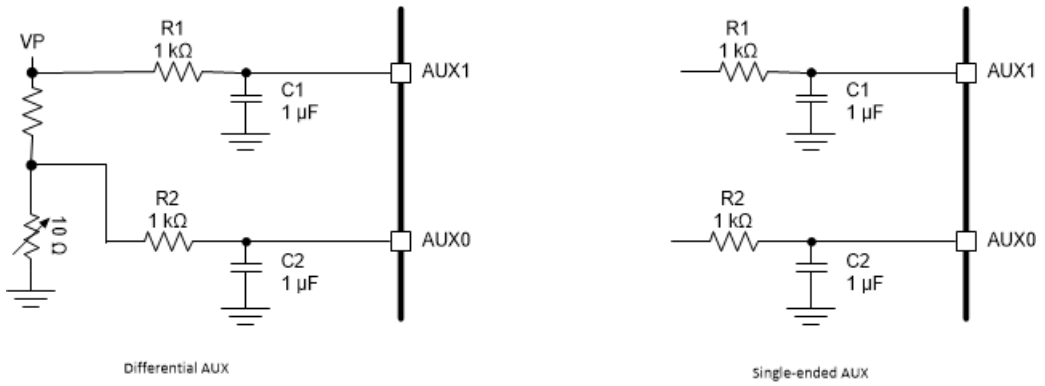


Figure 9. Connecting AUX Pins

10 General Purpose Input-Output (GPIO)

There are six GPIO pins available in the bq76PL455A-Q1. Register GPIO_xxx is located at addresses 0x78-7D and controls GPIO behaviors. Each register can be programmed to be an input or output pin. When DEVCONFIG[ADDR_SEL]==0, the device uses the address sampled from GPIO[4:0] to set ADDR. The address is sampled as part of the reset process or by setting DEV_CTRL[AUTO_ADDRESS].

GPIO pins are all programmed as inputs, no pullup or pulldown resistors are enabled, leaving the inputs floating. The pins should not be allowed to remain as floating inputs. The pins should be reprogrammed to become outputs or add a pullup or pulldown if none are provided externally.

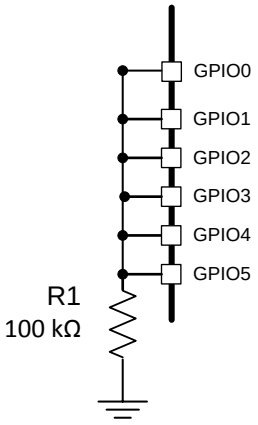


Figure 10. Example of GPIOs Configured as Input Without External Source

Design Checklist:

- GPIO pins are all programmed as inputs, no pullup or pulldown resistors are enabled, leaving the inputs floating. The pins should not be allowed to remain as floating inputs. Reprogram the pins to become outputs or add a pullup or pulldown as shown in Figure 10, if none are provided externally.

11 WAKEUP

The WAKEUP pin must be held in the low state to allow the device to enter and remain in the SHUTDOWN state. If the WAKEUP pin remains in the high state, the device will cycle off and immediately back on. Operation is unpredictable if the WAKEUP pin floats, ensure the WAKEUP pin is kept in a defined state. Setting the WAKEUP pin low does not put the device in the SHUTDOWN mode.

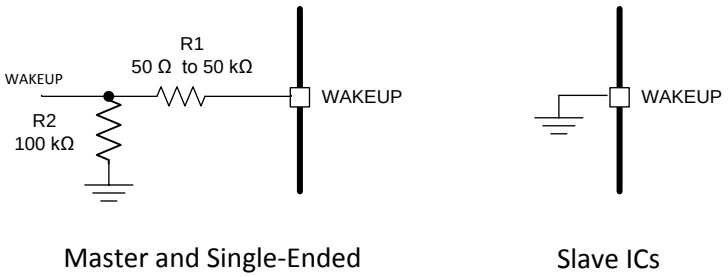


Figure 11. Connecting WAKEUP

Design Considerations

1. Connect WAKEUP to local GND for all Slave ICs
2. Add 0.1µF capacitor if WAKEUP signal is on cable. Capacitor is to filter out possible transient introduce by the cable.
3. R1 can be as low as 50 Ω, if the WAKEUP signal is less than 4 V
4. R1 can be high as 50 kΩ, if the WAKEUP is higher than 4-V signal. Wakeup is internally connected to V5VAO and it can be as low as 4V in shutdown mode.

12 Single-Ended Communication

Communication with the bq76PL455A-Q1 from a host controller is performed utilizing UART communication protocol. The UART interface requires the following configuration:

1. COMML– is connected by a 100-kΩ pulldown to DGND
2. COMML+ is connected by a 100-kΩ pullup to V5VAO
3. FAULT_N has a 50-kΩ pulldown to make sure faults are generated when VIO is not present. The pulldown on the FAULT_N notifies the host controller in the case of an inadvertent shutdown.
4. TX and RX are pulled-up to VIO through a 100-kΩ resistor. Do not leave TX and RX unconnected. The TX must be pulled high to prevent triggering an invalid communications frame during the idle state when TX is high. When using a serial cable to connect to the host controller, connect the TX pullup on the host side and the RX pullup on the bq76PL455A-Q1 side.

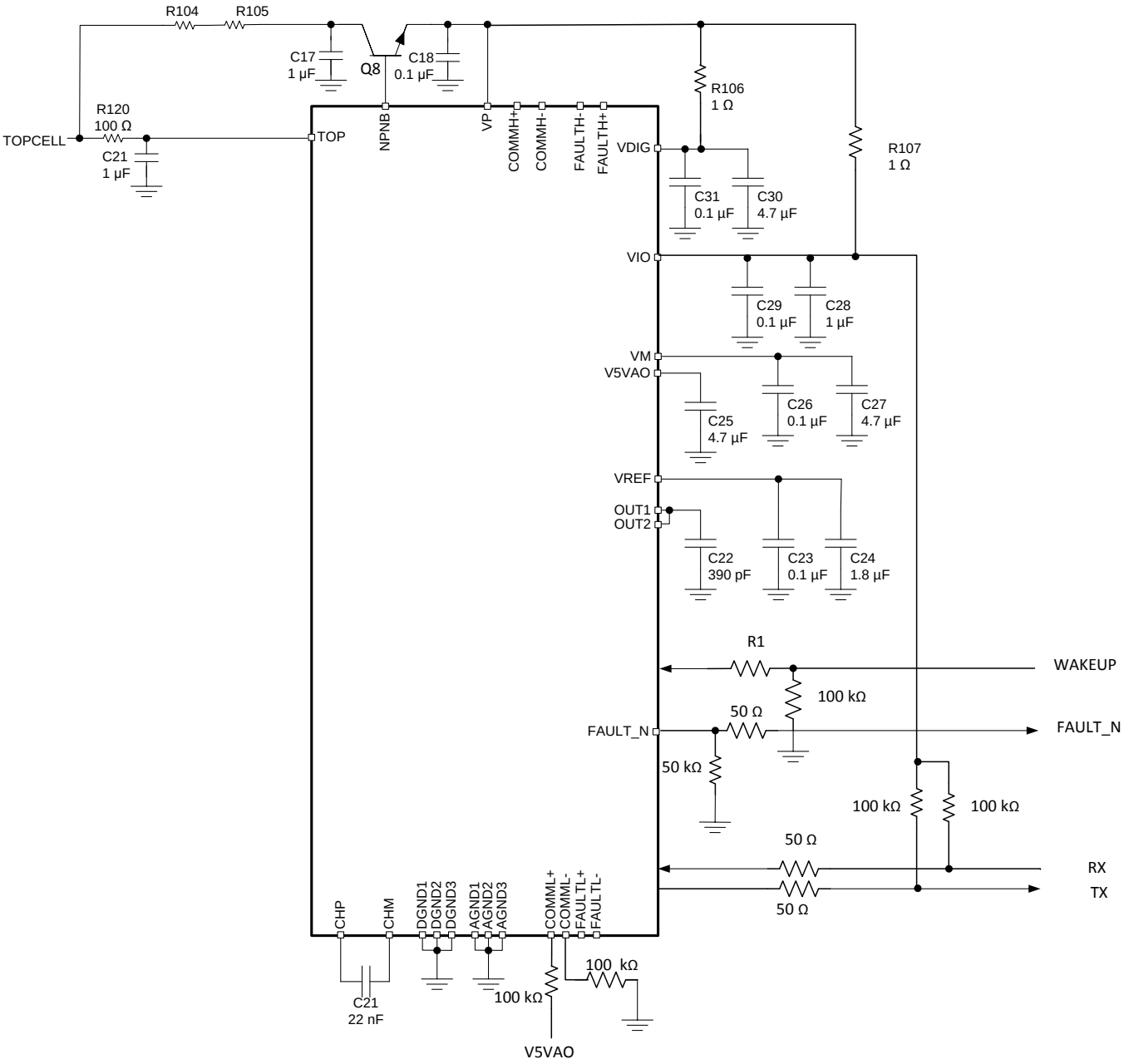


Figure 12. Single-Ended Circuit

Table 1. Single-Ended Communication Check List

List	Pin	Single-Ended (Figure 12)
1	RX	100-kΩ pullup to VIO
2	TX	100-kΩ pullup to VIO
3	COMML+	100-kΩ pullup to V5VAO
4	COMML–	100-kΩ pulldown to GND
5	COMMH+	Float
6	COMMH–	Float
7	FAULTH+	Float
8	FAULTH–	Float
9	FAULTL+	Float
10	FAULTL–	Float
11	FAULT_N	50 kΩ, pull down to GND and 50Ω series to host
12	WAKEUP	R1 should be 50 kΩ, if the WAKEUP signal is greater than 4 V (see Figure 11)

13 Stack Daisy-Chain Communication

In the stacked configuration, the main microcontroller first communicates through a bq76PL455A-Q1 device using the UART communications interface, see Figure 13. Communication is then relayed up the chain of connected slave bq76PL455A-Q1 devices using a proprietary differential communications protocol over AC-coupled differential links interconnected by the COMMH± and COMML± pins

Each device in the daisy chain buffers the signal drive levels. The signal is not re-clocked or filtered; it passes through the device without change and the entire stack sees all data sequencing regardless of the target device. The packet is not validated before being transmitted to the next device in the daisy chain. The uniquely-addressed or group-addressed device acts on the command (that is, begins an ADC conversion of the inputs) as soon as it receives and validates the packet for the correct address, message contents, and CRC.

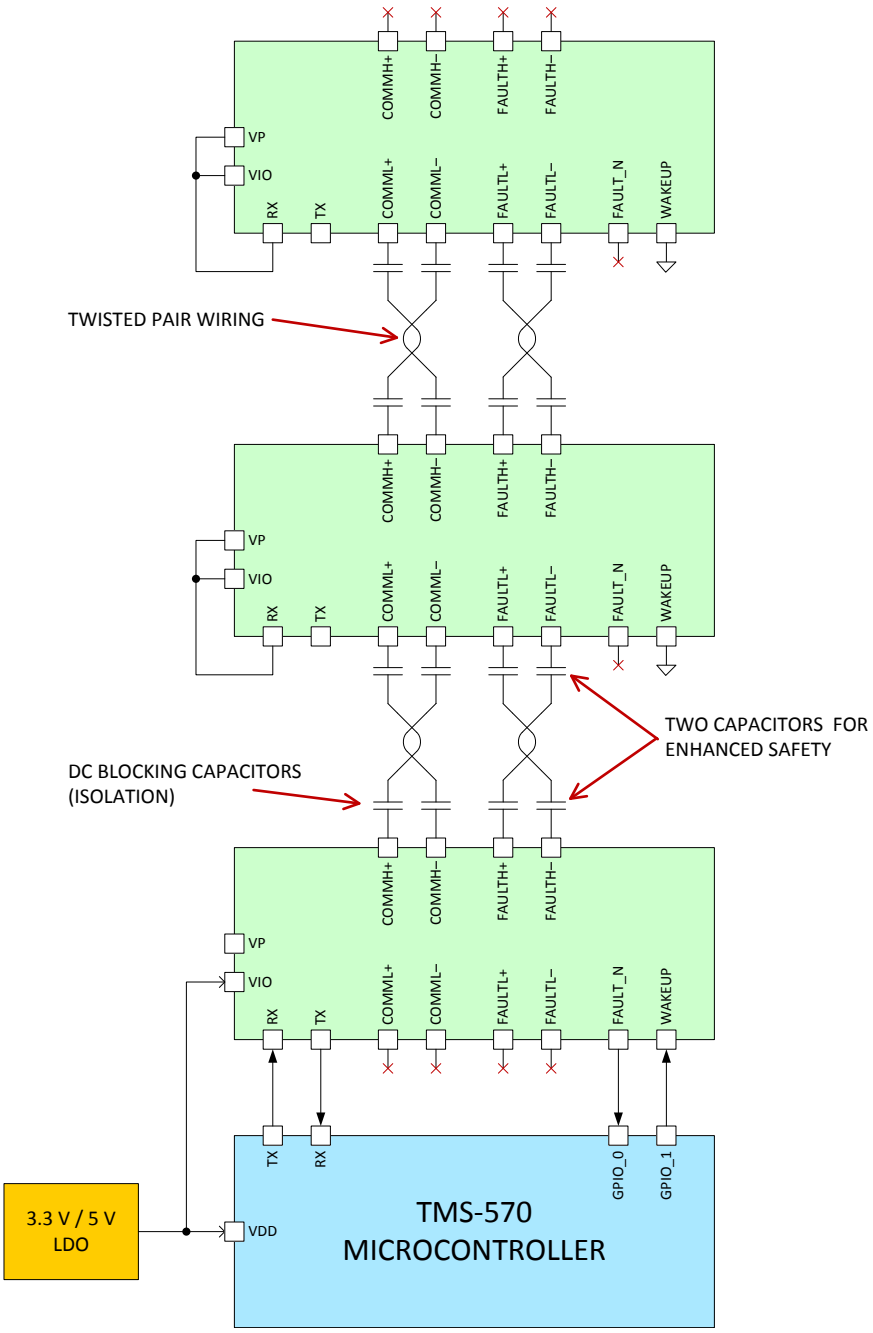


Figure 13. Simplified Stack Communication

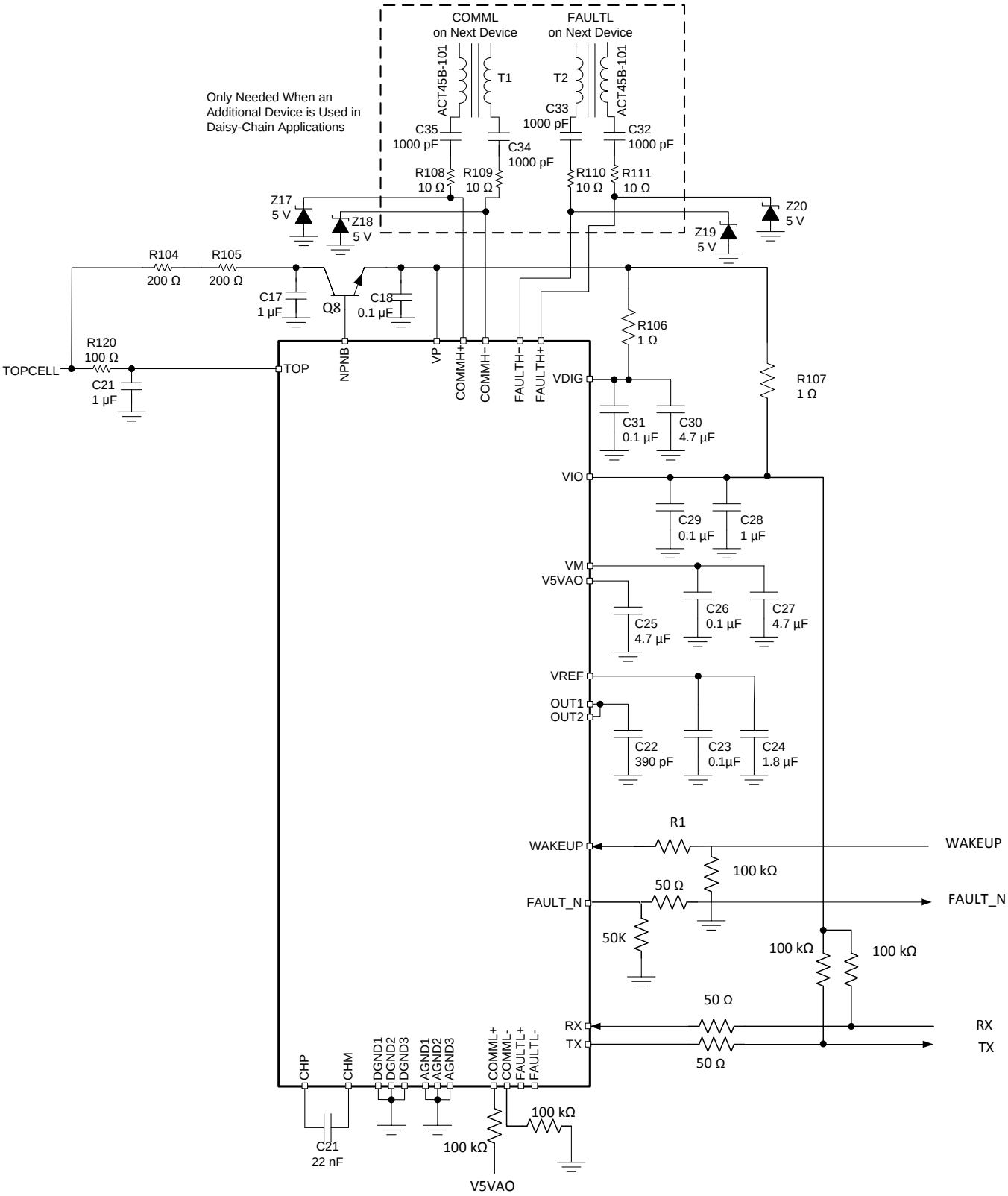


Figure 14. Stack Main (Master) Device

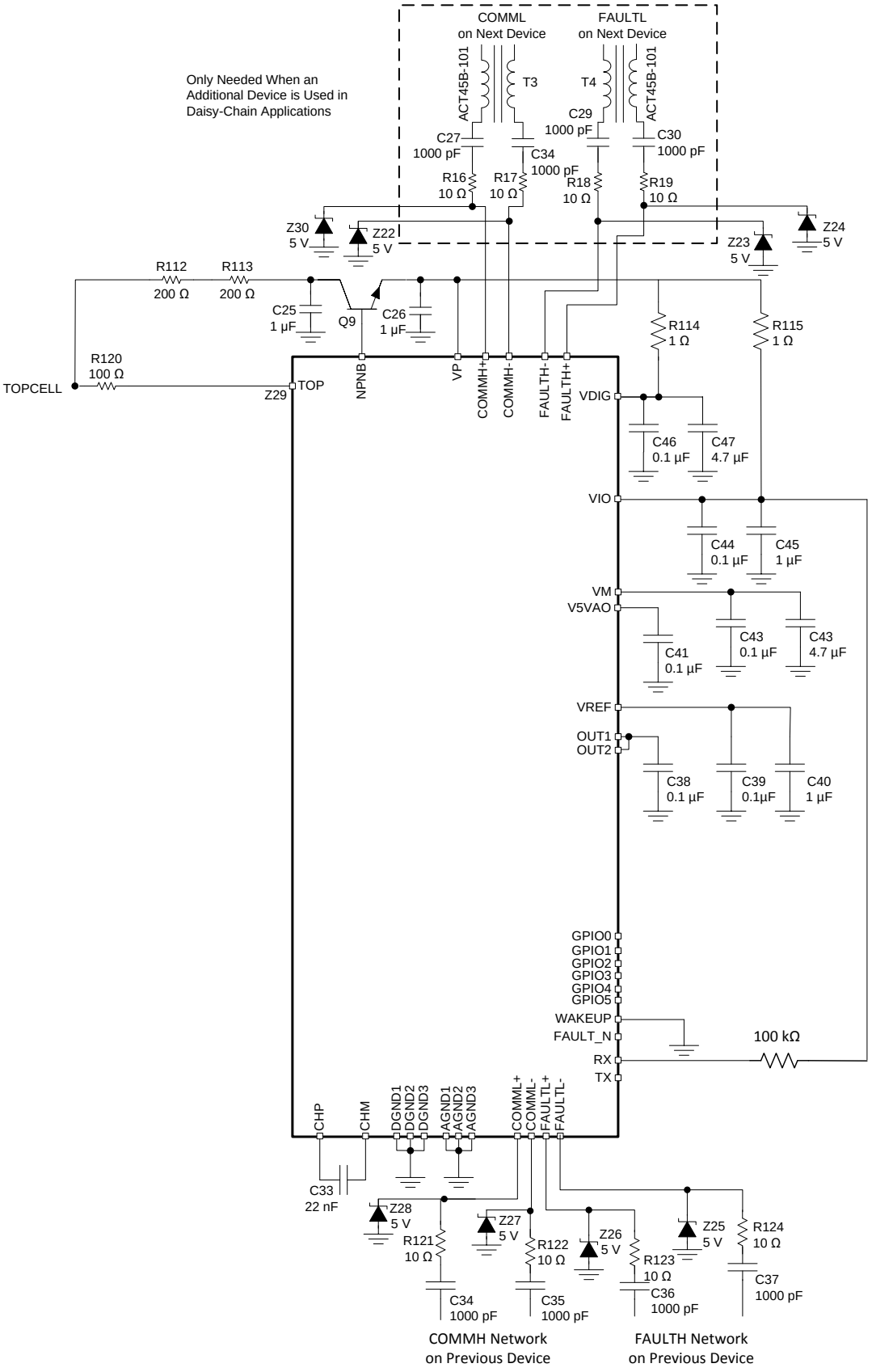


Figure 15. Stack Slave (Middle) Device

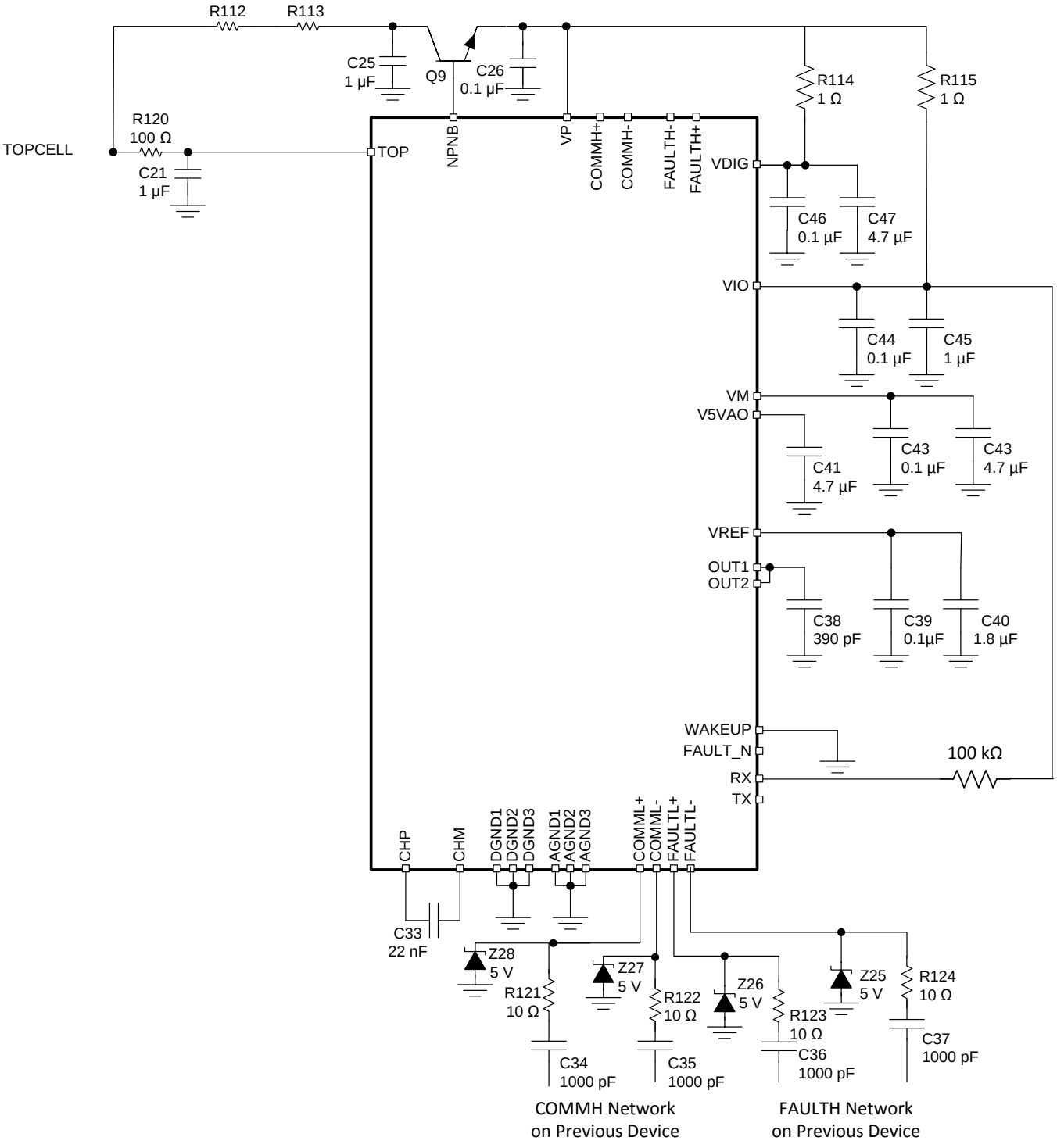
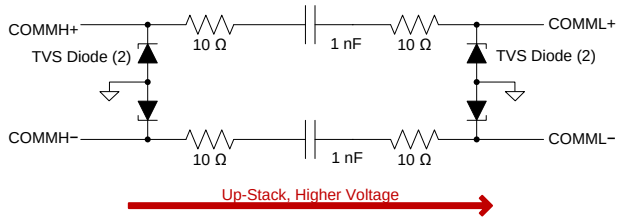
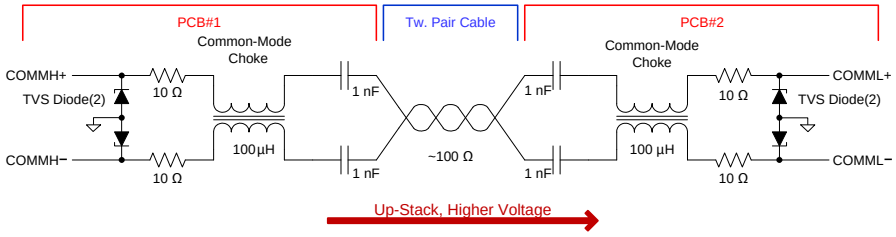


Figure 16. Stack Slave (TOP) Device

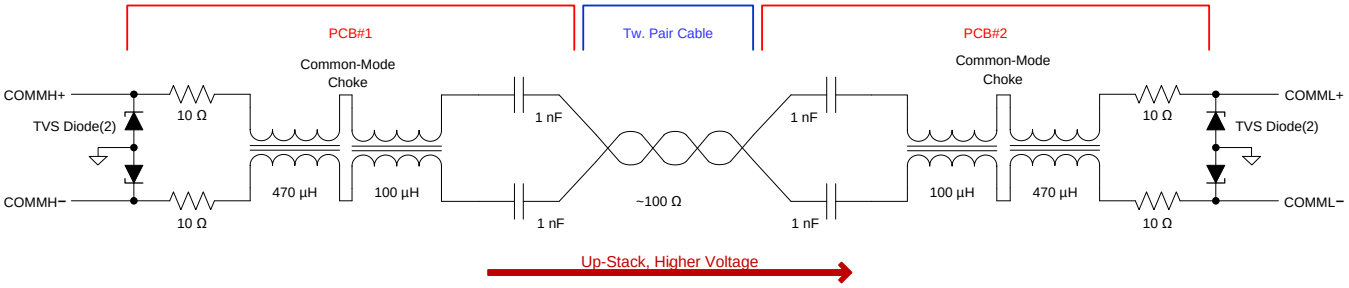
Many applications requires multiple, daisy-chained bq76PL455A-Q1 devices that are separated by cables or located on the same PCB. The cables can introduce additional challenges and additional components are needed for noisy environments. See Figure 17 for different ways of designing differential communication VBUS daisy chains.



Communication Between Devices on Same PCB



Communication Between Two PCBs



Communication Between Two PCBs in Noisy Environments

Figure 17. Communication Between Devices in Different Environments

Design Checklist:

1. Follow Table 2 for all communication pins.
2. TVS diodes are required for communicating between PCB. Use a TVS diode with the lowest capacitance as shown in Figure 17.

Table 2. Stack and Single-Ended Communication Check List

List	Pin	Stack Main (Master) Device (Figure 14)	Stack Slave (Middle) Device (Figure 15)	Stack Slave (TOP) Device (Figure 16)	Single-Ended (Figure 12)
1	RX	100-kΩ pullup to VIO	100-kΩ pullup to VIO	100-kΩ pullup to VIO	100-kΩ pullup to VIO
2	TX	100-kΩ pullup to VIO	Float	Float	100-kΩ pullup to VIO
3	COMML+	100-kΩ pullup to V5VAO	COMMH+ of lower (main) device	COMMH+ of lower (middle) device	100-kΩ pullup to V5VAO
4	COMML–	100-kΩ pulldown to GND	COMMH– of lower (main) device	COMMH– of lower (middle) device	100 kΩ pulldown to GND
5	COMMH+	COMML+ of upper (middle) device	COMML+ of upper (TOP) device	Float	Float
6	COMMH–	COMML- of upper (middle) device	COMML– of upper (TOP) device	Float	Float
7	FAULTH+	FAULTL+ of upper (middle) device	FAULTL+ of upper (TOP) device	Float	Float
8	FAULTH–	FAULTL - of upper (middle) device	FAULTL- of upper (TOP) device	Float	Float

Table 2. Stack and Single-Ended Communication Check List (continued)

List	Pin	Stack Main (Master) Device (Figure 14)	Stack Slave (Middle) Device (Figure 15)	Stack Slave (TOP) Device (Figure 16)	Single-Ended (Figure 12)
9	FAULTL+	Float	FAULTH+ of lower (main) device	FAULTH + of lower (middle) device	Float
10	FAULTL-	Float	FAULTH- of lower (main) device	FAULTH– of lower (middle) device	Float
11	FAULT_N	100 kΩ pulldown to GND	Float	Float	100 kΩ pulldown to GND
12	WAKEUP	See Figure 11.			

14 Common and Differential Mode Noises

X-Y caps are commonly used and may be required for extremely noisy environments

- Differential mode noise goes out one wire and returns back on another wire. An X capacitor is placed between two lines to suppress the noise.
- Common mode noise goes out from both wires and returns back to the chaises through stray capacitance to ground. A Y capacitor is placed between the Chassis as Figure 18 illustrates.

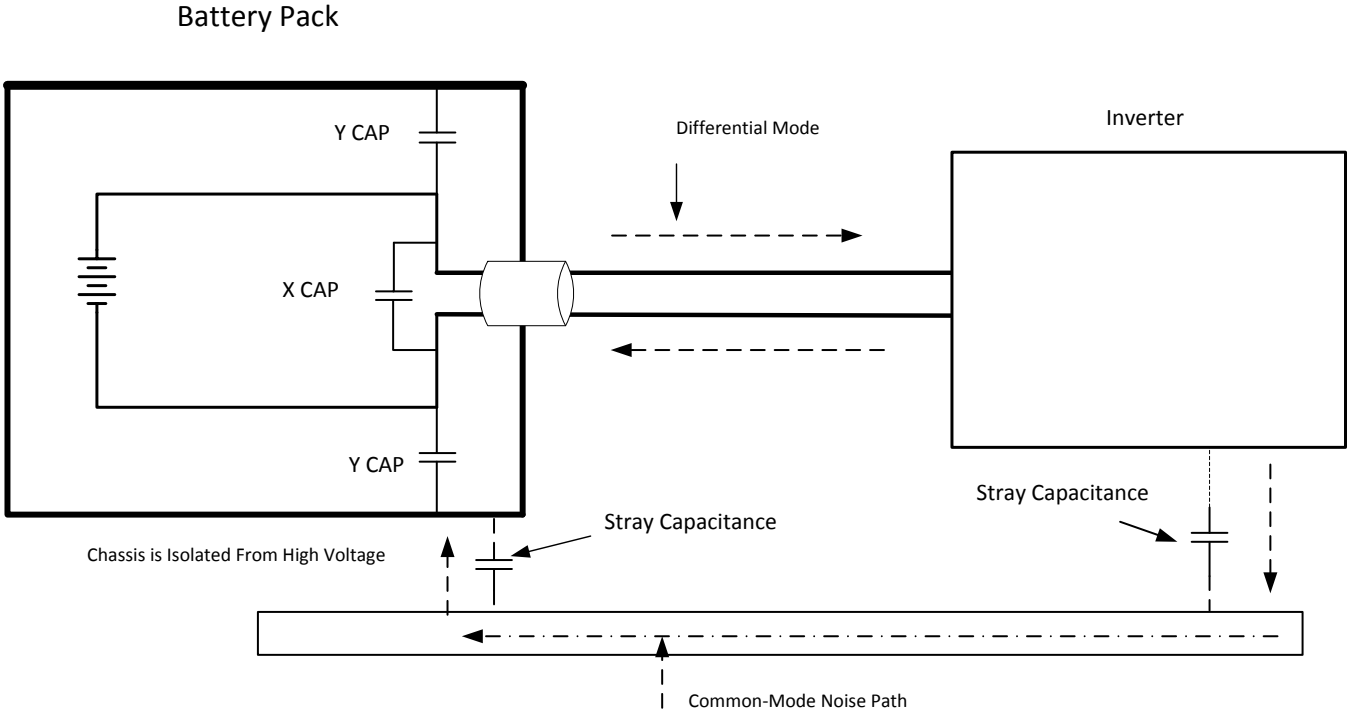


Figure 18. XY Caps

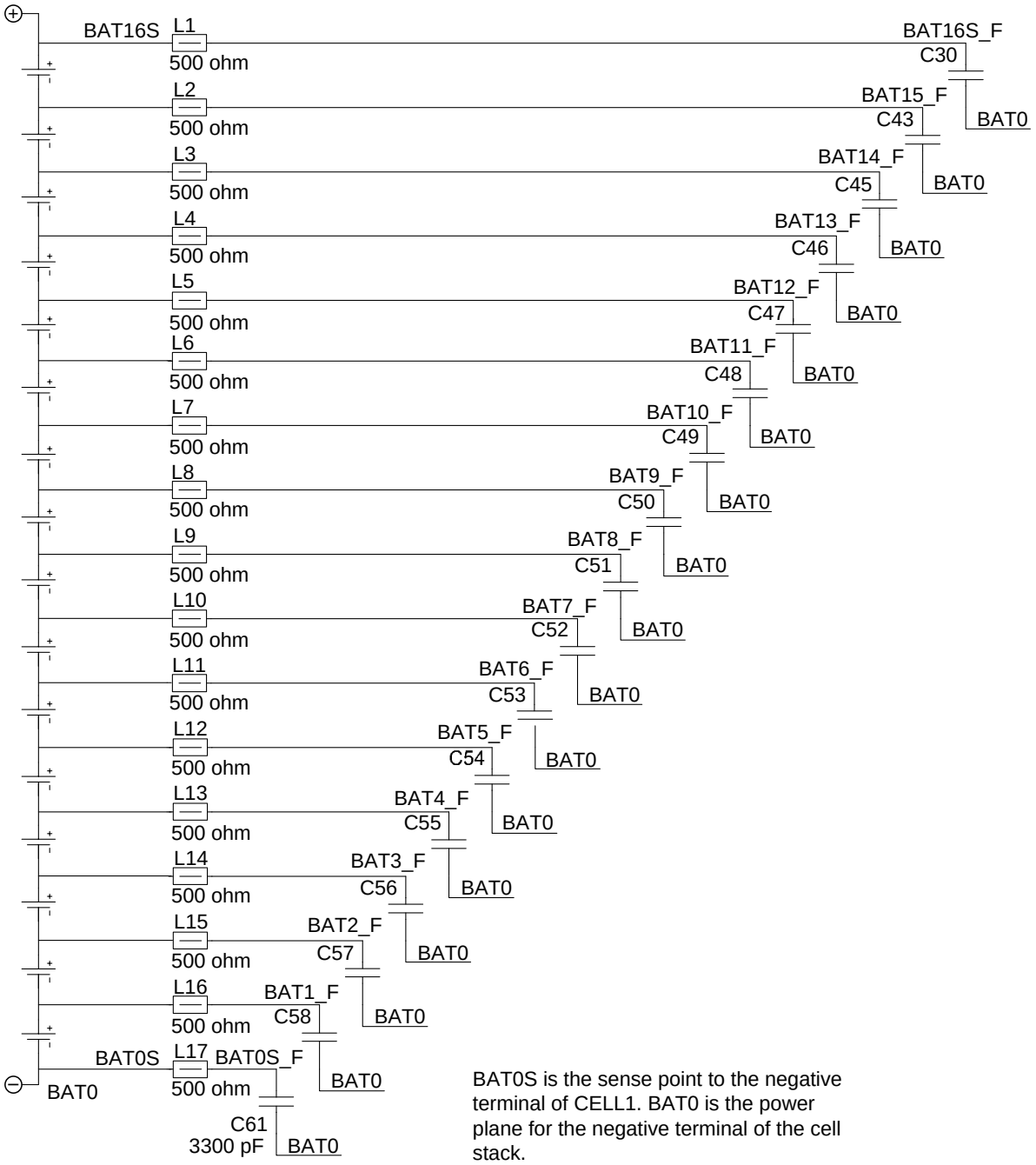
Design Considerations

- Device placements are important. Daisy-chain cable should not be resting on bus-bar or mental enclosure surface.

15 EMC Susceptibility on Cell Inputs

Additional components are necessary to improve EMC performance of the bq76PL455A-Q1 in automotive applications with electrically noisy environments.

- Use ferrite beads or small inductors in series with the cell inputs between the cell output and the series resistor to the VSENSE input. The bead and small capacitor must be located near each other.
- Add a 0.0033-µF capacitor from each cell input to the battery pack (BAT0 in Figure 19). Adjust the value of capacitance to satisfy the PCB layout and field conditions for the application.



BAT0S is the sense point to the negative terminal of CELL1. BAT0 is the power plane for the negative terminal of the cell stack.

Figure 19. EMC Filter

16 Layout Consideration

Since the bq76PL455A-Q1 measures small changes in voltage, care must be taken in the layout of signals to and from the device to avoid coupling noise onto sensitive inputs. The layout of ground and power connections, as well as communication signals should also be made carefully.

16.1 Layout Examples

To ensure the best possible accuracy performance, TI recommends following some basic layout guidelines for the bq76PL455A-Q1 to provide the best EMI and BCI performance. The isolation caps must be placed close to the edge of the board. The *Common Mode Chokes* must be close to the daisy-chain cable connector to provide a high-impedance path to common-mode noise as it enters the board. Place the series resistors and TVS diodes next to the bq76PL455A-Q1.

For detailed layout guidelines, see the bq76PL455A-Q1 datasheet (SLUSCB8).

An unbroken ground plane layer as part of a four or more layer board is recommended, with all AGND, DGND, and CGND connections made directly to the plane. The common GND planes are star connected directly to BAT0. There should also be a keep-out area on the plane area adjacent to the isolation capacitors, if daisy-chain communication is implemented. The following is a list of grounds:

- AGND1 – power section (noisy GND)
- AGND2 – GND for front-end output
- AGND3 – GND for ADC input
- DGND1, DGND2, DGND3 – digital GND
- CGND – communications digital GND

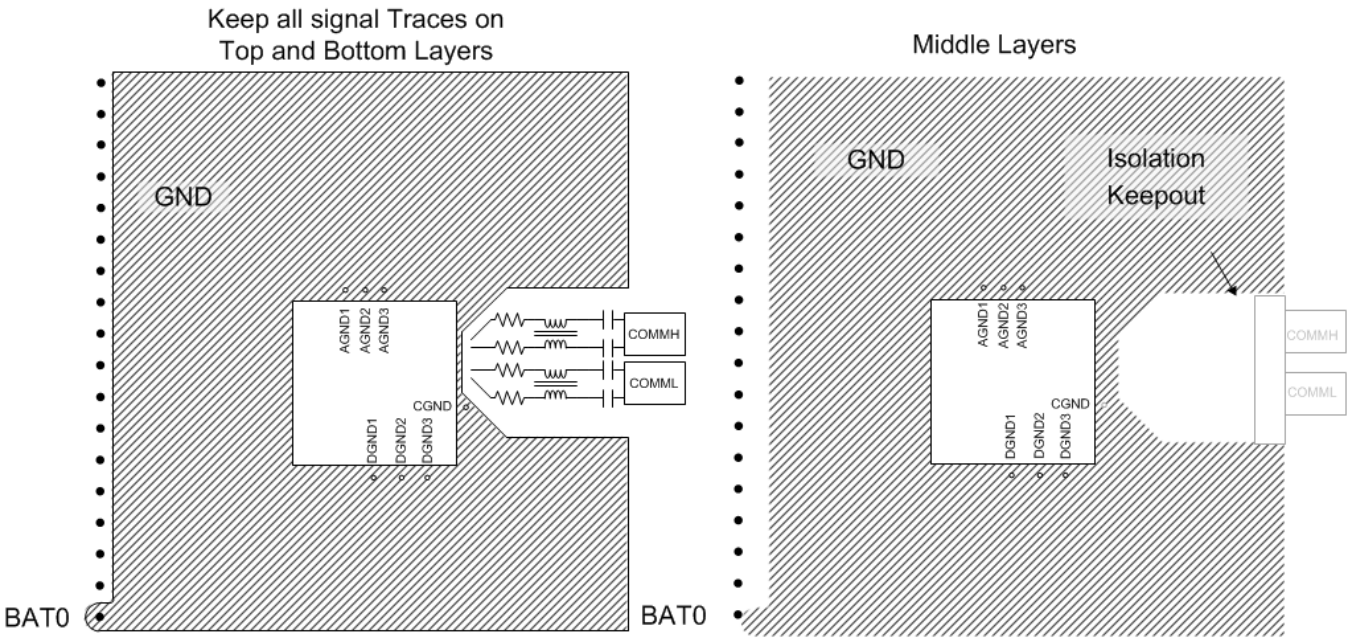


Figure 20. Simplified Layout Guideline

17 FAQ

17.1 Hot-Plug

The bq76PL455A-Q1 is designed for robust hot-plug performance. Component placement is critical for robust hot plugs.

1. Add a Zener diode between all VSENSE pins, as close as possible to input pins (see Figure 2).
2. Connect VSENSE16 input and any unused VSENSE pins to TOP using back-to-back diodes (see Figure 2).
3. Add a TVS diode on VSENSE16 to local ground to clamp the voltage to below 88 V and prevent an overvoltage and other transient events (see Figure 2).
4. Connect two back-to-back diodes between VSENSE0 and AGND as Figure 6 shows.
5. LPF should be 100 Ω to 1 kΩ and 0.1 µF to 1 µF. Higher resistance is better at limiting inrush current but the resistor value is directly proportional to error due to input bias (see Figure 7).
6. The total resistance of each COMML±, COMMH±, or FAULT_N± lines must be less than 20 Ω (10 Ω on each end of the signal connection between bq76PL455A-Q1 devices). This series resistance is required to limit in-rush current in a hot-plug event.
7. TI recommends connecting cell inputs first and then connecting daisy-chain cables.
8. TI recommends connecting VSENSE 16 to VSENSE 0, if possible.

17.2 Recommended Sample Periods and Setup for Best ADC Measurements

1. Apply 390 pF on OUT12 filter cap (see Figure 8)
2. Set AFE_PCTRL = 1. ADC power up will be 100 µs.
3. Set ADC_PERIOD_VOL = 60 µs. ADC sample period to 60 µs.
4. Set CMD_OVS_GPER = 12.6 µs. ADC sample period for oversamples.
5. Select CMD_OVS_CYCLE. Staying on a cell channel to oversample.
6. Set ADC_PERIOD_AUX = 12.6 µs. AUX ADC sample period
7. Set CMD_OVSMP for 8× oversampling for cells and Aux.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2016) to A Revision	Page
• Changed the description of FAULT_N From: "Float" To: "50 kΩ, pull down to GND and 50Ω series to host" in Table 1 .	13
• Changed the Stack Main description of COMML+ From: "Float" To: "100-kΩ pullup to V5VAO" in Table 2	18
• Changed the Stack Main description of COMML– From: "Float" To: "100-kΩ pulldown to GND" in Table 2	18

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      CAUTION

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
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Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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