TEXAS INSTRUMENTS

Application Report

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How to Estimate Overshoot and Undershoot of Load Transients of a DC/DC Regulator

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ABSTRACT

In a DC-to-DC circuit design, output capacitance is a critical design parameter, which directly affects the output voltage ripple, loop stability, and the overshoot and undershoot during load transient. The intent of this application report is to show how to estimate the overshoot and undershoot of load transients of a design before PCB fabrication. A typical topology, peak current mode (PCM) control buck regulator circuit, is used as an example to explain the mechanism.

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1 PCM Buck Regulator Block Diagram

For most popular DC/DC regulators available, the switching frequency gets extremely high, may reach several MHz, which allows smaller output inductance and capacitance. In many cases, output capacitance is small, allowing the use of only ceramic capacitors. In this application report, ceramic capacitors with low ESR and ESL are employed for the analysis.

Figure 1 shows a simplified schematic of PCM buck regulator.

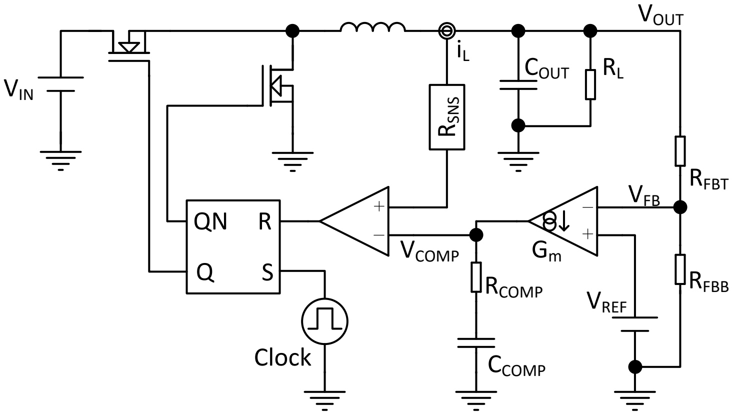

Figure 1. Simplified Schematic of PCM Buck Regulator

2 Load Transient Analysis in Both Frequency and Time Domain

2.1 PCM Buck Regulator Small Signal Model

Figure 2 shows a simplified small signal model of a PCM control buck regulator. This model adopts a voltage controlled current-sourcing concept. In this model, the inductor current is treated as well-controlled current source, which is a simple interpretation of current-loop effects. This model provides excellent physical insight to readers, and is accurate enough for a preliminary design loop analysis.

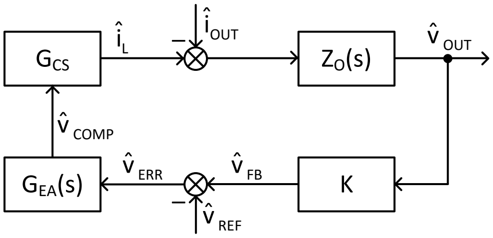

Figure 2. PCM Buck Regulator Small Signal Model

Equation 1 through Equation 4 show calculations for some of the elements in Figure 2.

$$K = \frac{\hat{v}_{FB}}{\hat{v}_{OUT}} = \frac{R_{FBB}}{R_{FBT} + R_{FBB}} = \frac{V_{REF}}{V_{OUT}}$$

where

- K is the feedback divider proportionality coefficient. (1)

$$G_{EA}(s) = \frac{\hat{v}_{COMP}}{\hat{v}_{ERR}} = G_m \times \left(R_{COMP} + \frac{1}{s \times C_{COMP}} \right)$$

where

- $G_{EA}(s)$ is the compensation circuit transfer function
- G_m is the gain of the transconductance amplifier
- R_{COMP} and C_{COMP} is the compensation RC (2)

$$G_{CS} = \frac{\hat{i}_L}{\hat{v}_{COMP}} = \frac{1}{R_{SNS}}$$

where

- G_{CS} is the transconductance of inductor current sense circuit, which is the reciprocal value of the current sense resistor R_{SNS} in Figure 1 (3)

$$Z_O(s) = \frac{\hat{v}_{OUT}}{\hat{i}_L} = \frac{1}{s \times C_{OUT}} \parallel R_L = \frac{R_L}{1 + s \times C_{OUT} \times R_L}$$

where

- $Z_O(s)$ is open-loop output impedance, because the inductor current is treated as voltage controlled current-sourcing, so the open-loop output impedance equals the output capacitance C_{OUT} parallel with the load resistance R_L (4)

The open-loop transfer function T(s) can be derived by multiplying every element in the loop (see Equation 5):

$$\begin{aligned} T(s) &= K \times G_{EA}(s) \times G_{CS} \times Z_O(s) \\ &= \frac{V_{REF}}{V_{OUT}} \times G_m \times \left(R_{COMP} + \frac{1}{C_{COMP}} \right) \times \frac{1}{R_{SNS}} \times \frac{R_L}{1 + s \times C_{OUT} \times R_L} \end{aligned} \tag{5}$$

Then the close-loop output impedance can be calculated by Equation 6.

$$Z_{OC}(s) = \frac{\hat{v}_{OUT}}{\hat{i}_{OUT}} = \frac{Z_O(s)}{1 + T(s)} \tag{6}$$

2.2 Overshoot and Undershoot Prediction

According to the definition, the output variation $v_{OUT}(s)$ equals the output impedance $Z_{OC}(s)$ multiplying the load variation $i_{OUT}(s)$. For a transient load step of ΔI_{OUT}, it can be transferred to $\Delta I_{OUT}/s$ according to the Laplace transform (see Equation 7).

$$\hat{v}_{OUT}(s) = \hat{i}_{OUT}(s) \times Z_{OC}(s) = \frac{\Delta I_{OUT}}{s} \times \frac{Z_O(s)}{1 + T(s)} \tag{7}$$

The entire small signal analysis is based on frequency domain; however, the system-required overshoot and undershoot limitation specification is defined in time domain. To obtain the time domain behavior of $v_{OUT}(t)$, transfer $v_{OUT}(s)$ into time domain with inverse Laplace transform. With the help of the mathematic tool Mathcad®, finally a simplified time domain equation is derived by doing inverse Laplace transform of Equation 7 (see Equation 8):

$$\hat{v}_{OUT}(t) = \mathrm{InvLaplace}\left(\hat{v}_{OUT}(s)\right) \approx \begin{cases} \dfrac{\Delta I_{OUT} \times e^{-A \times t} \times \sin\left(\sqrt{B - A^2} \times t\right)}{C_{OUT} \times \sqrt{B - A^2}} & \text{while } A^2 < B \\ \dfrac{\Delta I_{OUT} \times e^{-A \times t} \times \left(e^{\sqrt{A^2 - B} \times t} - e^{-\sqrt{A^2 - B} \times t}\right)}{2 \times C_{OUT} \times \sqrt{A^2 - B}} & \text{while } A^2 > B \end{cases}$$

where

- $A = \dfrac{G_m \times G_{CS} \times V_{REF} \times R_{COMP}}{2 \times C_{OUT} \times V_{OUT}}$
- $B = \dfrac{G_m \times G_{CS} \times V_{REF}}{C_{OUT} \times V_{OUT} \times C_{COMP}}$ (8)

To get the overshoot peak value or undershoot valley value, calculate the extremum point t_{EP} when the derivative of $v_{OUT}(t)$ equals 0 (see Equation 9).

$$\frac{d\hat{v}_{OUT}(t_{EP})}{dt} = \begin{cases} \dfrac{\Delta I_{OUT} \times e^{-A \times t_{EP}} \times \left[\sqrt{B - A^2} \times \cos\left(\sqrt{B - A^2} \times t_{EP}\right) - A \times \sin\left(\sqrt{B - A^2} \times t_{EP}\right)\right]}{C_{OUT} \times \sqrt{B - A^2}} = 0 & \text{while } A^2 < B \\ \dfrac{\Delta I_{OUT} \times \left[\left(\sqrt{A^2 - B} - A\right) \times e^{\left(\sqrt{A^2 - B} - A\right) \times t_{EP}} + \left(\sqrt{A^2 - B} + A\right) \times e^{\left(-\sqrt{A^2 - B} - A\right) \times t_{EP}}\right]}{2 \times C_{OUT} \times \sqrt{A^2 - B}} = 0 & \text{while } A^2 > B \end{cases} \quad (9)$$

According to Equation 10, t_{EP} can be calculated:

$$t_{EP} = \begin{cases} \dfrac{\arctan\left(\dfrac{\sqrt{B - A^2}}{A}\right)}{\sqrt{B - A^2}} & \text{while } A^2 < B \\ \dfrac{\ln\left(\dfrac{A + \sqrt{A^2 - B}}{A - \sqrt{A^2 - B}}\right)}{2 \times \sqrt{A^2 - B}} & \text{while } A^2 > B \end{cases} \quad (10)$$

Substitute t_{EP} back into Equation 8, calculate the overshoot peak value or undershoot valley value with Equation 11.

$$V_{OS/US} = V_{OUT} + \hat{v}_{OUT}(t_{EP}) \approx \begin{cases} V_{OUT} + \dfrac{\Delta I_{OUT} \times e^{-A \times t_{EP}} \times \sin\left(\sqrt{B - A^2} \times t_{EP}\right)}{C_{OUT} \times \sqrt{B - A^2}} & \text{while } A^2 < B \\ V_{OUT} + \dfrac{\Delta I_{OUT} \times e^{-A \times t_{EP}} \times \left(e^{\sqrt{A^2 - B} \times t_{EP}} - e^{-\sqrt{A^2 - B} \times t_{EP}}\right)}{2 \times C_{OUT} \times \sqrt{A^2 - B}} & \text{while } A^2 > B \end{cases} \quad (11)$$

$V_{OUT}(t)$ values at every moment can be calculated with Equation 11. So a time-continuous curve can be plotted with a mathematic tool like Mathcad or Excel.

3 Simulation Verification

Here we take TPS54335A as an example. We have made a design of a PCM buck regulator, working in the condition involved: V_{IN} = 12 V, V_{OUT} = 5 V, switching frequency 1 MHz, max load current 3 A. Load transient from 1 A to 3 A (ΔI_{OUT} = 1 A – 3 A = –2 A).

Table 1. Design Example Specifications

Design Parameter	Value
Input voltage, V_{IN}	9 V to 15 V, Typical 12 V
Output voltage, V_{OUT}	5.0 V
Maximum output current I_{OUT_MAX}	3 A
Undershoot or overshoot during load transient of 1 A to 3 A	3% of V_{OUT}
Switching frequency, f_{SW}	1 MHz
TPS54335A reference voltage, V_{REF}	0.8 V
TPS54335A error amplifier gain, G_m	1.3 A/V
TPS54335A power stage gain, G_{CS}	8 A/V

3.1 Output Filter Components Design

The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 12 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value of K_{IND} should be 30% to 50%. For this application, choose K_{IND} = 0.5 for smaller inductance.

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT\_MAX} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} = \frac{15-5}{3 \times 0.5} \times \frac{5}{15 \times 1} = 2.2\ \mu H \tag{12}$$

The desired response to a large load current change is usually the first criterion for output capacitance selection. When a large load step occurs, output capacitors provide the required charge before the inductor current can regulate to the appropriate level. The control loop of the regulator usually needs several clock cycles to regulate the inductor current equal to the new load level. The output capacitance must be large enough to supply or absorb the current difference to maintain the output voltage within the specified range. An engineering empirical formula, Equation 13, shows the minimum output capacitance needed for specified output overshoot or undershoot.

$$C_{OUT} > \frac{\Delta I_{OUT} \times \left(\frac{1}{4 \times f_C} + \frac{1}{f_{SW}} \right)}{2 \times \Delta V_{OUT}} = \frac{2 \times \left(\frac{1}{4 \times 0.05} + \frac{1}{1} \right)}{2 \times 5 \times 3\%} = 40\ uF$$

where

- f_C = crossover frequency (13)

A good starting value for f_C is 1/20 to 1/10 of the switching frequency, f_{SW}.

For this application, choose f_C to be 1/20 × 1 MHz = 0.05 MHz. To leave some margin, choose 47 µF as the C_{OUT}.

3.2 Compensation Circuit Design

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, f_C. In this application, choose f_C = 0.05 MHz.
2. Use Equation 14 to calculate the value of R_{COMP}. A standard 8.87-kΩ resistor is selected as R_{COMP}.

$$R_{COMP} = \frac{2\pi \times f_C \times C_{OUT} \times V_{OUT}}{V_{REF} \times G_m \times G_{CS}} = \frac{2\pi \times 0.05 \times 47 \times 5}{0.8 \times 1.3 \times 8} = 8.9\ k\Omega \tag{14}$$

3. Design the R_{COMP} and C_{COMP} zero at 1/4 of the f_C. C_{COMP} can be calculated by Equation 15.

$$C_{COMP} = \frac{2}{\pi \times f_C \times R_{COMP}} = \frac{2}{\pi \times 0.051 \times 8.87} = 1.4\ \text{nF} \tag{15}$$

A standard 1.5-nF capacitor is selected as C_{COMP}.

3.3 Comparison of Simulation and Calculation Result

After completing the previous design procedure, all the design parameters are obtained in Table 2.

Table 2. Design Parameters

L	C_{OUT}	R_L	V_{REF}	G_m	R_{COMP}	C_{COMP}	G_{CS}
2.2 µH	47 µF	5 Ω	0.8 V	1.3 mA/V	8.87 kΩ	1.5 nF	8 A/V

With all the known parameters in Table 2, A and B can be calculated by and .

$$A = \frac{G_m \times G_{CS} \times V_{REF} \times R_{COMP}}{2 \times C_{OUT} \times V_{OUT}} = 1.57 \times 10^5 \tag{16}$$

$$B = \frac{G_m \times G_{CS} \times V_{REF}}{C_{OUT} \times V_{OUT} \times C_{COMP}} = 2.36 \times 10^{10} \tag{17}$$

Because $A^2 > B$, the critical point t_{EP} can be calculated by the second formula in Equation 10.

$$t_{EP} = \frac{\ln\left(\dfrac{A + \sqrt{A^2 - B}}{A - \sqrt{A^2 - B}}\right)}{2 \times \sqrt{A^2 - B}} = 6.46 \times 10^{-6} \tag{18}$$

Finally, the undershoot can be calculated by Equation 11.

$$V_{OS/US} = V_{OUT} + \hat{v}_{OUT}(t_{EP}) \approx V_{OUT} + \frac{\Delta I_{OUT} \times e^{-A \times t_{EP}} \times \left(e^{\sqrt{A^2 - B} \times t_{EP}} - e^{-\sqrt{A^2 - B} \times t_{EP}}\right)}{2 \times C_{OUT} \times \sqrt{A^2 - B}} = 4.9\ \text{V} \tag{19}$$

To verify the calculation result, we built a simulation model of PCM buck regulator according to Figure 1 in Simplis™. Figure 3 shows the Simplis simulation circuit diagram. A load transient from 1 A to 3 A occurs at 0.1 ms (Figure 4 shows the simulation result). The undershoot valley value 4.9 V occurs at 6.5 µs after the load transient happens, which is almost the same as the calculated values in Equation 18 and Equation 19. In Figure 4, an additional time-continuous curve is plotted using Mathcad with Equation 11. The calculated curve matches well with the simulated curve during the entire period.

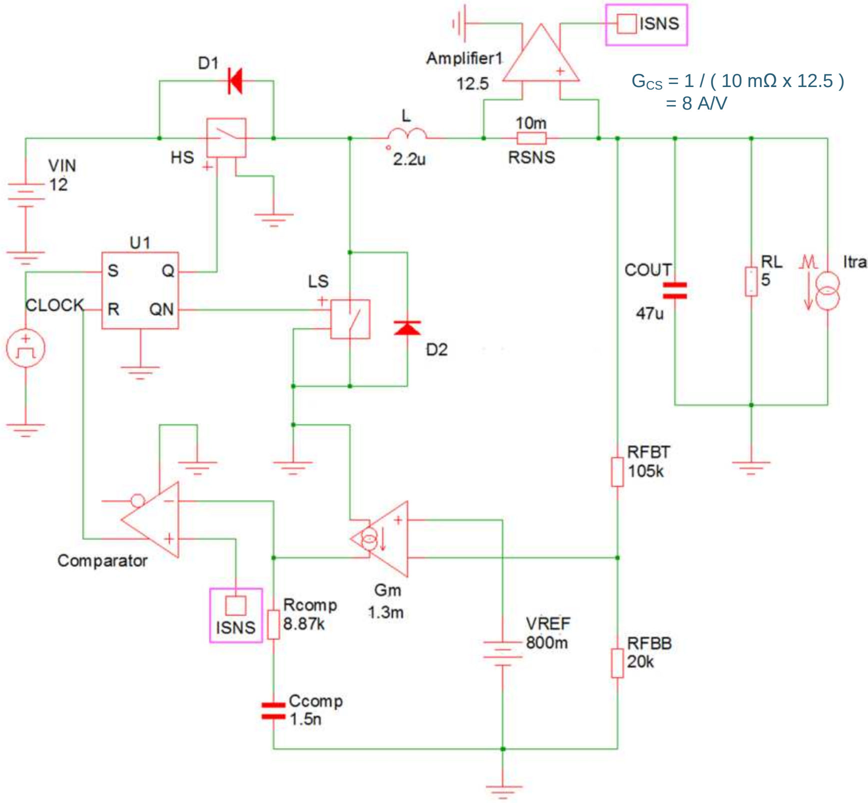

Figure 3. Simplis™ Simulation Circuit

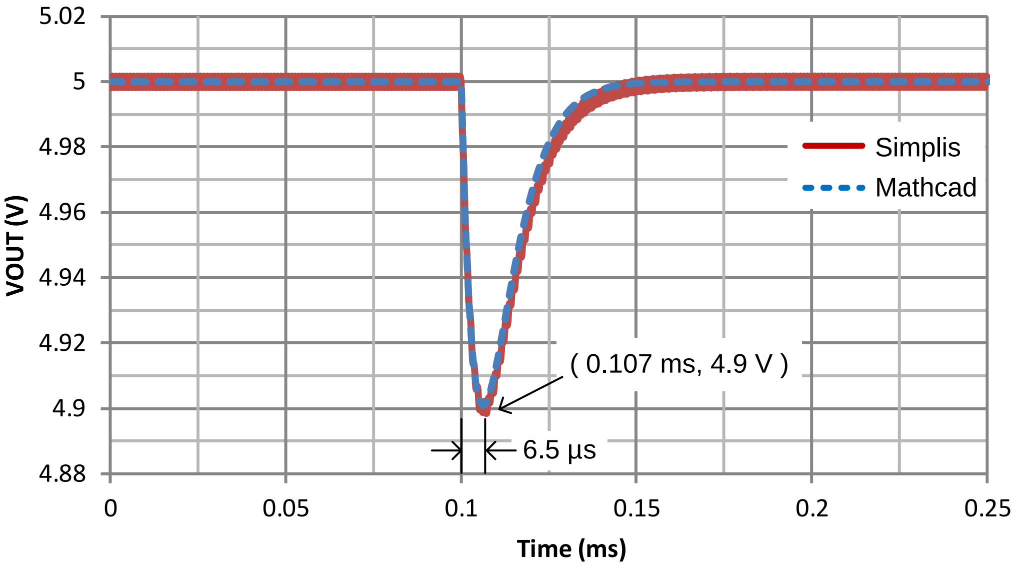

Figure 4. Comparison of Simulation and Calculation Result

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