Application Note

Stacking Implementations with BQ77915

ABSTRACT

The BQ77915 3-5S low-power protector with simple stacking capabilities supports cell counts up to 20S or higher. The data sheet shows signal descriptions and simplified connection diagrams for stacking. This document provides schematics and test data for the user implementing a stacking BQ77915 protector design.

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1 Configuration

The following stacking configuration represents a battery pack protection system for up to 10-S cell pack. Figure 1-1 shows the configuration of the two devices. For configurations with less than 10-S cell pack, only use the two devices. For configurations with 11-S to 15-S cell packs, use three devices. For configurations with 16-S to 20-S cell packs, use four devices.

Note

For configurations where one or more of the devices supports a lower cell count (for example, three or four) than the rest of the stacked devices, TI recommends using the uppermost device on the stack to support the highest cell count. For example, if the user wants to protect a 9-S cell pack, the top device would support five cells and the bottom device would support four cells. If the user wanted to protect a 17-S cell pack, the top device supports five cells and the lower devices each support four cells. When possible, configure each device to support the same number of cells.

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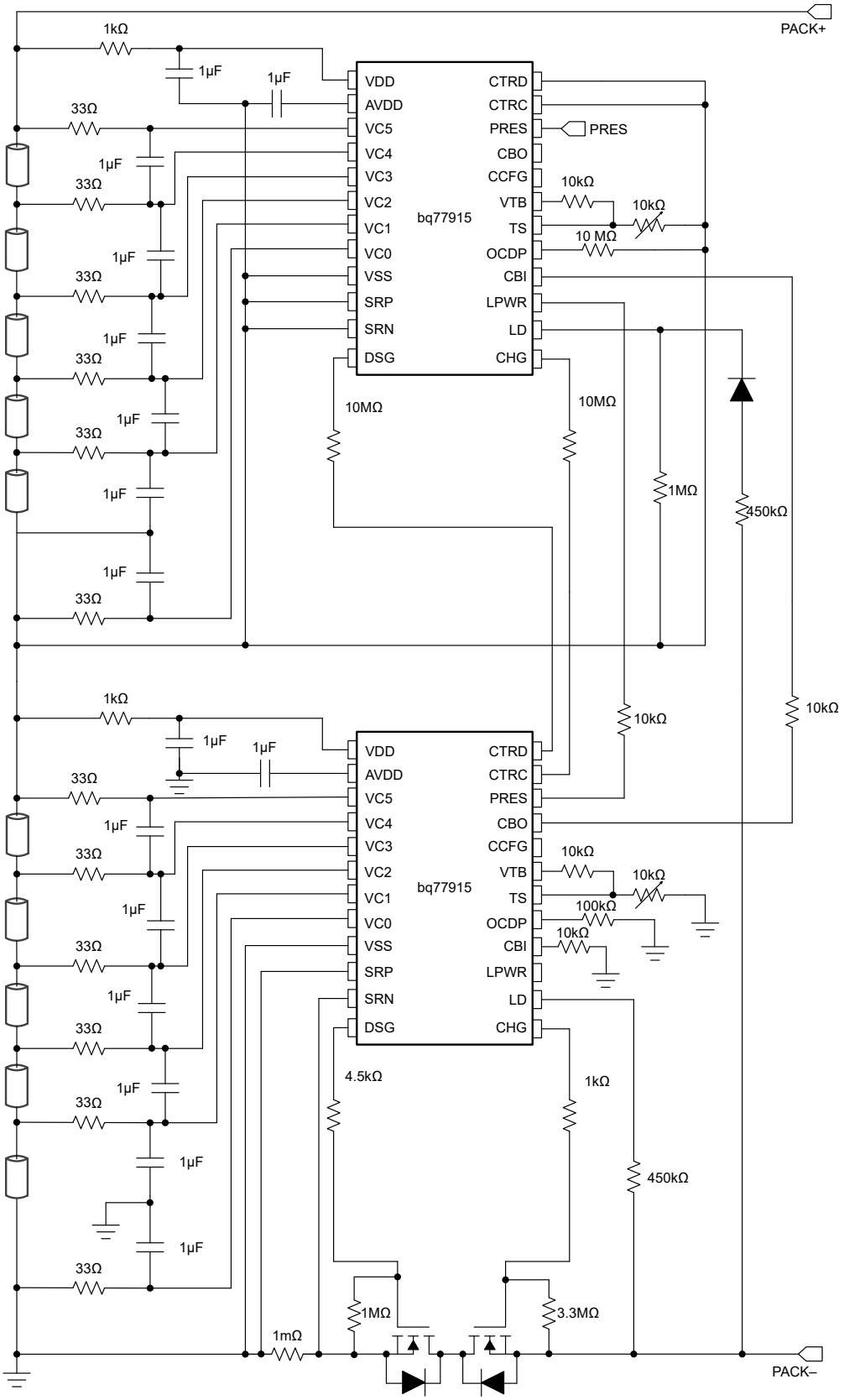

Figure 1-1. Stacking Diagram with HIBERNATE Mode Enabled

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1.1 General Setup Instructions

The following instructions are useful when constructing any stacking configuration with the BQ77915. Many steps refer to the pin connections that can best be understood by observing the schematic. Further information on the setup of the Stacking Implementations is found in the *bq77915 3-5S Low Power Protector with Cell Balancing and Hibernate Mode* data sheet.

- Ensure each device has a connection on at least the three lowest cell inputs.
- Ensure that the CCFG pin of each device is configured appropriately for the specific number of cells, either three, four, or five.
- Connect the CHG pin of the upper device with a R_{CTRC} to the CTRC pin of the immediate lower device.
- Connect the DSG pin of the upper device with a R_{CTRD} to the CTRD pin of the immediate lower device.
- All upper devices must have the SRP and SRN pins shorted to the VSS pin.
- Connect the upper CBI pins with R_{CB} to the CBO pin of the immediate lower device.
- Connect upper LPWR pins with an $R_{HIB}$to the PRES pin of the immediate lower device.
- Connect the upper OCDP pins with a 10-MΩ resistor to VSS. Use the lower OCDP pin to program the OCD1/2 delay.

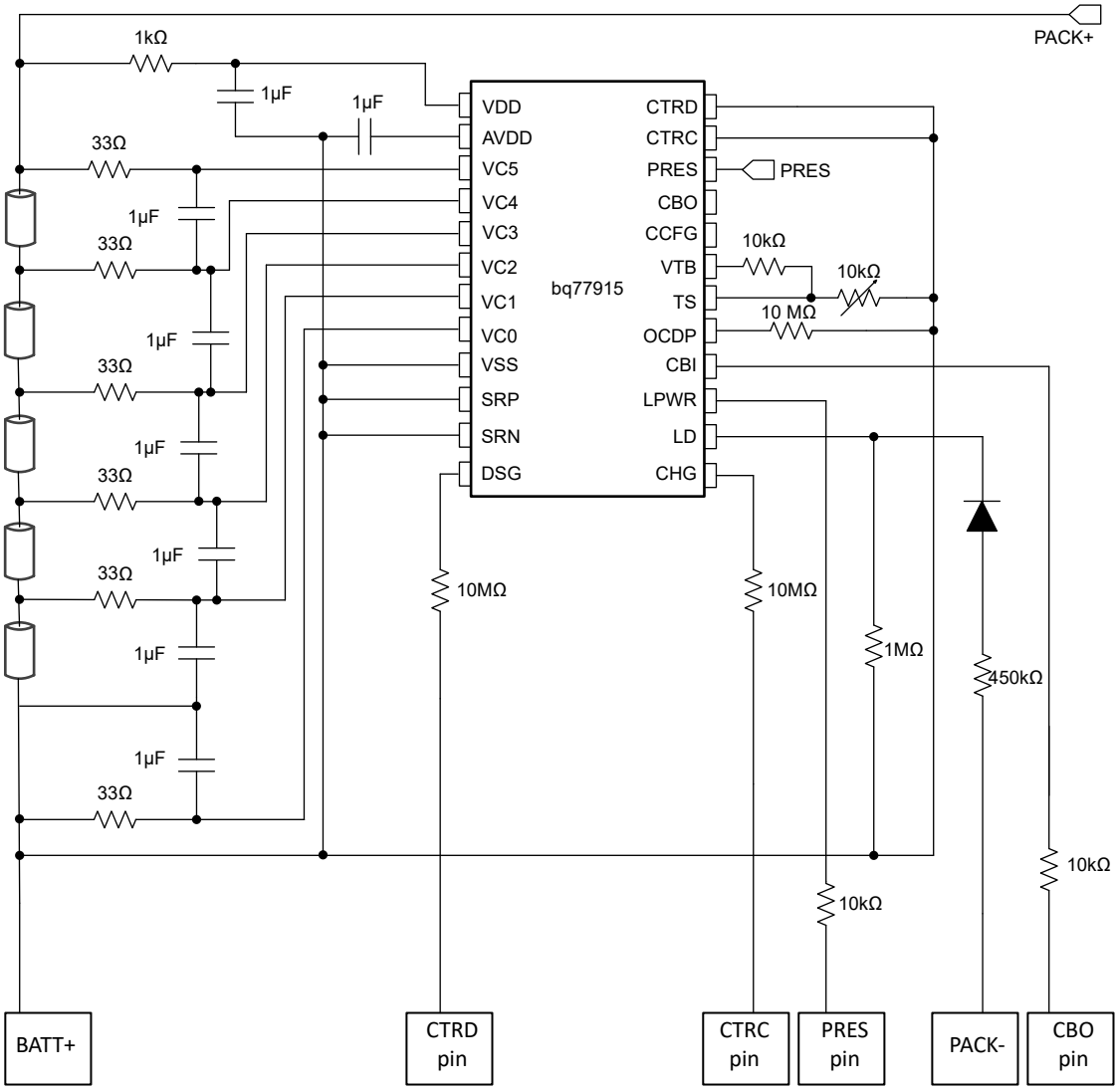

Figure 1-2. Top Device with HIBERNATE Mode Enabled

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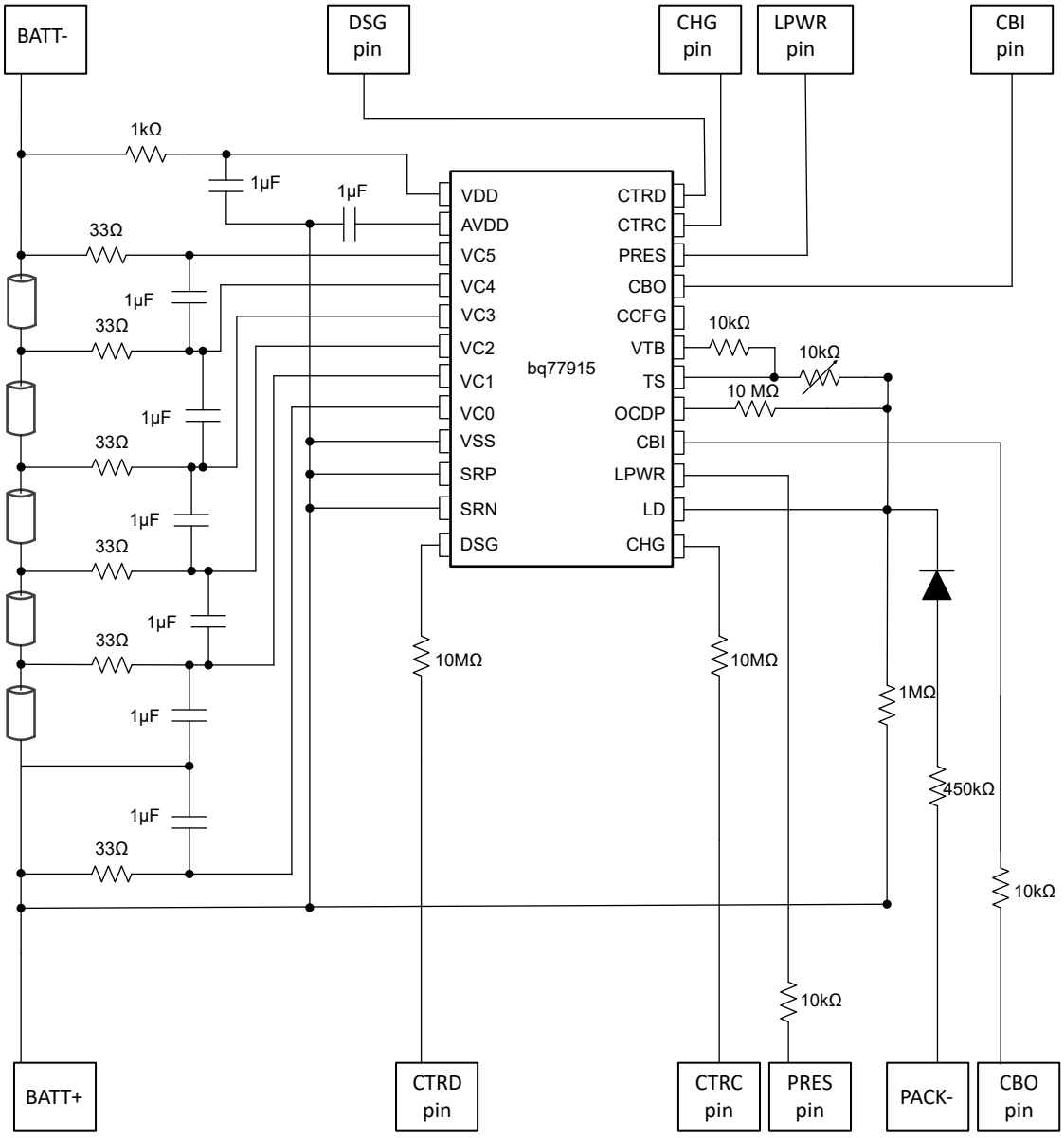

Figure 1-3. Middle Device(s) with HIBERNATE Mode Enabled

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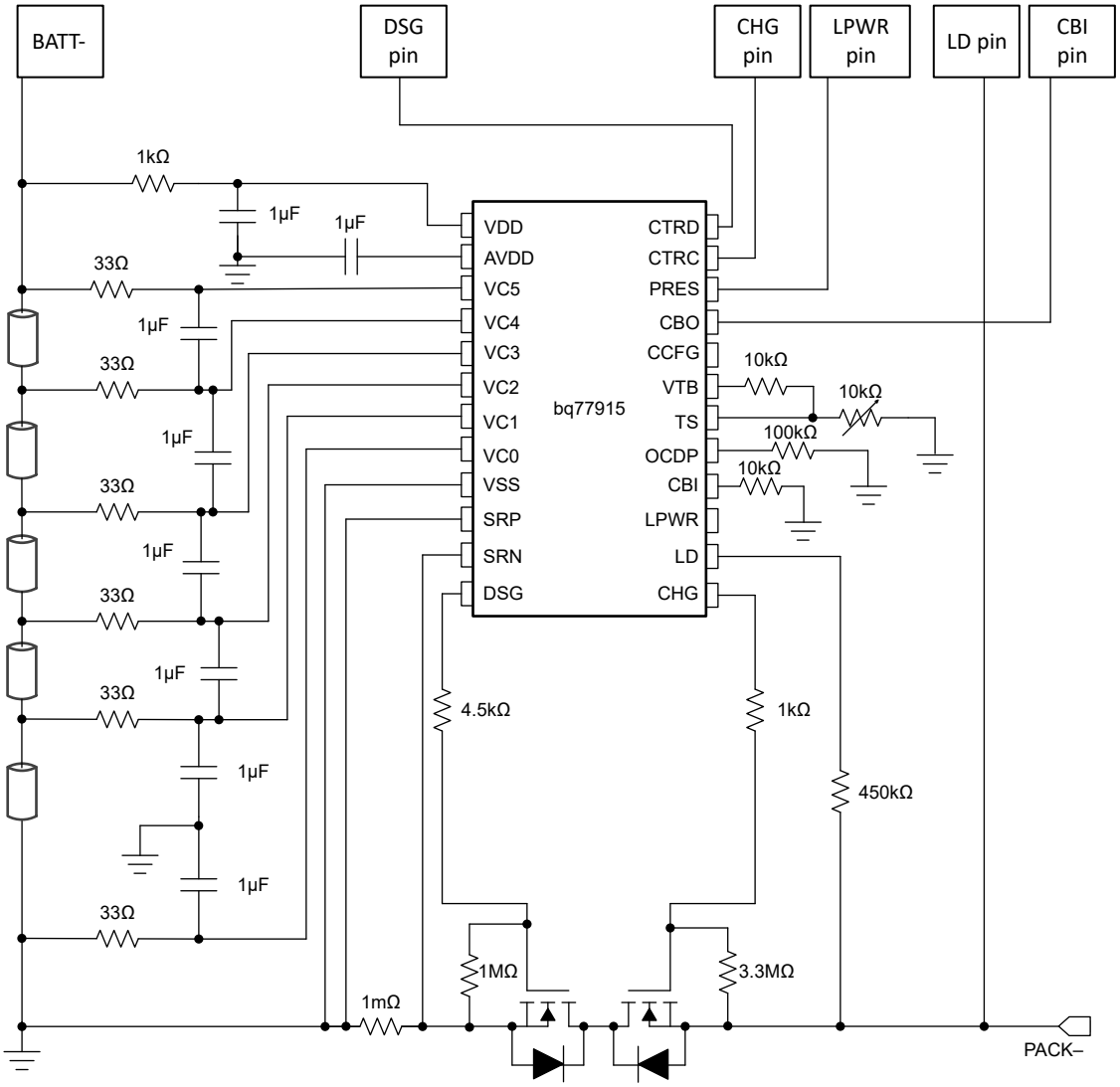

Figure 1-4. Bottom Device with HIBERNATE Mode Enabled

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2 Functionality

Sections Section 2.1 and Section 2.2 describe fault and recovery of the DSG and CHG FET controls. Each device in the stack is functional in protecting OV, UV, OTC, OTD, UTC and UTD faults.

2.1 Undervoltage (UV)

The UV fault test focuses on the DSG turnoff time as cell 17 is monitored below the desired threshold. In Figure 2-1, it is clear that DSG falls and stays low while any cell has a UV fault detected. When all faults are removed the DSG rises, see Figure 2-2. When examining the delay of the DSG rise and fall by measuring the delta between the UV threshold and DSG rise and fall, both figures display a similar response time of close to 1s due to the large R_{GS}. This is expected for the BQ77915 and needs to be accounted for appropriately in any system.

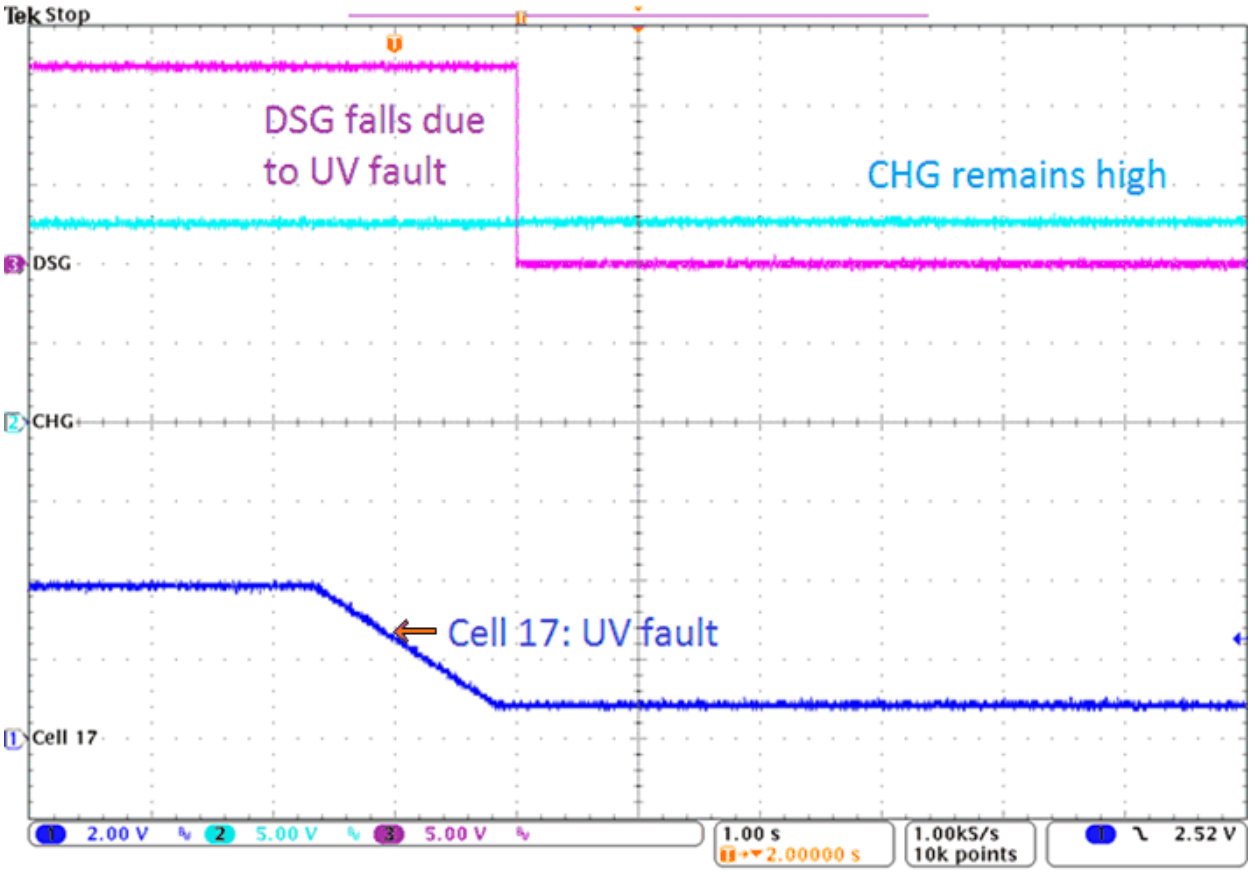

Figure 2-1. UV Detection

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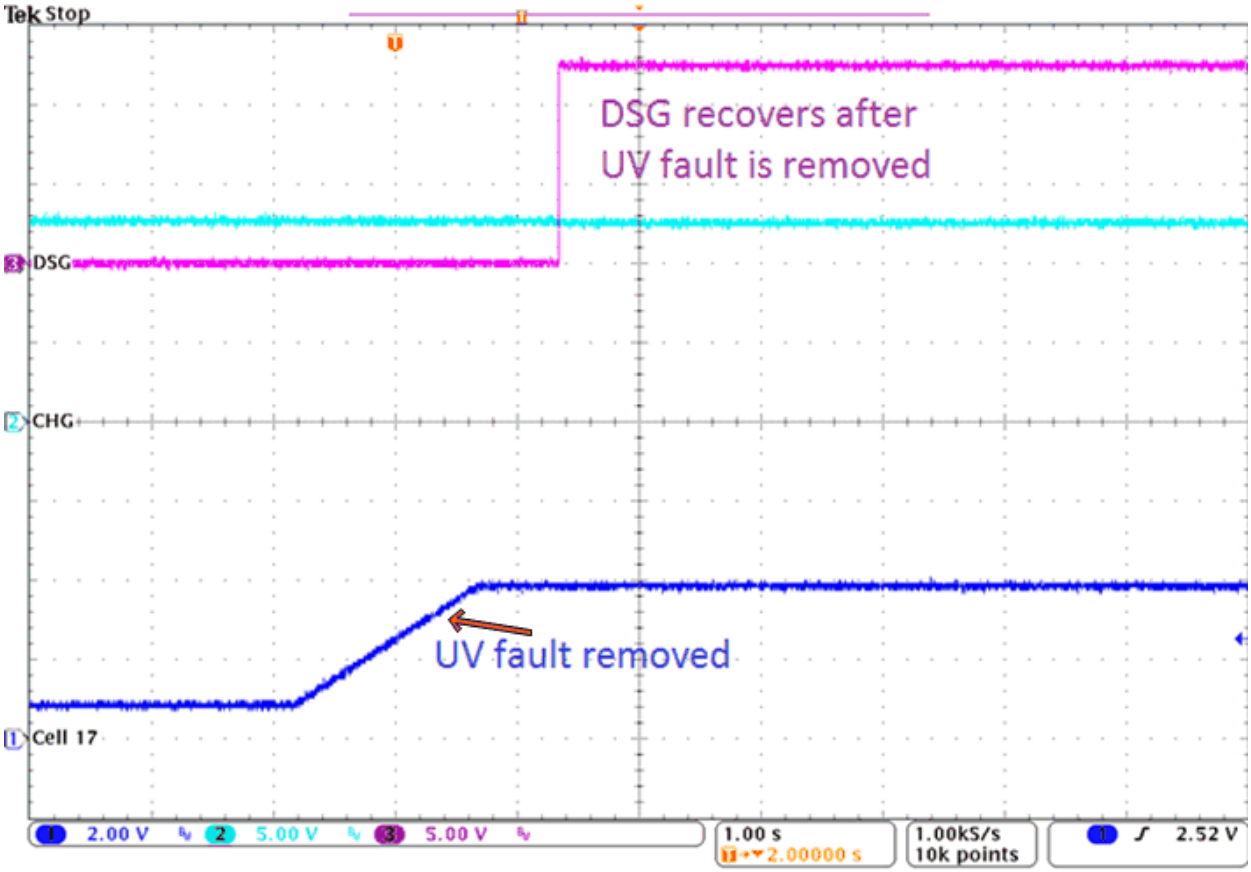

Figure 2-2. UV Recovery

2.2 Overvoltage (OV)

The OV fault test is almost identical to the UV fault test, but instead focuses on the CHG turnoff time as a cell is monitored above the desired threshold. As shown in Figure 2-3, the CHG pin falls due to the OV fault after a delay of approximately 500 ms. Recovery is shown in Figure 2-4.

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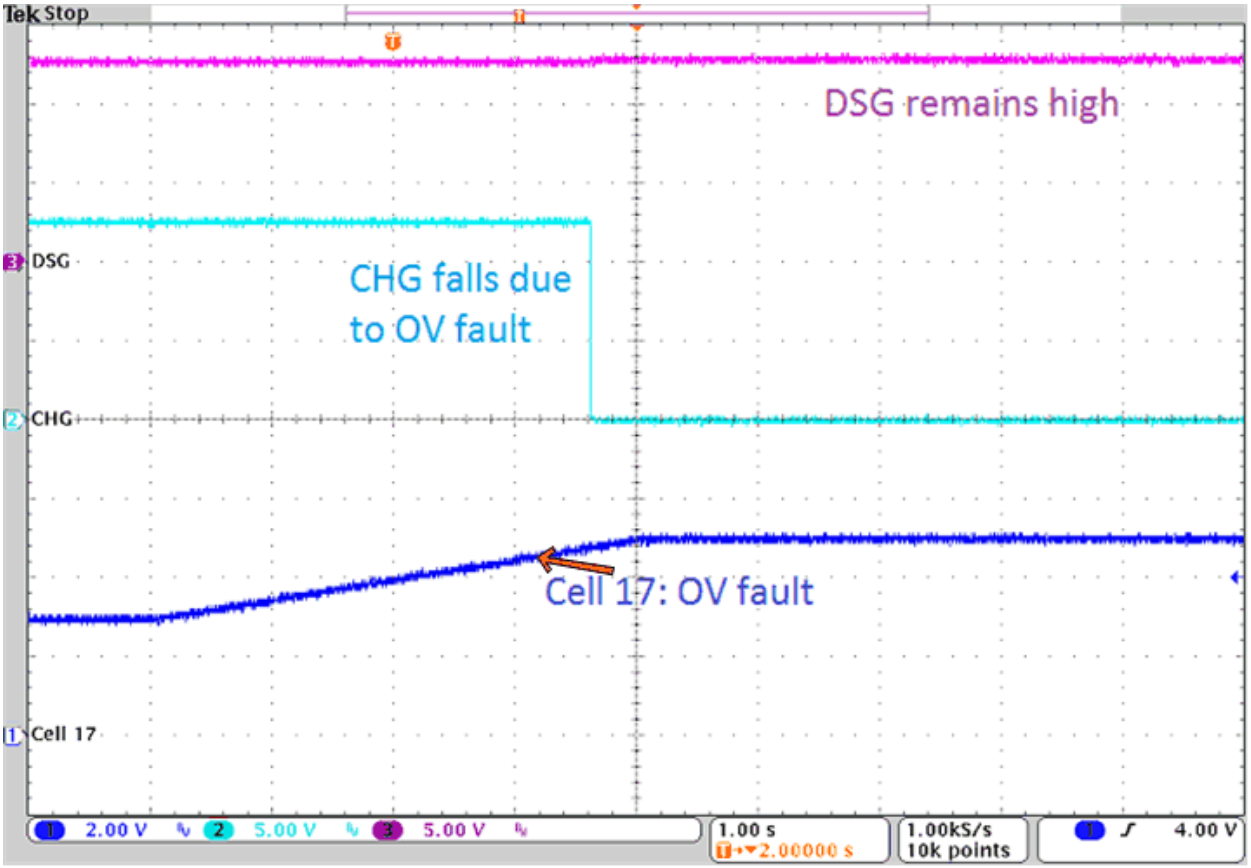

Figure 2-3. OV Detection

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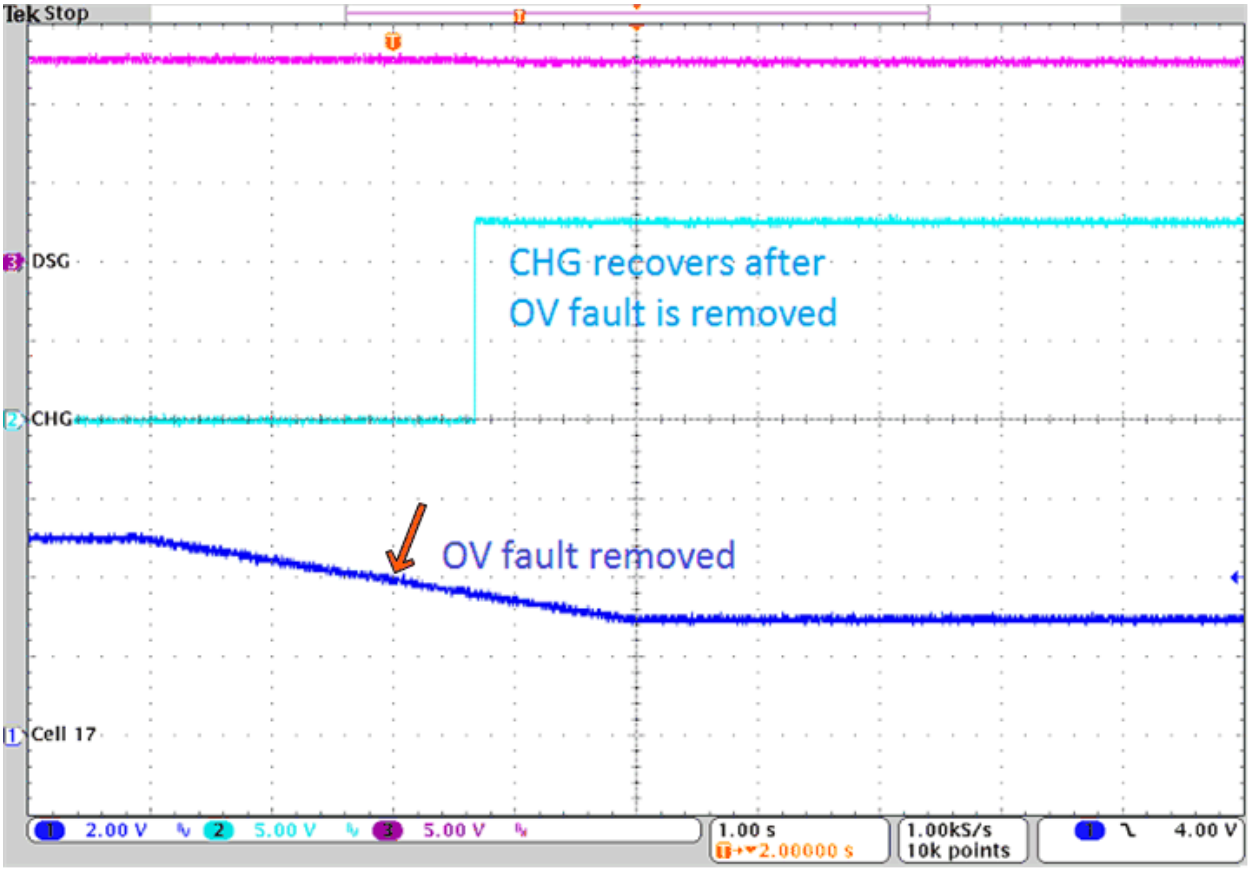

Figure 2-4. OV Recovery

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3 Troubleshooting FAQ

- Q: Is there a limit to how many technical devices a user can stack?
- A: The BQ77915 has no technical limitation on the number of devices in the stack. However, the larger the stack becomes, the greater the noise impact on the CTRC/D signal strength, and the greater the total delay time from the top to the bottom of the stack. This delay time is not an increase in the individual device protections, but it is a minimal increase due to logic propagation across each device in the stack. Typically this is only 1-10 ms per device added in the stack. Decide if this is a small enough margin for the application.
- Q: What happens if the user configures the lower devices to support more cells than an upper devices?
- A: The system must function appropriately, but TI does not recommended doing this as the CTRC/D signal strength across the stack is impacted. However, the tradeoff is lower gate voltage on the FETs. Determine which option is more effective for the specific application.
- Q: What changes must be made for a device to only support three or four cells?
- A: As mentioned in Section 9.3.12 in the data sheet, the CCFG pin must be configured appropriately, and the unused cells must always be selected as the uppermost cells and shorted to the immediate lower cell.

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4 References

- Texas Instruments, *bq77915 3-5S Low Power Protector with Cell Balancing and Hibernate Mode* data sheet

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2020) to Revision A (August 2020)	Page
• Changed schematic Rin value from 1kOhm to 330Ohm	2

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