Application Report

SLUA928A–December 2018–Revised March 2019

Low Dropout Operation in a Buck Converter

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ABSTRACT

Certain applications require the DC/DC to maintain output voltage regulation when the input voltage is only slightly higher than the target output voltage. They still require it to be regulated although the input voltage is lower than the target output voltage in some extreme cases. For a buck converter, these low dropout operation conditions require high duty cycle operation that may approach 100%. A similar description can be found like the following sentence in some buck converters datasheet: "To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1 V (typical)". However, when operating near 100% duty cycle with light loads, the Bootstrap capacitor can be discharged below the BOOT UVLO threshold, causing high ripple voltage on the output side. This application report discusses the cause and various operating modes associated with the low dropout operation. The TPS54231 is an example to introduce this operation behavior and providing work-around to maintain the Bootstrap capacitor voltage.

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Trademarks

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1 Introduction

An N-channel MOSFET is widely used in a buck converter as the high-side (HS) switch. To drive this HS MOSFET properly, a bootstrap circuit is designed to generate a floating power supply between gate node and source node of the MOSFET and an external small ceramic capacitor between the BOOT and PH pins is required. This bootstrap capacitor is refreshed when the HS MOSFET is off and the catch diode or low-side (LS) MOSFET conducts. An undervoltage lock-out (UVLO) circuit is also required for the gate drive supply to keep the converter from attempting to switch when the gate drive may be too low.

Certain applications require the DC/DC to maintain output voltage regulation when the input voltage is only slightly higher than the target output voltage. They still require it to be regulated although the input voltage is lower than the target output voltage in some extreme cases. For a buck converter, these low dropout operation conditions require high duty cycle operation that may approach 100%. However, when operating near 100% duty cycle with light loads, the Bootstrap capacitor can be discharged below the BOOT UVLO threshold, causing high ripple voltage on the output side.

This application report discusses the cause and various operating modes associated with the low dropout operation. This report uses the TPS54231 as an example to introduce this operation behavior and providing work-around to maintain the Bootstrap capacitor voltage. The end of this report introduces some synchronous parts with the low dropout operation has been improved.

2 TPS54231 Low Dropout Operation

The input voltage range for the TPS54231 is 3.5 V to 28 V, and the rated output current is 2 A. The TPS54231 is non-synchronous and its low-side switching element is an external catch diode. The TPS54231 can operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) depending on the output current.

Figure 1 shows the TPS54231 circuit used for testing. Some modifications are needed to investigate low dropout.

1. Remove R1 and R2 to float EN pin. Internal input voltage UVLO is used to allow operation at low input voltages without the device shutting off.
2. Change R6 to 53.6 kΩ when testing the 5 V output.

Use the TPS54231EVM-372 for evaluation which is an official EVM board for the TPS54231 device with 3.3 V output. Similar modifications are needed if using the official EVM board.

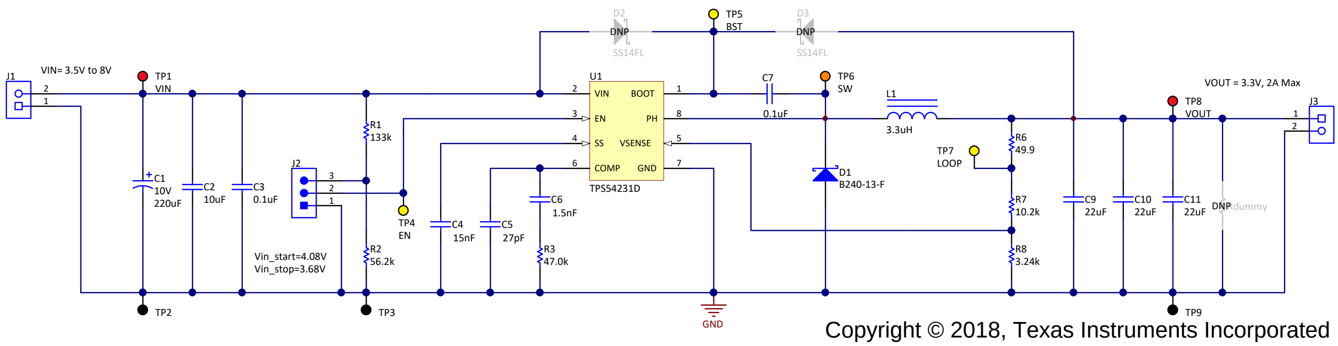

Figure 1. TPS54231 Test Circuit

2.1 Low Dropout Operation in CCM

In the CCM operation, when the HS MOSFET is turned off, the inductor current continues to flow in the catch diode, and the diode clamps the PH node voltage at one diode drop below ground. The BOOT to PH voltage is (V_{IN} + 0.7) V, allowing the Bootstrap capacitor to be fully charged. Therefore, low dropout operation can be obtained in CCM. Figure 2 illustrates the TPS54231 output waveforms at an input voltage of 4.25 V and an output current of 2 A. As the input voltage is 6 V, the Bootstrap capacitor voltage can remain higher than 2.1 V. The TPS54231 works in normal CCM with a nominal switching frequency of 580 kHz.

To improve dropout, the TPS54231 device is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1 V. For a buck converter, the duty cycle D = V_{OUT} / V_{IN}. Note that the effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, catch diode, and printed circuit board resistance. With the decreasing of VIN, the duty cycle is increased to maintain the output voltage. When the duty cycle approaches 100%, the on-time of the HS MOSFET can be extended with the effective switching frequency decreased. Figure 3 illustrates the TPS54231 output waveforms at an input voltage of 3.87 V and an output current of 2 A. The switching frequency has been reduced to approximately 34 kHz from the nominal of 580 kHz.

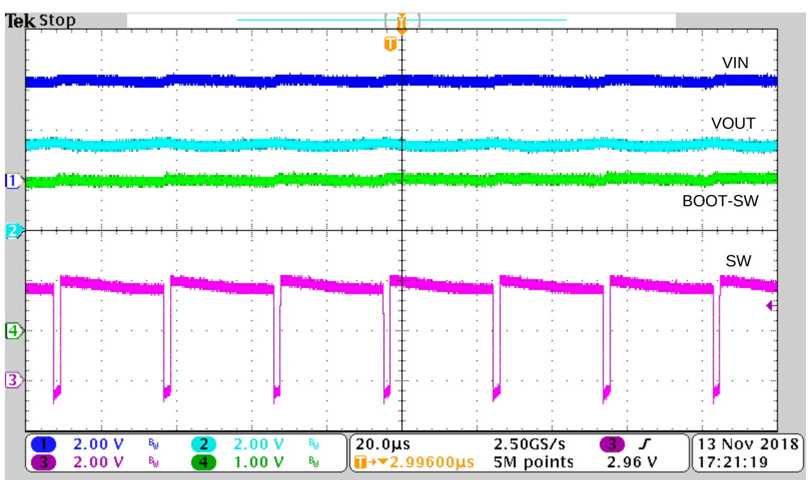

Figure 2. TPS54231 Waveforms at V_{IN} = 4.25 V, I_{OUT} = 2 A

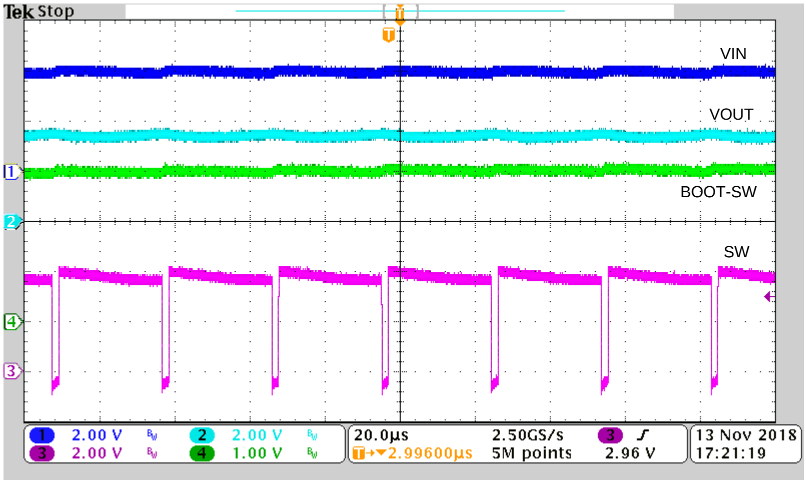

Figure 3. TPS54231 Waveforms at V_{IN} = 3.87 V, I_{OUT} = 2 A

2.2 Low Dropout Operation in DCM

Decreasing the output current makes the device work in DCM. Figure 4 and Figure 5 show the waveforms of the PH node with a different output current. There are three states during each duty cycle. During ON state, HS MOSFET is on, the catch diode D1 is off, and the PH node voltage equals to VIN. During the OFF state, HS MOSFET is off, D1 is on, and the PH node voltage is clamped one diode drop below ground. During IDLE state, both HS MOSFET and D1 is off, the PH voltage waveform oscillates because the output inductor, the junction capacitance of the catch diode and HS MOSFET constitute a resonant LC network. The Bootstrap capacitor can be charged during OFF state and IDLE state. Thus, low dropout operation can be obtained in DCM.

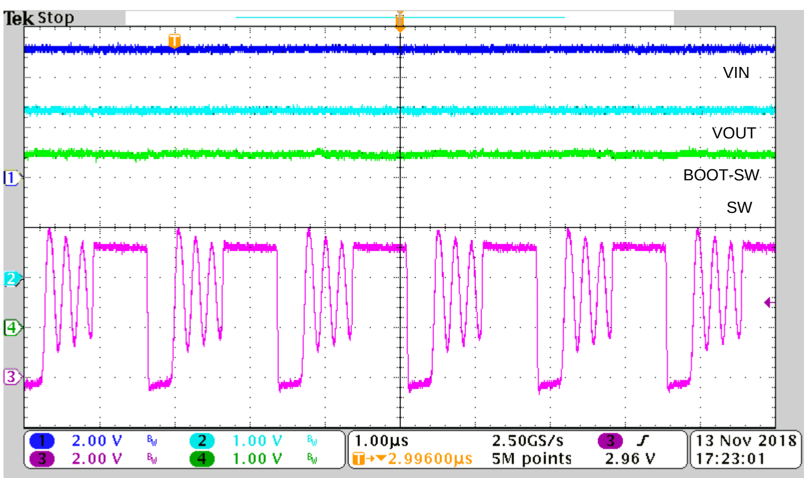

Figure 4. TPS54231 Waveforms at V_{IN} = 5 V, I_{OUT} = 0.1 A

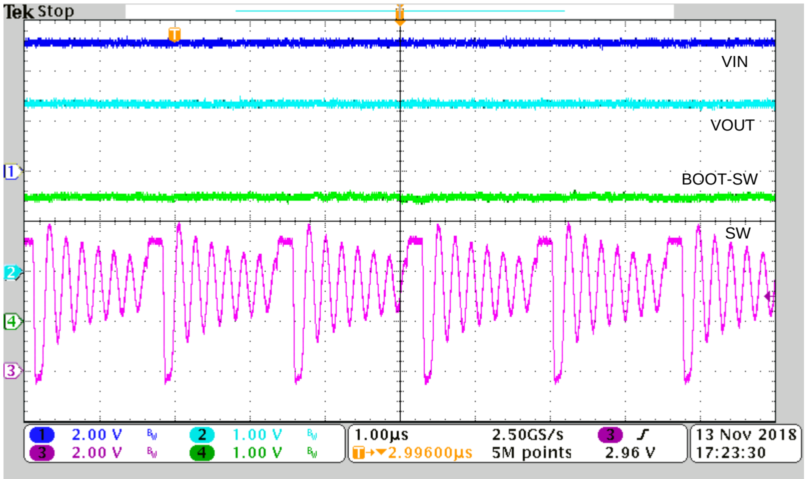

Figure 5. TPS54231 Waveforms at V_{IN} = 5 V, I_{OUT}= 10 mA

2.3 Low Dropout Operation in No-Load

In the no-load condition, there is no current flowing in the output inductor, so the OFF state is gone. The PH node voltage is very close to VOUT, and the BOOT to PH voltage is (VIN-VOUT). When running in low dropout operation, the (VIN-VOUT) can be significantly less than the BOOT UVLO voltage. If the (VIN-VOUT) is less than 2.1 V (the BOOT UVLO threshold), the device stops switching and the output voltage decays. As the output voltage decaying, the Bootstrap capacitor is charged until the output voltage decays to (VIN-2.1) and the HS MOSFET turns on again. Figure 6 shows a high ripple voltage was presented on the output.

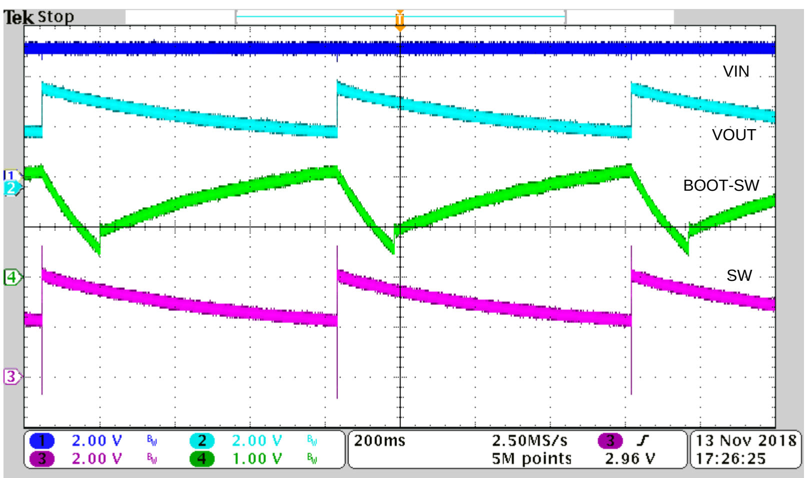

Figure 6. TPS54231 Waveforms at V_{IN}=5 V, I_{OUT}=0 A

When decreasing the input voltage from nominal 8 V with no load, the output begins to exhibit this ripple at a certain input voltage. This voltage is defined as the entry voltage. If the input voltage is increased again, the converter returns back to expected operation. This voltage level is defined as the recovery voltage. There is hysteresis between the entry and recovery voltages.

3 Solutions for Non-synchronous Part

Based on the above description, two basic methods can be used to improve the low dropout operation. Solution (A) is adding a dummy load at the output to keep the OFF state and extend the duration time. Solution (B) is adding an external voltage at BOOT pin to raise the BOOT to PH voltage directly.

Providing Continuous Gate Drive Using a Charge Pump Application Report: Used a charge pump to boost the BOOT to PH voltage on the basic of solution (B), however, it requires more additional counts with complex design, increasing BOM cost and solution size.

Methods to Improve Low Dropout Operation with the TPS54240 and TPS54260 Application Report: Provided four additional solutions on the basic of solution (B).

(1) Diode tied from input to BOOT

(2) Diode tied from output to BOOT

(3) Charge pump tied from output to BOOT

(4) Diode and resistor at PH

4 Design Example

Figure 7 and Figure 8 show the circuit of solution (1) + (A) and solution (2) + (A) with 3.3 V output.

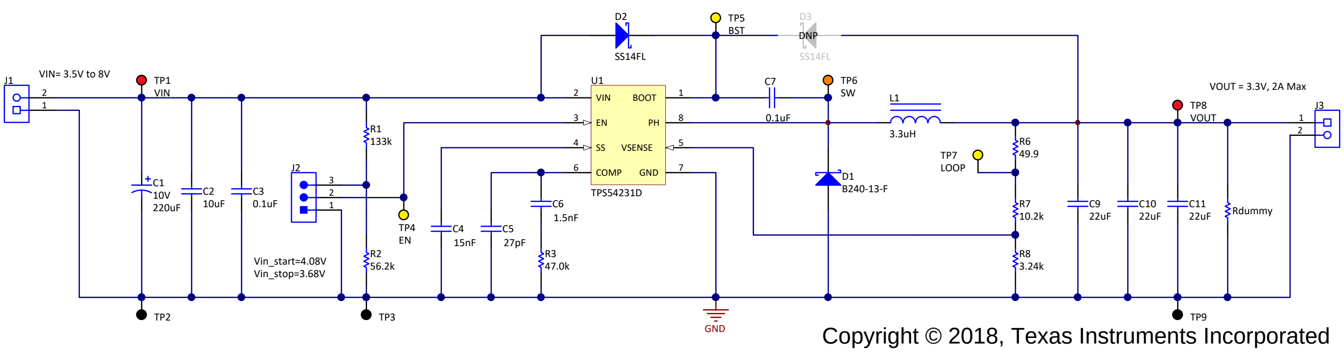

Figure 7. TPS54231 Circuit with Solution (1) + (A)

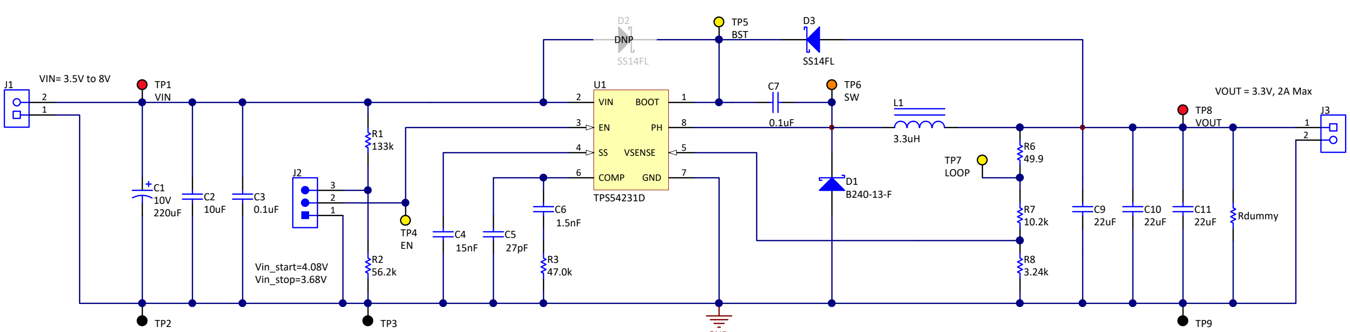

Figure 8. TPS54231 Circuit with Solution (2) + (A)

4.1 Auxiliary Diode Selection

The reverse voltage on the auxiliary diode is limited by the Bootstrap capacitor voltage. The reverse voltage equals the Bootstrap capacitor voltage when HS MOSFET is ON, and the absolute maximum rating of BOOT to PH is 8 V.

The charging current in the auxiliary diode is very small in normal running, but considering the extreme condition, a large peak charging current can be observed when powering on with a low output voltage, as shown in Figure 9 and Figure 10. A diode with 0.5-A average rectified forward current and 2-A peak repetitive forward current are required.

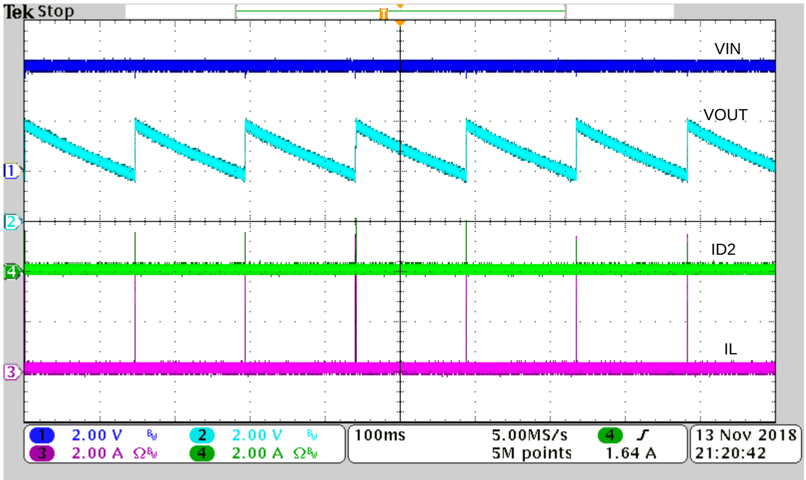

Figure 9. Current in Auxiliary Diode and Inductor

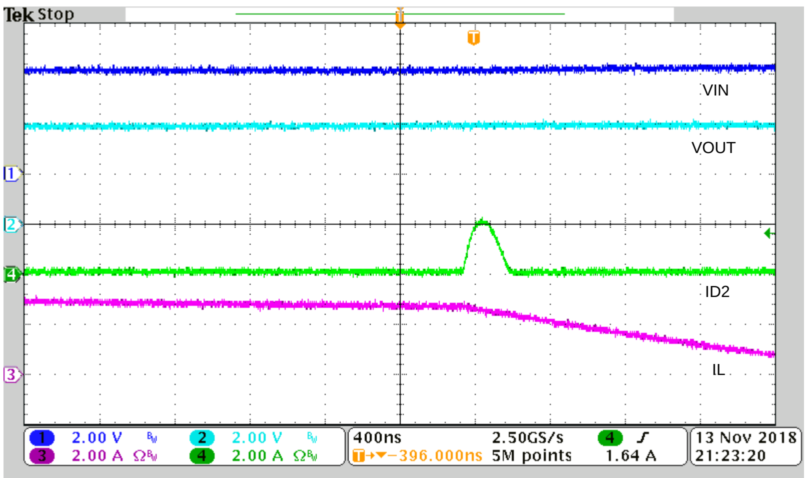

Figure 10. Current in Auxiliary Diode and Inductor (Zoom In)

There is a path for the leakage current from the Bootstrap capacitor to the VIN (VOUT) side through the auxiliary diode. The reverse current has an influence to the recovery voltage, especially under no-load. Three different schottky diodes are tried during the test. Table 1 shows the difference of entry and recovery voltage under light load. Figure 11 shows the reverse current under different reverse voltage based on bench test. The SS14 has the lowest reverse current of 1SS404 and B0520LW, thus the SS14 has a lower entry and recovery voltage.

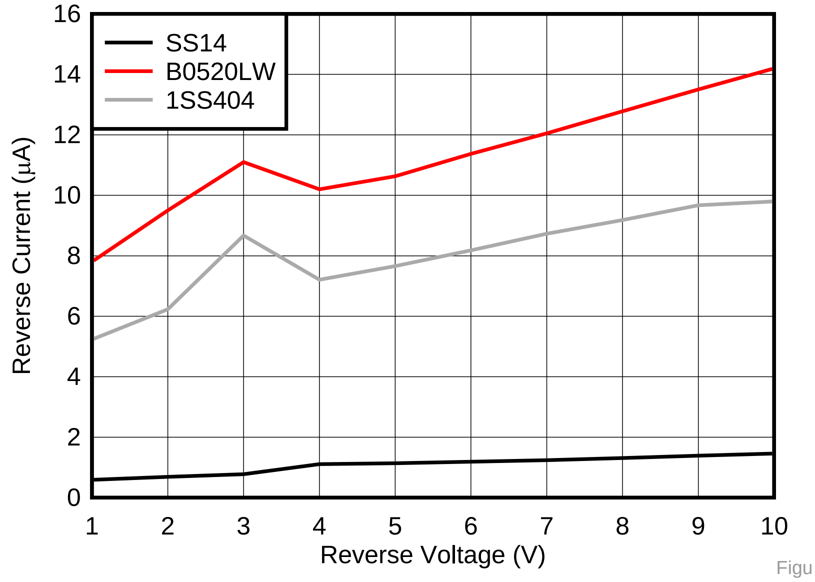

Figure 11. Reverse Current under Different Reverse Voltage

Table 1. The Entry and Recovery Voltages with Different Schottky Diodes

DIODE P/N	LOADING CURRENT (mA)	DIODE TIED FROM INPUT		DIODE TIED FROM OUTPUT	
		ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)
SS14	0	4.22	4.23	4.32	4.33
1SS404	0	4.24	5.56	4.80	6.19
B0520LW	0	4.43	5.6	4.59	6.19
SS14	1	4.22	4.23	4.32	4.33
1SS404	1	4.12	4.35	4.42	4.55
B0520LW	1	4.34	4.55	4.59	6.19
SS14	5	3.7	3.73	3.76	3.77
1SS404	5	3.67	3.972	3.70	4.42
B0520LW	5	3.77	4.05	3.83	4.51

4.2 Entry Voltage and Recovery Voltage

Table 2 and Table 3 show the entry and recovery voltage of solution (1), solution (2), and the original converter under a different dummy load current with 3.3 V and 5 V output. The solution (1) has lowest entry and recovery voltage and the smallest hysteresis voltage when compared to solution (2) and the original converter.

If you use a 1SS404 or B0520LW to do the same above test, their recovery voltage is higher than SS14 especial under light load. The root cause is the revere current of the auxiliary diode.

Table 2. The Entry and Recovery Voltages with V_{OUT} = 3.3 V

LOADING CURRENT (mA)	ORIGINAL CURRENT		DIODE TIED FROM INPUT		DIODE TIED FROM OUTPUT	
	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)
0	5.10	5.11	4.22	4.23	4.32	4.33
1	5.10	5.11	4.22	4.23	4.32	4.33

Table 2. The Entry and Recovery Voltages with V_{OUT} = 3.3 V (continued)

LOADING CURRENT (mA)	ORIGINAL CURRENT		DIODE TIED FROM INPUT		DIODE TIED FROM OUTPUT	
	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)
2	5.10	5.11	4.11	4.12	4.22	4.23
3	5.10	5.11	3.98	3.99	4.14	4.15
4	5.10	5.11	3.82	3.87	3.9	3.91
5	4.76	4.77	3.7	3.73	3.76	3.77
6	4.64	4.65	3.68	3.69	3.72	3.73
7	4.56	4.57	3.58	3.6	3.61	3.62
8	4.58	4.59	3.56	3.59	3.6	3.61
9	4.59	4.60	3.55	3.56	3.57	3.58
10	4.59	4.60	3.51	3.52	3.53	3.54
11	4.50	4.51	3.5	3.51	3.52	3.53
12	4.43	4.44	3.49	3.5	3.51	3.52
13	4.31	4.32	3.46	3.47	3.48	3.5
14	4.23	4.24	3.46	3.47	3.48	3.5
15	4.25	4.26	3.44	3.45	3.46	3.47

Table 3. The Entry and Recovery Voltages with V_{OUT} = 5 V

LOADING CURRENT (mA)	ORIGINAL CONVERTER		DIODE TIED FROM INPUT		DIODE TIED FROM OUTPUT	
	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)	ENTRY VOLTAGE (V)	RECOVERY VOLTAGE (V)
0	6.47	7.82	5.84	5.85	5.98	5.99
1	6.47	7.82	5.83	5.84	5.97	5.98
2	6.47	7.79	5.74	5.76	5.85	5.86
3	6.34	7.72	5.65	5.67	5.78	5.79
4	6.25	7.7	5.51	5.6	5.58	5.64
5	6.17	7.6	5.38	5.39	5.42	5.51
6	5.85	7.76	5.36	5.37	5.4	5.5
7	5.77	7.75	5.26	5.27	5.28	5.38
8	5.57	7.68	5.25	5.26	5.27	5.43
9	5.57	7.73	5.24	5.25	5.26	5.47
10	5.58	7.43	5.19	5.2	5.2	5.43
11	5.57	7.73	5.19	5.2	5.2	5.27
12	5.51	7.68	5.18	5.19	5.19	5.41
13	5.45	7.69	5.15	5.16	5.15	5.24
14	5.42	7.57	5.15	5.16	5.14	5.34
15	5.42	7.62	5.14	5.15	5.14	5.43

4.3 Input Capacitance

Large input capacitance can be required to ensure a low ripple voltage at the input side, which is helpful for the low dropout operation.

4.4 Bootstrap Capacitor Voltage

Figure 12 through Figure 15 show the bootstrap capacitor voltage of solution (1) under different load conditions. From Figure 14, the minimum load current is 3 mA to keep the bootstrap capacitor voltage higher than 2.1 V.

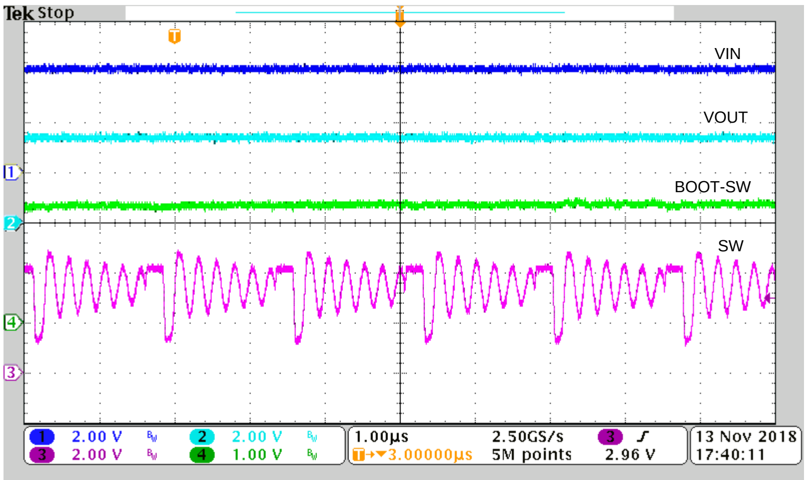

Figure 12. Bootstrap Capacitor Voltage Waveform with V_{IN} = 4 V, I_{OUT} = 3 mA

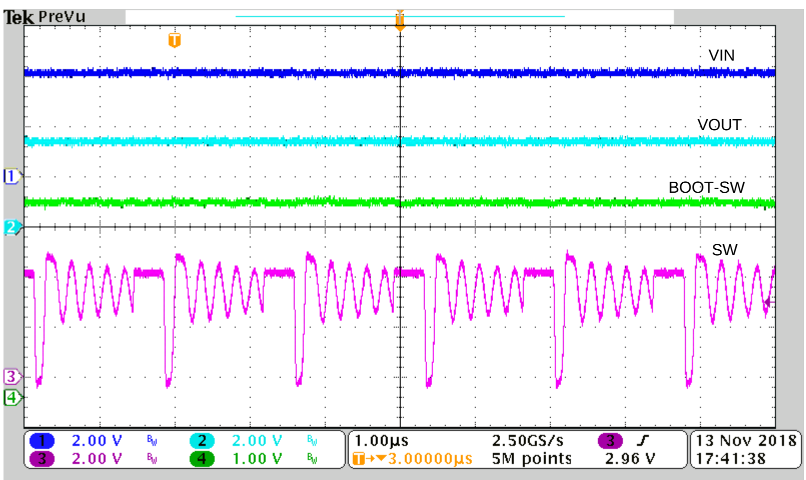

Figure 13. Bootstrap Capacitor Voltage Waveform with V_{IN} = 4 V, I_{OUT} = 10 mA

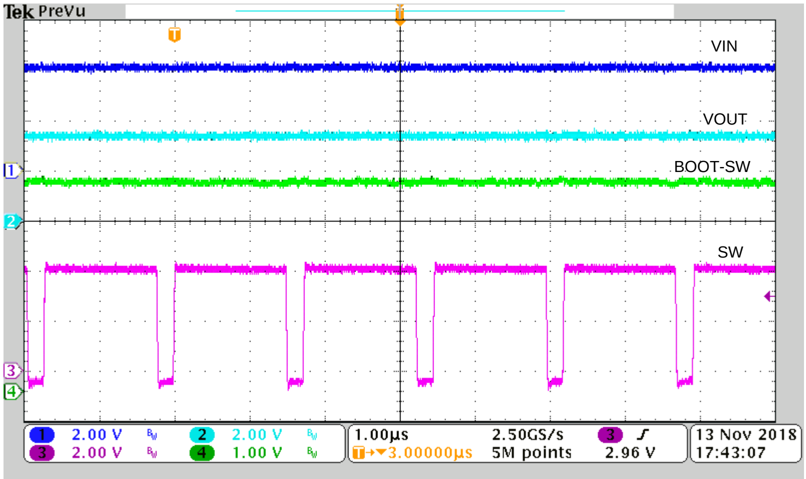

Figure 14. Bootstrap Capacitor Voltage Waveform with V_{IN} = 4 V, I_{OUT} = 1 A

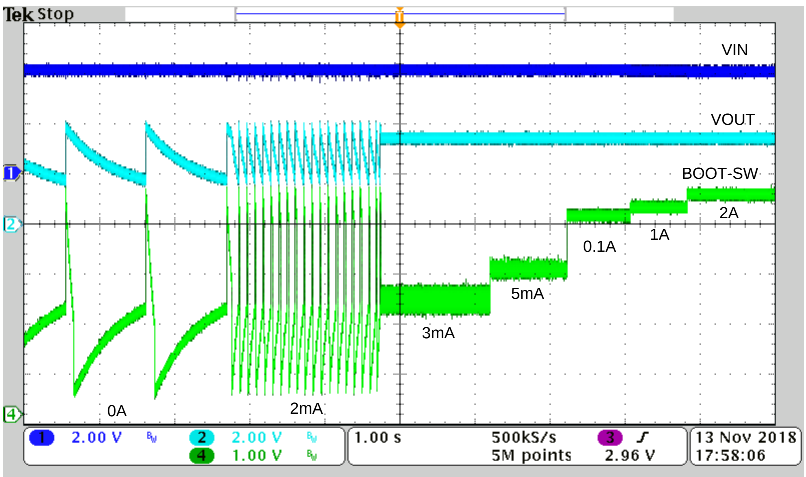

Figure 15. Bootstrap Capacitor Voltage Waveform with V_{IN} = 4 V, Variation I_{OUT}

4.5 Startup

Figure 16 and Figure 17 show the startup waveforms of solution (1) under different conditions.

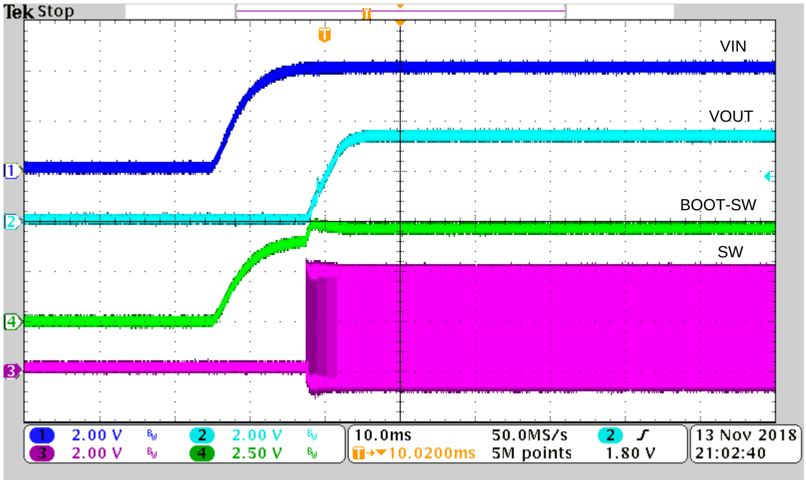

Figure 16. Startup Waveform with V_{IN} = 4 V, I_{OUT} = 2 A

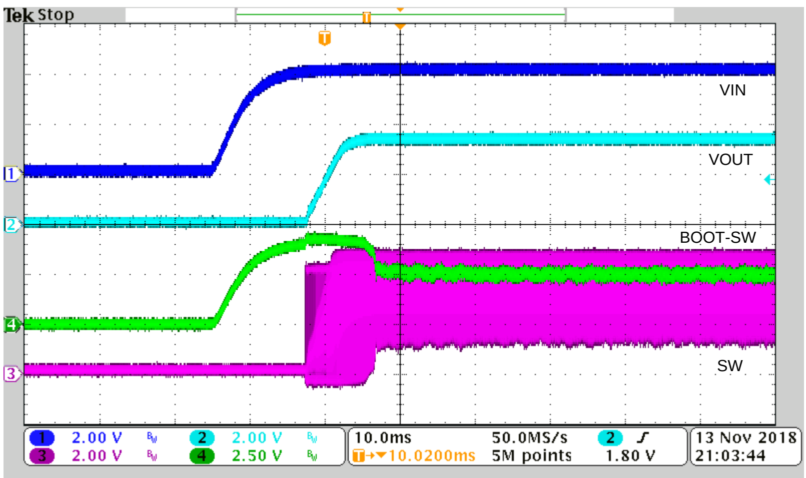

Figure 17. Startup Waveform with V_{IN} = 4 V, I_{OUT} = 3 mA

4.6 Load Transient Response

With a verified the load transient response, there is no significant difference in solution (1) and (2) compared to the original converter. Figure 18 through Figure 20 show the typical load transient response comparison results. The input voltage is 4 V, the output current step is from 25% to 75% of 2 A.

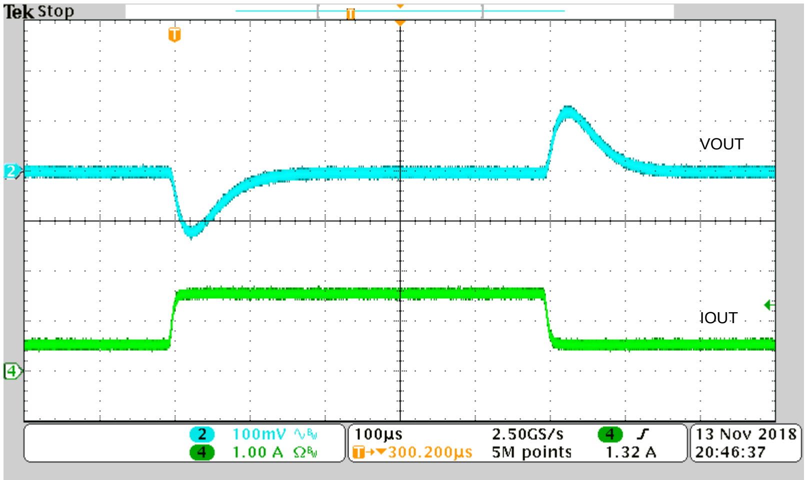

Figure 18. Load Transient of Solution (1)

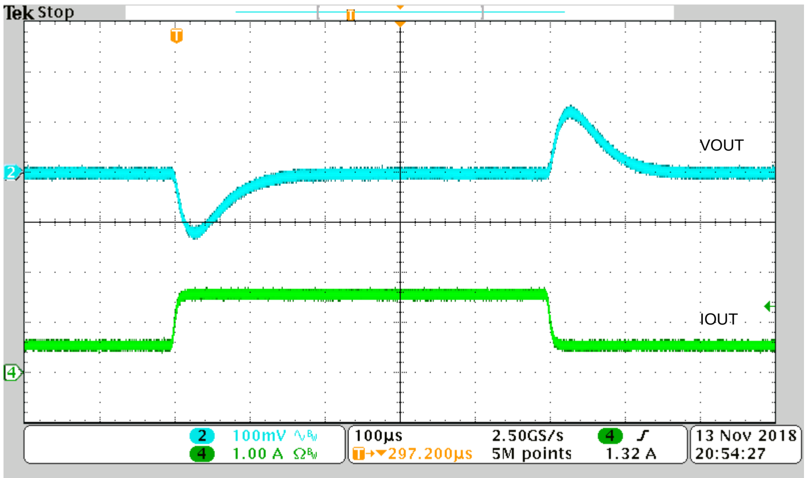

Figure 19. Load Transient of Solution (2)

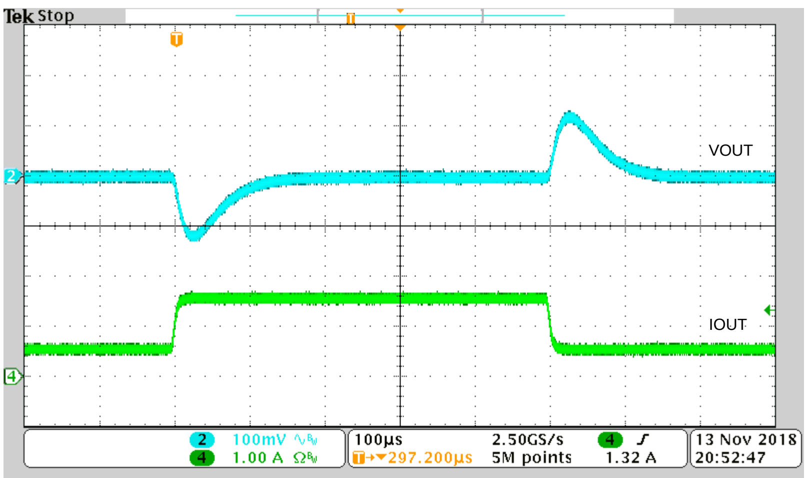

Figure 20. Load Transient of Original Converter

4.7 Efficiency

Figure 21 through Figure 23 show the efficiency of solution (1) and (2) with 3.3 V / 5 V output under different V_{IN}. The efficiency of solution (1) is lower than the efficiency of solution (2) and the original converter. Solution (2) has a closer efficiency performance to the original converter. The lower the input voltage, the higher the efficiency.

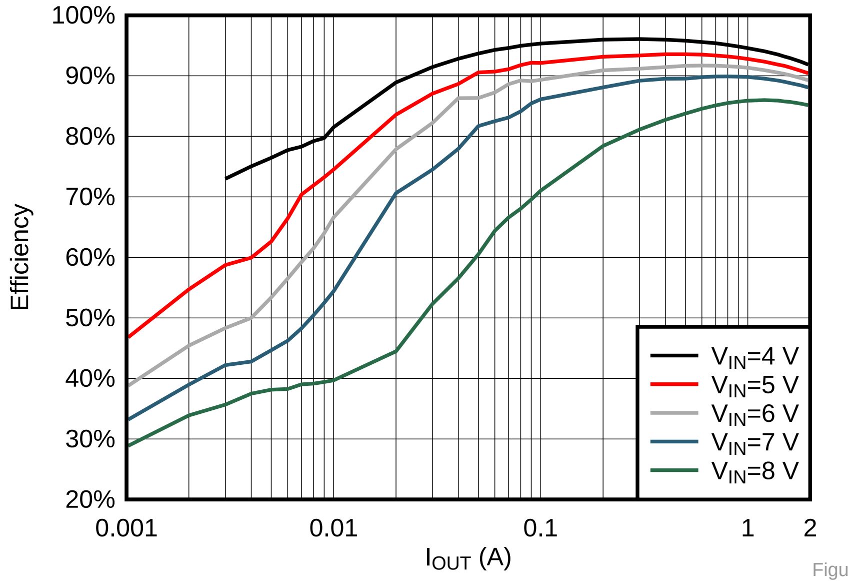

Figure 21. Efficiency of Solution (1) with 3.3 V Output under Different Input Voltage

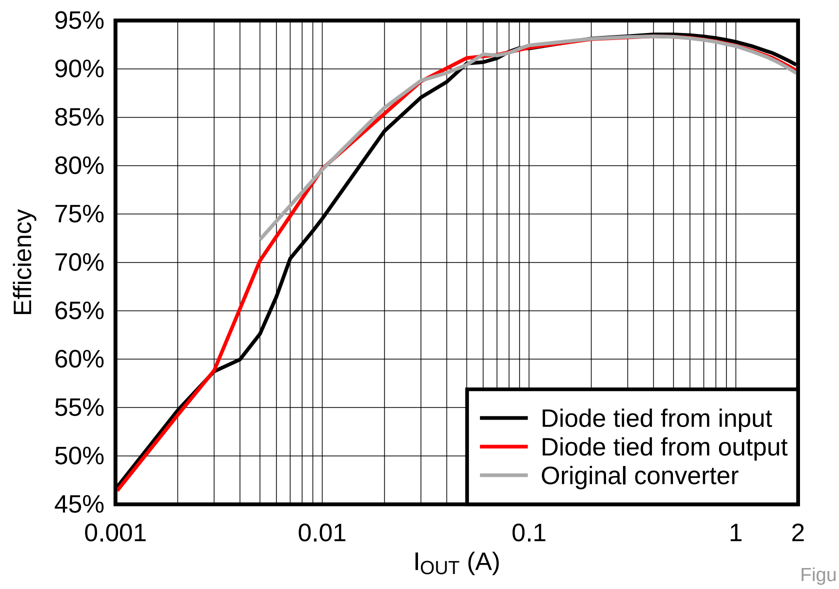

Figure 22. Efficiency Comparison with 5 V Input and 3.3 V Output

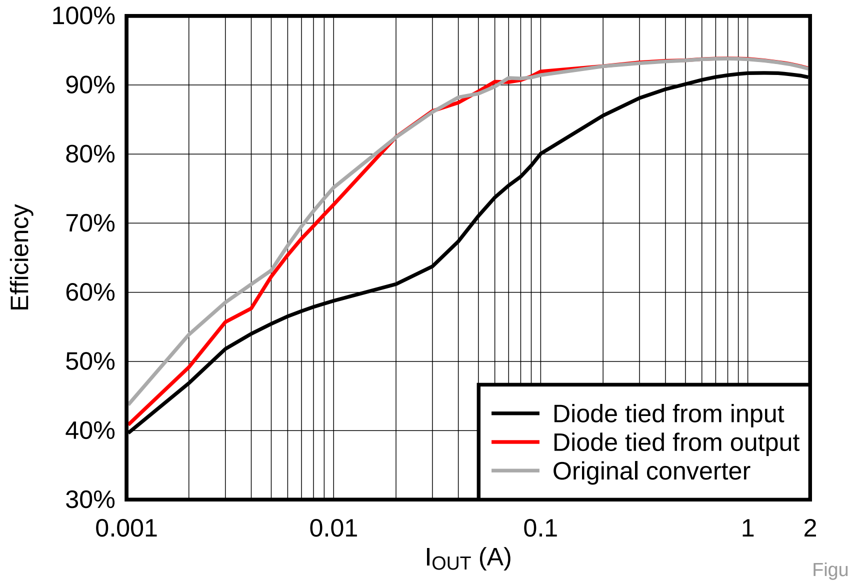

Figure 23. Efficiency Comparison with 8 V Input and 5 V Output

5 Low Dropout Operation Improved in Synchronous Part

Some synchronous parts like TPS54202, TPS54302 and TPS56339, are all designed to improve the drop out operation.

The TPS54202 and TPS54302 has a boot cap refresh function. When the BOOT UVLO is triggered, the LS MOSFET is forced to be OFF to charge the Bootstrap capacitor to maintain the Bootstrap capacitor voltage higher than 2.1 V. Figure 24 shows the typical operating waveform.

In the TPS56339, a frequency foldback scheme is employed to extend the maximum duty cycle when T_{OFF_MIN} is reached. The switching frequency decreases once a longer duty cycle is needed under low V_{IN} conditions. With the duty increase, the on time increases, until up to the maximum ON-time, 5-µs. The wide range of frequency foldback allows the TPS56339 output voltage to stay in regulation with a much lower supply voltage V_{IN}, leading to a lower effective dropout voltage. The boot cap voltage is always higher than 2.1 V. Figure 25 shows the typical operating waveform.

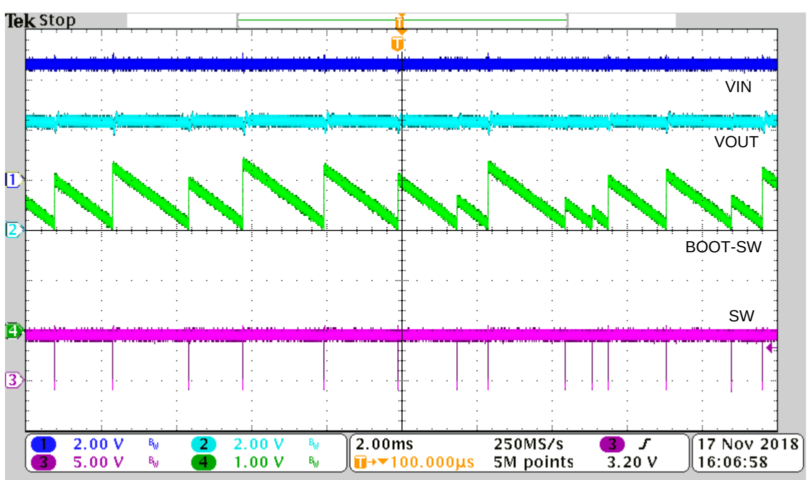

Figure 24. TPS54202 Waveforms, V_{IN} = 4.9 V, V_{OUT} = 5 V (Target), I_{OUT} = 2 A

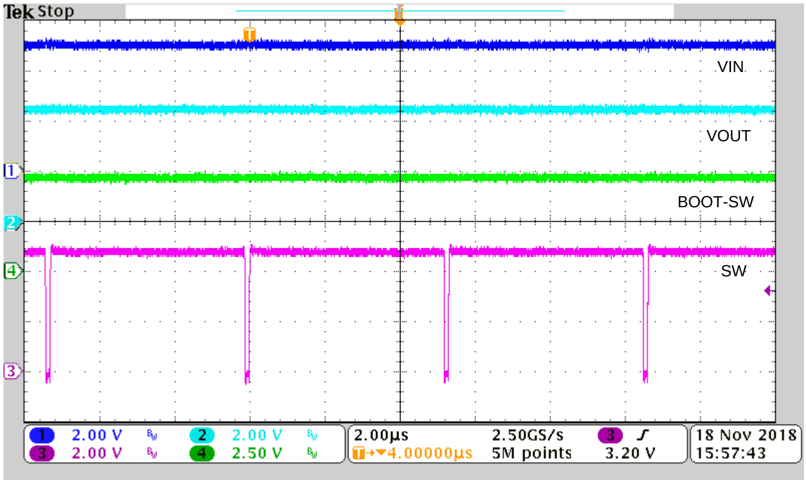

Figure 25. TPS56339 Waveforms, V_{IN} = 4.9 V, V_{OUT} = 5 V (Target), I_{OUT} = 3 A

6 Conclusion

This application report compares the two different solutions for improving the low dropout operation and provides guideline to the auxiliary diode selection.

The reverse current of the auxiliary diode has an influence to the entry and recovery voltage. A small ripple voltage at the input side would be helpful for the low dropout operation.

Solution (1): diode tied from input to BOOT, it has the lowest entry voltage and smallest hysteresis, lower efficiency, and a maximum input voltage is only 8 V.

Solution (2): diode tied from output to BOOT has no the above input voltage limitation, has the 8 V limitation of the maximum output voltage, and has a closer efficiency performance to the original converter.

The low dropout operation has been improved in synchronous part like the parts of TPS54202, TPS54302, TPS56339, and their family series part.

7 References

- Texas Instruments, *TPS54231 2-A, 28-V Input, Step-Down DC-DC Converter with Eco-mode Data Sheet*
- Texas Instruments, *TPS54202 4.5-V to 28-V Input, 2-A Output, EMI Friendly Synchronous Step Down Converter Data Sheet*
- Texas Instruments, *TPS56339 4.5-V to 24-V Input, 3-A Output Synchronous Step-Down Converter Data Sheet*
- Texas Instruments, *Providing Continuous Gate Drive Using a Charge Pump Application Report*
- Texas Instruments, *Methods to Improve Low Dropout Operation with the TPS54240 and TPS54260 Application Report*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2018) to A Revision	Page
• Edited application report for clarity.	1

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