

Understanding and Simulation of Loop Stability Test for DC/DC Converters



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ABSTRACT

Loop performance is critical for the proper operation in a DC-DC converter system. The stability test and its simulation are important in the converter design. This application note explains how an open-loop transfer characteristic is obtained in a closed-loop working converter. Besides, a simulation method is built in PSpice and verified, which can be applied in any DC-DC converters with transient PSpice models.

Table of Contents

| | |
|--|---|
| 1 Introduction..... | 2 |
| 2 Understanding of Loop Stability Test | 3 |
| 3 Loop Stability Test Circuit and Simulation in PSpice | 5 |
| 4 Conclusion..... | 8 |
| 5 References..... | 8 |

List of Figures

| | |
|--|---|
| Figure 1-1. Closed-loop Control Block Diagram..... | 2 |
| Figure 1-2. Loop Stability Test Connection in DC-DC converter..... | 2 |
| Figure 2-1. (a) DC-DC Converter with Closed-loop Control (b) DC-DC Converter with Open-loop Control..... | 3 |
| Figure 2-2. Open-loop Feedback with AC Voltage Injection..... | 3 |
| Figure 2-3. An Equivalent Closed-loop Connection with AC Voltage Injection..... | 4 |
| Figure 2-4. An Equivalent Closed-loop Connection with Frequency Response Analyzer..... | 4 |
| Figure 3-1. Frequency Sweeping Process in Loop Stability Test..... | 5 |
| Figure 3-2. Synchronous Buck Converter with Peak Current Mode Control in PSpice..... | 5 |
| Figure 3-3. Calculated Bode Plot of Buck Converter with Peak Current Mode Control..... | 6 |
| Figure 3-4. Loop Stability Test Circuit and Commands of Synchronous Buck Converter in PSpice..... | 6 |
| Figure 3-5. Calculated Bode Plot of Buck Converter with Peak Current Mode Control..... | 7 |

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1 Introduction

The DC-DC converter is a typical closed-loop control system. Loop performance is critical for the system to properly work. In a closed loop, response in output is determined by input interference and closed-loop control.

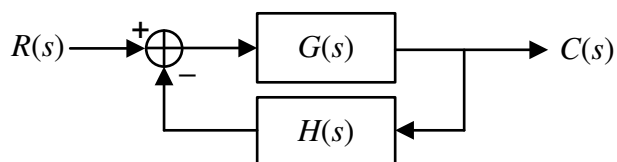


Figure 1-1. Closed-loop Control Block Diagram

Figure 1-1 shows the block diagram of a closed-loop system. From the diagram, loop performance is directly determined by closed-loop transfer function expressed in Equation 1.

$$\Phi(s) = \frac{G(s)}{1 + G(s)H(s)} \quad (1)$$

Calculation with closed-loop transfer function from s-domain to time-domain is the most straightforward method to check if the response is oscillating. A more simple judgement method on loop response is frequency stability criterion which is equivalent to Nyquist stability criterion. The frequency stability criterion checks Bode plot of open-loop transfer function as Equation 2.

$$\Phi'(s) = G(s)H(s) \quad (2)$$

To obtain a Bode plot of an actual DC-DC converter, a frequency response analyzer is often used to perform the loop test. Figure 1-2 shows the typical connection of the loop test in a DC-DC converter.

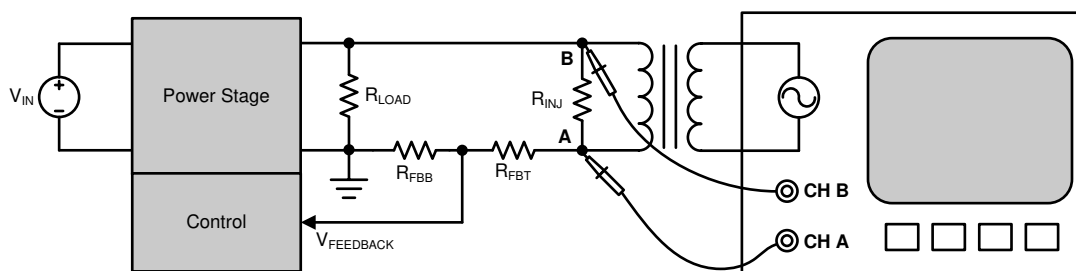


Figure 1-2. Loop Stability Test Connection in DC-DC converter

In a loop test, the analyzer will generate a small disturbance voltage signal at different frequency sweeping by certain step and collect the response at the same time. When the frequency sweep is done the analyzer will process the data and show Bode plot of open loop transfer function of the converter under test.

2 Understanding of Loop Stability Test

The purpose of a loop stability test is obtaining Bode plot of the open-loop transfer function in a closed-loop DC-DC converter. Consider a normally working converter circuit with a voltage feedback, shown in Figure 2-1(a).

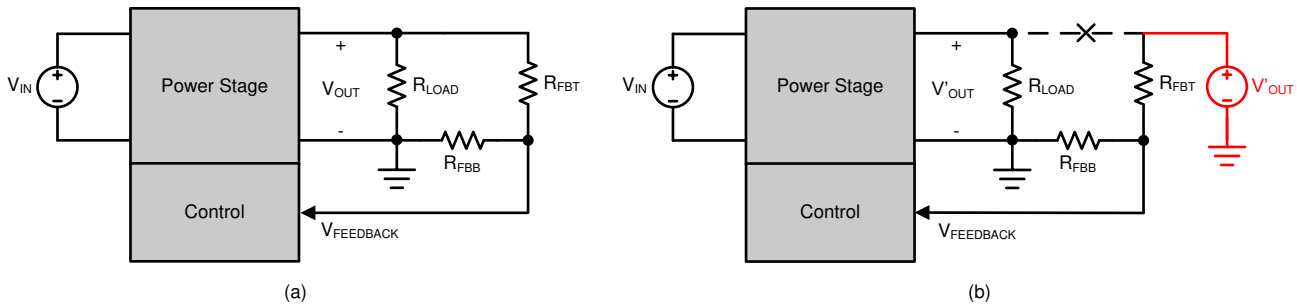


Figure 2-1. (a) DC-DC Converter with Closed-loop Control (b) DC-DC Converter with Open-loop Control

In Figure 2-1(a) the feedback voltage directly comes from output voltage and controls the same output simultaneously, making the converter a closed loop. Now make the top-side feedback resistor not connected to output voltage but to an external voltage source V'_{OUT} as shown in Figure 2-1(b). Then output voltage will be automatically adjusted to V'_{OUT} . If V'_{OUT} is equal to V_{OUT} , the working status in Figure 2-1(a) and (b) are exactly the same.

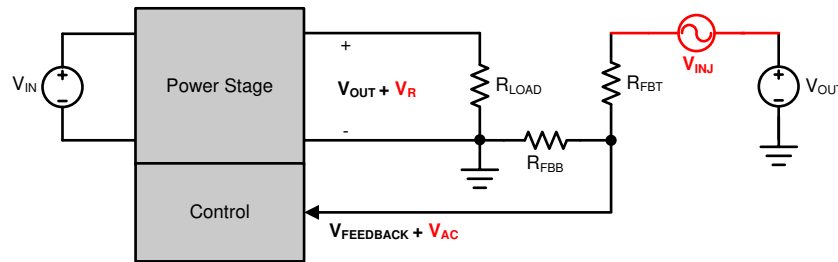


Figure 2-2. Open-loop Feedback with AC Voltage Injection

Consider an extra AC voltage source with small amplitude V_{INJ} applied in series with the external source, shown in Figure 2-2, then there will be an AC component V_{AC} in feedback voltage and thus output voltage V_{OUT} will also have an AC component V_R . V_R and V_{INJ} normally have different amplitude and are out-of-phase but their frequencies are same which are much lower than switching frequency of the converter. So the open-loop transfer response in both Figure 2-1(b) and (a) can be expressed in Equation 3.

$$G_{OPEN}(s) = \frac{V_R(s)}{V_{INJ}(s)} \tag{3}$$

The circuit in Figure 2-2 can be considered as basis of any loop stability test methods for DC-DC converters, in another word, any loop stability test circuits should be equivalent to it. Otherwise the test will lead to a wrong Bode plot.

When the above circuit is directly applied in a practical loop stability test, several high-precision measuring equipments are needed. Thus some simplifications are applied and here consider the circuit in Figure 2-3.

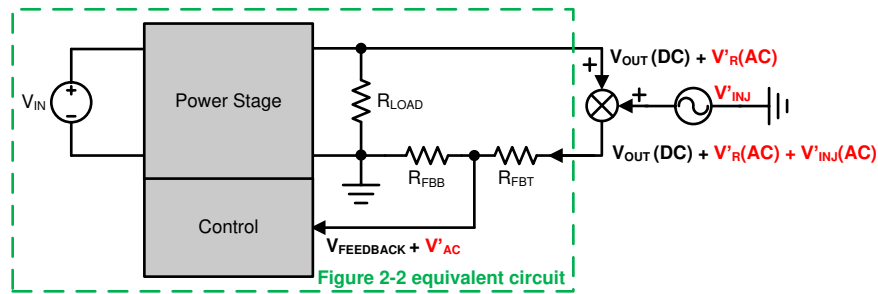


Figure 2-3. An Equivalent Closed-loop Connection with AC Voltage Injection

In [Figure 2-3](#) circuit, when the AC voltage V'_{INJ} is inserted in the closed-loop, there will be AC components with same frequency anywhere in the loop including output voltage, shown as V'_R . Here R_{FBT} will see an AC component as $V'_R + V'_{INJ}$ which is exactly equivalent to the V_{INJ} in [Figure 2-2](#) because V'_R and V'_{INJ} have a same frequency. The part of [Figure 2-3](#) circuit circled with dash line is actually the same as [Figure 2-2](#) circuit.

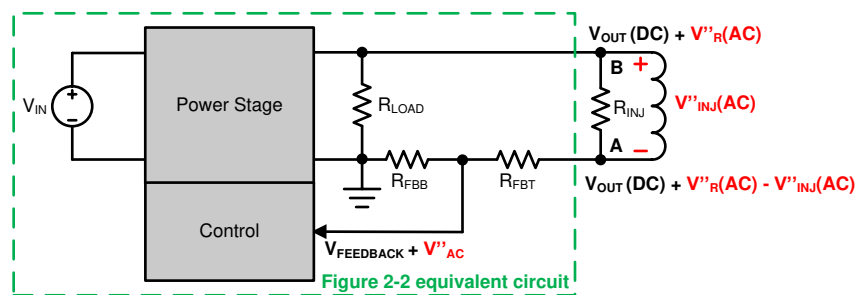


Figure 2-4. An Equivalent Closed-loop Connection with Frequency Response Analyzer

In a practical loop stability test, the connection outside dash line circle in [Figure 2-3](#) is achieved by a frequency response analyzer, shown in [Figure 2-4](#). The equivalent relations from [Figure 2-2](#) to [Figure 2-4](#) are described in the following equations.

$$V_R = V'_R = V''_R \quad (4)$$

$$V_{INJ} = V'_R + V'_{INJ} = V''_R - V''_{INJ} \quad (5)$$

The frequency response analyzer only collects and processes AC components of voltages at point A and B, so [Equation 3](#) can be expressed in [Equation 6](#):

$$G_{OPEN}(s) = \frac{V''_R(s)}{V''_R(s) - V''_{INJ}(s)} = \frac{V_{B(AC)}(s)}{V_{A(AC)}(s)} \quad (6)$$

When a frequency sweeping of injection signal is finished by analyzer, the gain and phase curves of $G_{OPEN}(s)$ in [Equation 6](#) will be displayed as the Bode plot of the converter loop.

3 Loop Stability Test Circuit and Simulation in PSpice

In a loop stability test, the frequency response analyzer draws Bode plot not by obtaining open-loop transfer function but by directly calculating on the gain and phase shift of the output and input signal. The process can be described in Figure 3-1.

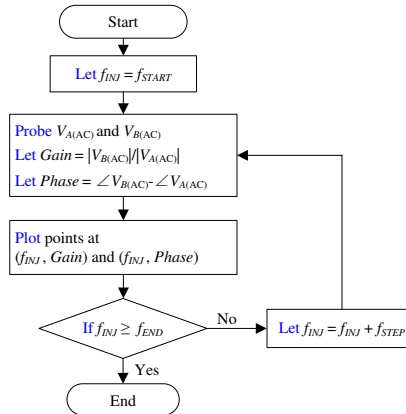


Figure 3-1. Frequency Sweeping Process in Loop Stability Test

In Figure 3-1, f_{INJ} is injection signal frequency, $[f_{START}, f_{END}]$ is frequency sweep range, $V_{A(AC)}$ and $V_{B(AC)}$ are AC components of voltages at injection and output voltage points.

In PSpice, a loop stability test simulation follows the same process. Consider a synchronous buck converter with a typical peak current mode control, shown in Figure 3-2.

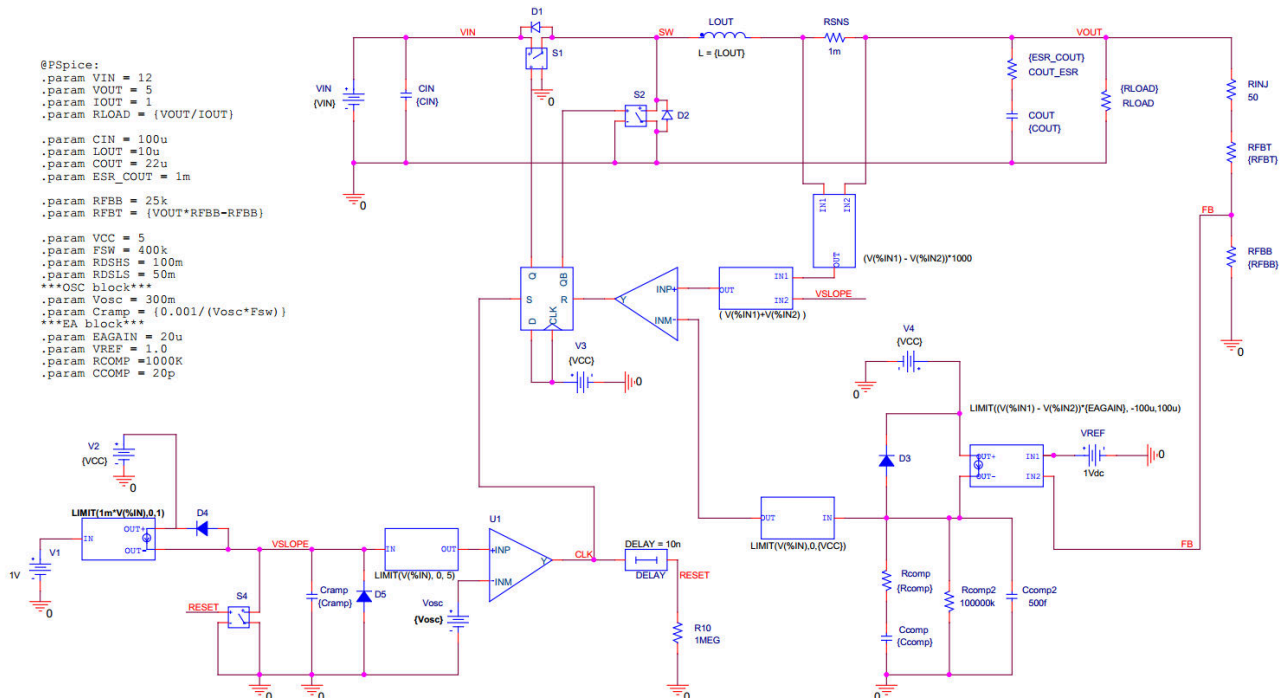


Figure 3-2. Synchronous Buck Converter with Peak Current Mode Control in PSpice

The open-loop transfer function is derived in the reference application note SNVA793. When taking the parameters of the circuit in Figure 3-2 into its transfer function, the theoretical Bode plot can be obtained shown in Figure 3-3.

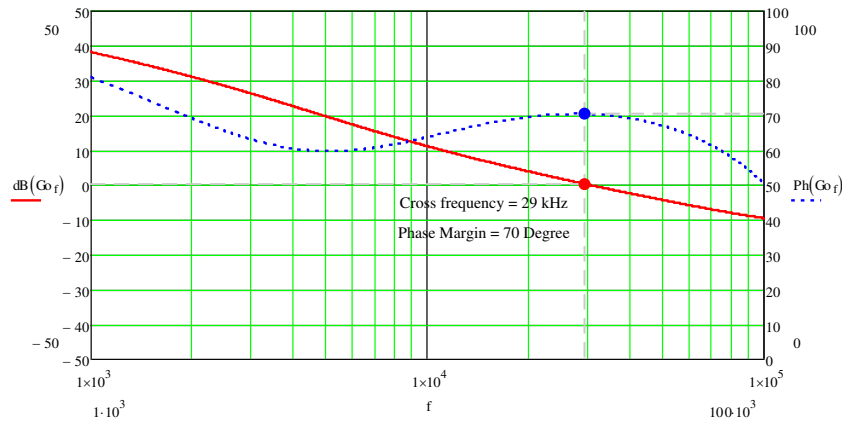


Figure 3-3. Calculated Bode Plot of Buck Converter with Peak Current Mode Control

When making a loop stability simulation, the circuit connection of ripple injection should be same as a practical loop test. Also, the part of frequency response analyzer function which is performing sweeping also needs to be achieved by PSpice commands. With these considerations, the simulation circuit is shown in Figure 3-4.

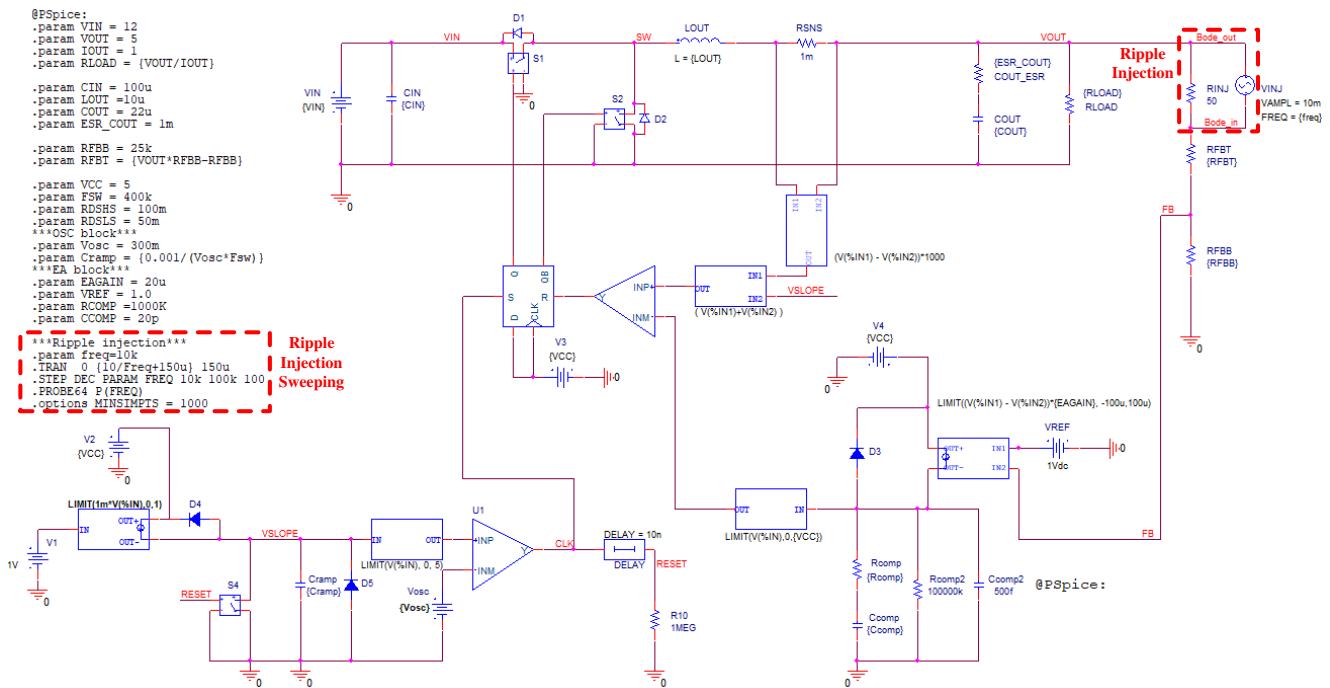


Figure 3-4. Loop Stability Test Circuit and Commands of Synchronous Buck Converter in PSpice

In Figure 3-4, an AC voltage source is connected in parallel with a typical 50-Ohm resistor. The voltage should be very low so that the DC operating point of converter won't be changed. A 10mV-amplitude source is applied in this case. The frequency of AC source will be on sweep so a variants freq is used. With the proper connection of ripple injection, frequency sweeping is achieved by PSpice commands which are listed in the red box. The below are detailed descriptions of the commands.

Line 1: .param freq = 10k

Line 1 is the definition of freq and it also sets the default value.

Line 2: .TRAN 0 {10/Freq+150u} 150u

On Line 2, simulation time at a single frequency point is defined. Normally it starts from 0 to a certain time after the converter reaches steady operating. In this case, the buck converter works steadily after 150 us. Before it, it's on start-up and not suitable for a loop test. After 150 us, the remaining simulation time is 10 cycles at present frequency. 10 cycles are long enough for the simulator to calculate the gain and phase shift on input and output signals.

Line 3: .STEP DEC PARAM FREQ 10k 100k 100

Line 3 defines the total range and steps of frequency sweep. In this case, the sweep starts from 10 kHz and ends at 100 kHz. The steps number is 100 in each 10 times. So there will be totally 100 steps from 10-kHz to 100-kHz range.

Line 4: .PROBE64 P(FREQ)

Line 4 is probe and plot command in PSpice.

Line 5: .options MINSIMPTS = 1000

Line 5 specifies the minimum number of points per section in simulation output.

When running the simulation, a cluster of waveforms will be simulated and loaded on the probe window. Choose the FRA function and use the waveform data file, respectively set trace 1 and 2 by Bode-out and Bode_in net. Then the Bode plot can be processed, shown in [Figure 3-5](#).

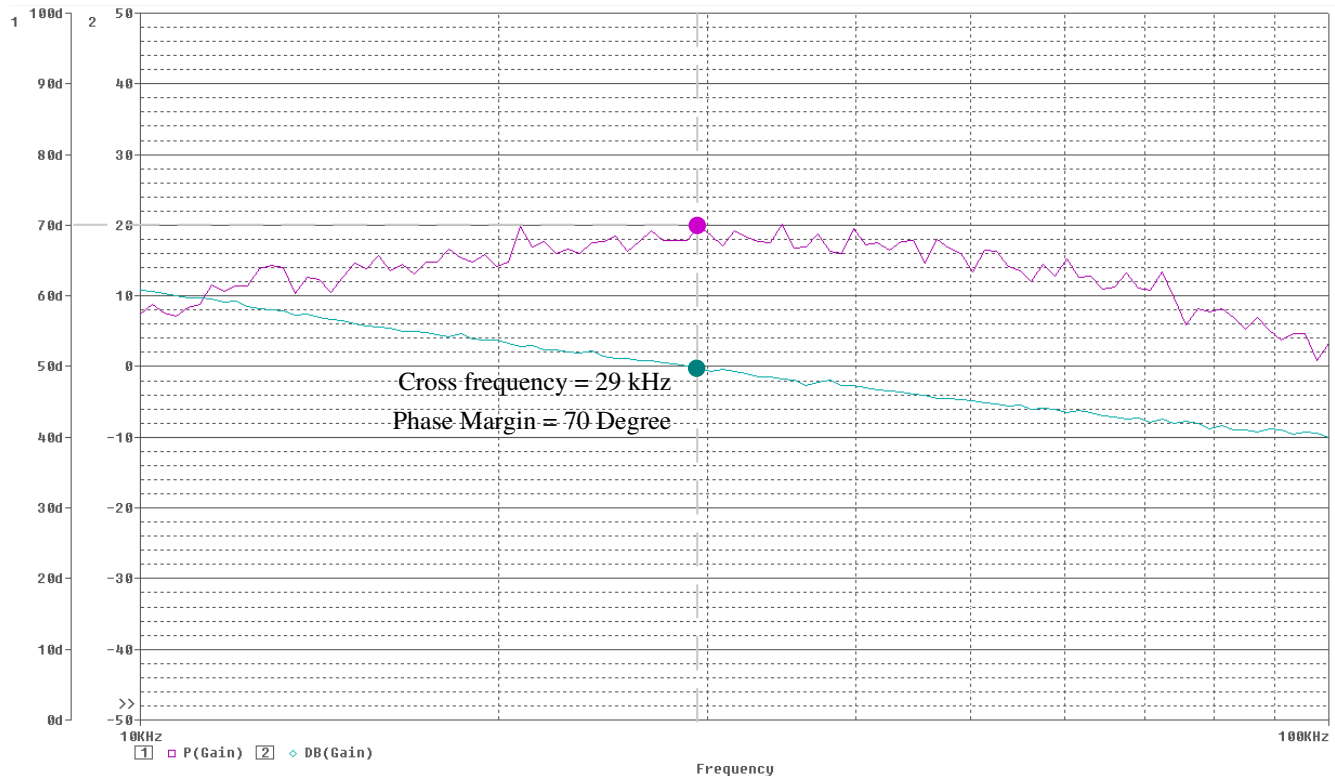


Figure 3-5. Calculated Bode Plot of Buck Converter with Peak Current Mode Control

The simulated Bode plot has little deviation compared with the calculated one. Thus, it verifies the loop test injection circuit and frequency response analyzer modeling so that can be applied in any kinds of DC-DC converter simulations with transient PSpice models.

4 Conclusion

This application report firstly explains how an open-loop transfer characteristic is obtained in a closed-loop working converter. Then a simulation method of loop stability test for a synchronous buck converter with peak current mode is built in PSpice. The simulation result shows it has little deviation compared with calculation results in theory. Thus, the simulation method can be applied in any kinds of DC-DC converter simulations with transient PSpice models.

5 References

- Texas Instruments, [How to Evaluate the Maximum Inductor in an Internal Compensation PCM Buck Converter](#)

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