Application Report

Flyback Aux Winding OVP and UVLO Fault Sensing Design and Troubleshooting Tips

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ABSTRACT

Texas Instruments has developed discontinuous mode (DCM) flyback controllers that use transformer coupling to sense the input voltage (V_{IN}) and output voltage (V_{OUT}) for power supply control; as well as, circuit fault protection. These voltages are sensed across the flyback transformer (T1) auxiliary winding (V_{AUX}) of the flyback converter shown in Figure 1-1. The problem with this technique is if the aux winding is noisy it could falsely trigger and input under voltage lockout (UVLO) fault or an output over voltage protection (OVP) fault and unexpectedly shut down the system. The purpose of this application report is to give design guidance to resolve and avoid false OVP and UVLO faults caused by noise on the aux winding. TI primary-side regulated (PSR) DCM flyback controllers that use this kind of auxiliary winding sensing for OVP and UVLO are the UCC28700/1/2/3/4, UCC28710/1/2/3, UCC28720/22 UCC28730, UCC28910/1. The UCC28740/2 secondary side regulated (SSR) controllers also use auxiliary winding fault sensing.

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Trademarks

1 Introduction

Texas Instruments has developed discontinuous mode (DCM) flyback controllers that use transformer coupling to sense the input voltage (V_{IN}) and output voltage (V_{OUT}) for power supply control; as well as, circuit fault protection. These voltages are sensed across the flyback transformer (T1) auxiliary winding (V_{AUX}) of the flyback converter shown in Figure 1-1. The problem with this technique is if the aux winding is noisy it could falsely trigger and input under voltage lockout (UVLO) fault or an output over voltage protection (OVP) fault and unexpectedly shut down the system. The purpose of this application report is to give design guidance to resolve and avoid false OVP and UVLO faults caused by noise on the aux winding. TI primary-side regulated (PSR) DCM flyback controllers that use this kind of auxiliary winding sensing for OVP and UVLO are the UCC28700/1/2/3/4, UCC28710/1/2/3, UCC28720/22 UCC28730, UCC28910/1. The UCC28740/2 secondary side regulated (SSR) controllers also use auxiliary winding fault sensing.

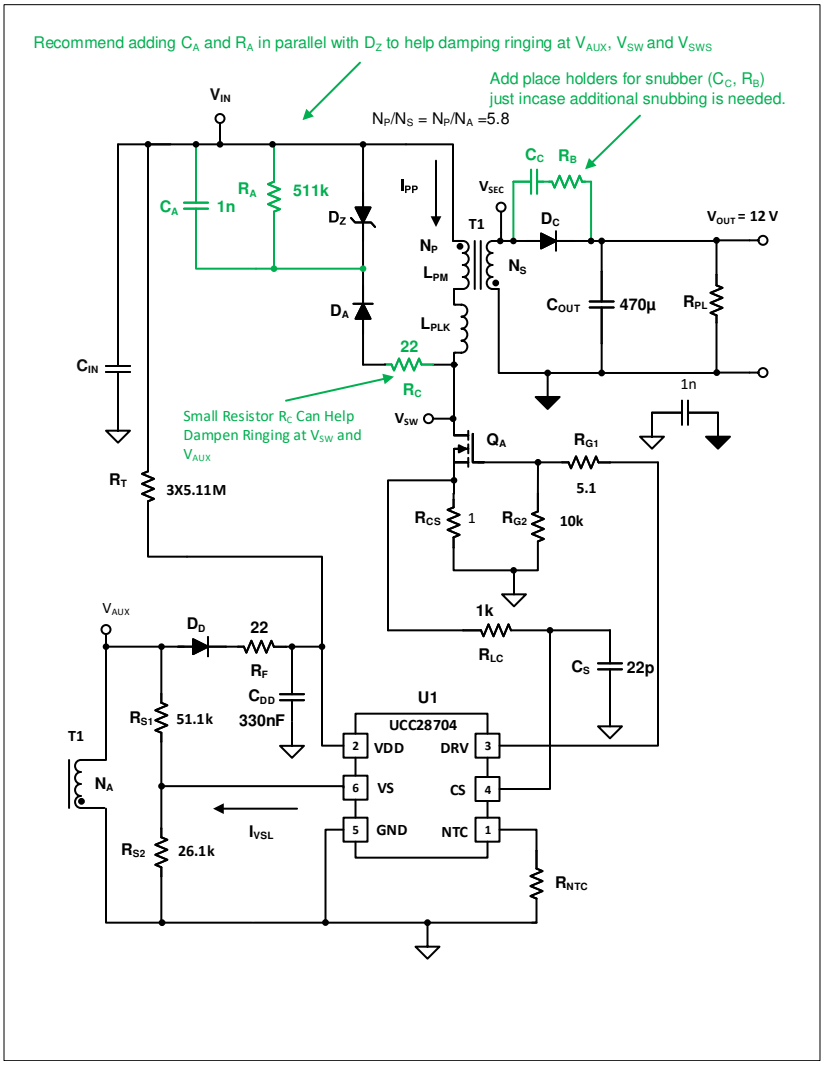


Figure 1-1. DCM Flyback Converter Using Auxiliary Winding Sensing to Detect Input UVLO and OVP

2 Brief Review of DCM FM, AM, FM Flyback Control Law

The DCM flyback controllers presented here use Frequency Modulation (FM) and Primary Peak Current Modulation (AM) to control the flyback converters frequency, duty cycle, primary peak current and output voltage. These controllers sense the output voltage at the VS pin of the flyback controller (Figure 1-1) and will adjust an internal control voltage (V_{CL}) to adjust the primary peak current (I_{PP}) and the converters switching frequency (f_{SW}). This control technique is known as control law. The control law of the UCC28704 is presented in Figure 2-1. All of the devices presented in this paper use similar control laws but are parametrically different. It is required that the designer review the data sheet of the specific flyback controller they are using in their design for specific control law details.

When the converter operates at maximum load and at the minimum input voltage the application operates in critical conduction at the converter's maximum switching frequency, (fsw(max)).

When the converter operates in region 4 if less duty cycle is required, the internal feedback amplifier will adjust V_{CL} from 4.85 V to 3.0 V to decrease f_{SW} to obtain the correct duty cycle to maintain V_{OUT}. The f_{SW} will be adjusted from $f_{SW(max)}$ to 25 kHz minimum in region 4.

In region 3 when the converter is operating at 25 kHz, the flyback controller will adjust the primary peak current (I_{PP}) amplitude to adjust the duty cycle. The peak current varies from the maximum programed I_{PP} to $I_{PP}/4$ to maintain the duty cycle. The device adjusts V_{CL} from 3 V to 2.2 V in this region.

In region 2 with the primary peak current controlled to $I_{PP}/4$ if the controller needs less duty cycle it decreases the switching from 25 kHz to control the duty cycle. In this region V_{CL} operates from 2.2 V to 1.3V.

In region 1 when V_{CL} is below 1.3 V the converter is operating at the minimum switching frequency and requires a pre-load resistor (R_{PL}) to maintain regulation.

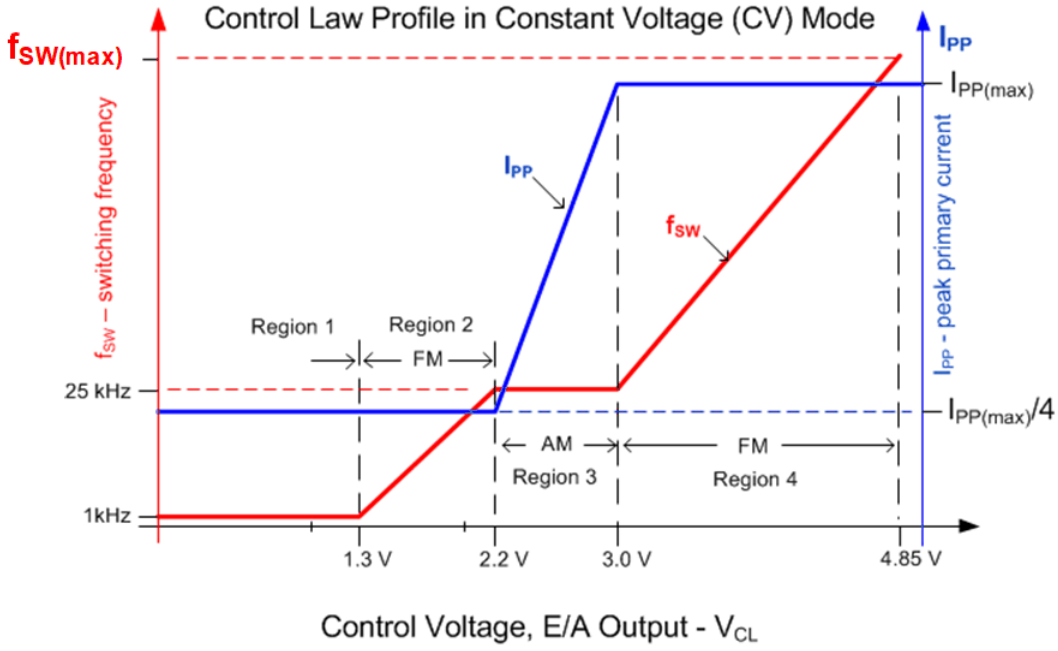


Figure 2-1. Control Law of UCC28704

3 Input (V_{IN}) and Output (V_{OUT}) Voltage Sensing for UVLO and OVP Fault Protection

V_{IN} and V_{OUT} are sensed and measured across the auxiliary winding (V_{AUX}) that is used to provide power to the flyback controller (U1) while the transformer is being energized. Figure 3-1 shows the switching wave form of DCM flyback converter operating near critical conduction. In this figure DRV is the logic level of the flyback controllers gate driver and CS is the voltage measured across the current sense resistor (R_{CS}). When the transformer is being energized during the flyback FETs (Q_A) on-time (t_{ON}) V_{IN} can be measured directly across V_{AUX}. Refer to Equation 1, Figure 1-1, and Figure 3-1 for details.

$$V_{IN} \cong \left| V_{AUX} \times \frac{N_P}{N_A} \right| \quad (1)$$

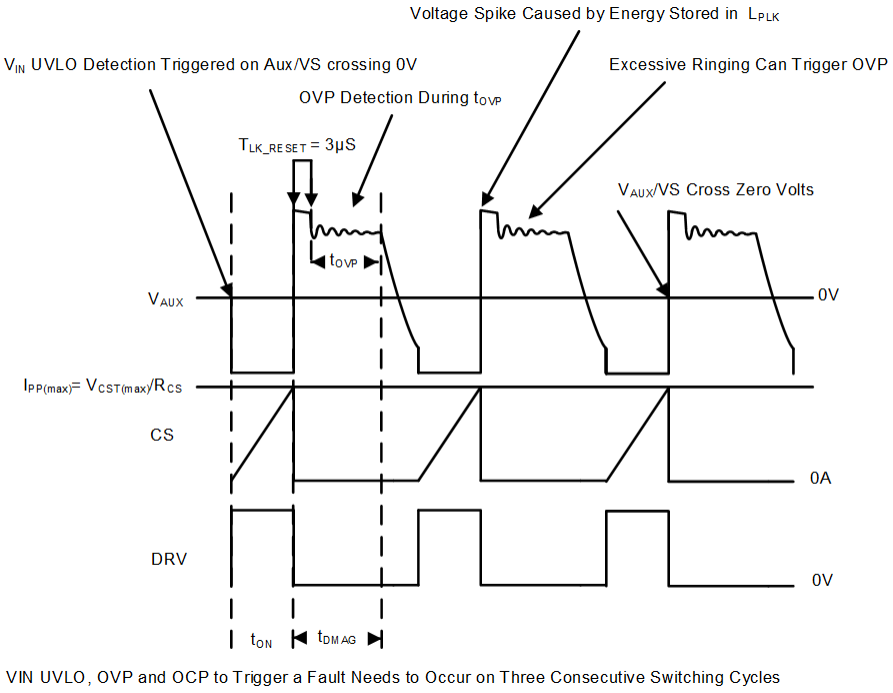


Figure 3-1. Aux, CS, and DRV Signals at Max Load Minimum Line Voltage

The flyback controller can sense V_{OUT} while the transformer is delivering energy after the flyback converters transformer leakage spike that occurs during the T_{LK_RESET} time period has dissipated during t_{DMAG}. Refer to Equation 2 and Figure 1-1 for details.

$$V_{OUT} \cong \left| V_{AUX} \times \frac{N_S}{N_A} \right| \quad (2)$$

To prevent false measurements of V_{OUT} the flyback controllers discussed in this paper have a leading edge blanking circuit. The controllers do not sense V_{OUT} during pre-programed blanking time (T_{LK_RESET}). T_{LK_RESET} moves with loading. For example, at full load, the UCC28704 controller will not sense V_{OUT} for 3 us (T_{LK_RESET}). When operating in the AM band to control the duty cycle, the transformer primary peak current adjusts linearly from I_{PP} to $I_{PP}/4$ to control the duty cycle. When the UCC28704 is operating in the AM band T_{LK_RESET} will be adjusted from 3 µs down to 750 ns as the primary-peak current decreases. When this occurs the flyback converter will go deeper into DCM operation. Refer to Figure 3-2 for details. Please note for this aux winding to sense the V_{OUT} correctly requires the aux winding signal to be as clean as possible between the end of T_{LK_RESET} and the end of t_{DMAG}. This will be discussed in greater detail later in this application note.

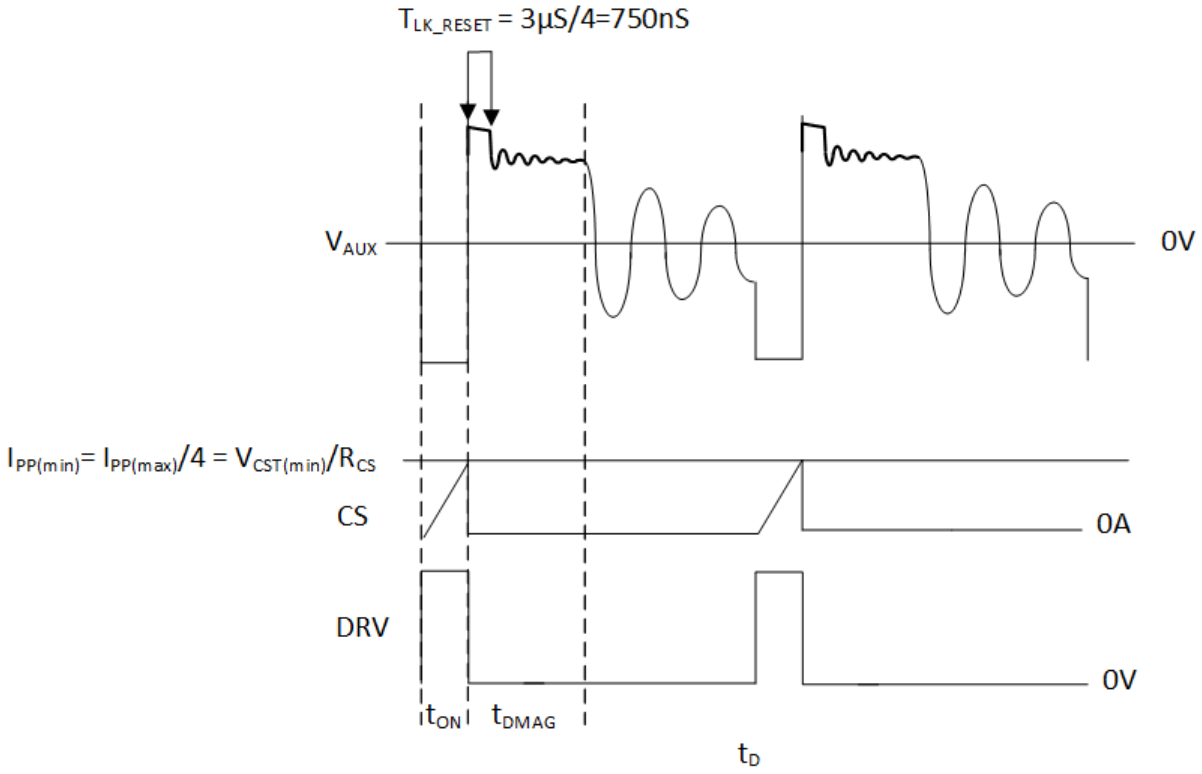


Figure 3-2. V_{AUX}, CS, and DRV While the Flyback Operating Deep into DCM Operation

4 Input Under Voltage Lockout (UVLO) Protection

These flyback controllers have programmable input under voltage detection that can be set and adjusted primary to auxiliary turns ration and properly selecting R_{S1} and R_{S2} Figure 1-1. Refer to the flyback controller data sheet for instructions on programming the input UVLO.

The VS pin of these flyback controllers have an internal clamp on the VS pin that clamps the VS pin to roughly ground (GND) while Q1 is on (t_{ON}), (Figure 3-1 and Figure 3-2). During this this time the current coming out of the VS pin (I_{VSL}) in combination with R_{S1} and the N_P/N_A turns ratio will determine the input voltage level the flyback converter will start at ($V_{IN(run)}$) and what input voltage the converter will stop switching at ($V_{IN(stop)}$). The value $I_{VSL(run)}$ start and $I_{VSL(stop)}$ stop thresholds will vary based on the flyback controller that is used in the design, refer to the flyback controller data sheet for the correct values.

The design presented in Figure 1-1 does not start switching until V_{IN} is greater than 67 V and will stop switching when V_{IN} drops below 23.8 V. Refer to Equation 3 through Equation 6 for details.

$$I_{VSL(run)} = 225\mu A \text{ , VS line sensed run current} \tag{3}$$

$$V_{IN(run)} \geq I_{VSL(run)} \times R_{S1} \times \frac{N_P}{N_A} = 225\ \mu A \times 51.1\ k\Omega \times 5.83 = 67\ V,\ V_{IN} \text{ startup threshold} \tag{4}$$

$$I_{VSL(stop)} = 80\mu A \tag{5}$$

$$V_{IN(stop)} < I_{VSL(stop)} \times R_{S1} \times \frac{N_P}{N_A} = 80\ \mu A \times 51.1\ k\Omega \times 5.83 = 23.8\ V \tag{6}$$

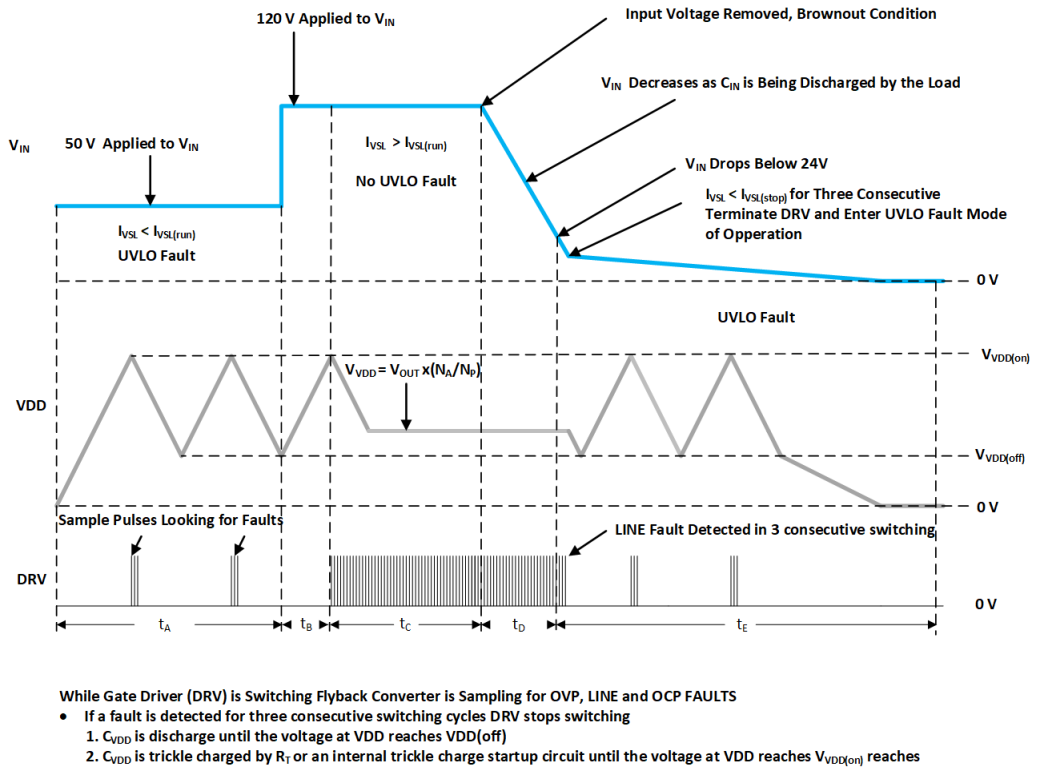
When power is first applied to V_{IN} the VDD capacitor (C_{DD}) trickle charges through R_T of Figure 1-1. Note that some flyback controllers trickle charge the C_{DD} capacitor with an internal JFET startup circuit. The capacitor continues to trickle charge until the flyback controllers turn on threshold is reached ($V_{VDD(on)}$). At this point it will deliver 3 gate drivers pulse to sample V_{IN} and V_{OUT} at the controllers maximum switching frequency ($f_{SW(max)}$). The UCC28704 controls the primary current to $I_{PP(max)}$ /4. At this point t_{LK_RESET} will be reduced to it's minimum blanking time of 750 ns. If the converter detects a UVLO and/or a OVP fault during this time, the gate driver

stops switching and the I_{DD} current will discharge C_{DD} to the flyback controllers turnoff threshold ($V_{VDD(off)}$). After C_{DD} is discharged to $V_{VDD(off)}$, C_{DD} will once again be charged through R_T until the VDD pin reaches $V_{VDD(on)}$. At this point the controller will sample V_{OUT} and V_{IN} again. If the fault is cleared the flyback will continue to operate. If the fault is not cleared switching will stop and the C_{DD} capacitor will be discharged and charged between $V_{VDD(off)}$ and $V_{VDD(on)}$ until the fault is cleared.

$$V_{VDD(on)} = 21\ V \quad (7)$$

$$V_{VDD(off)} = 8\ V \quad (8)$$

Figure 4-1, shows an example of how the input fault protection operates with different input voltages. At the beginning of time interval t_A 50 V is applied at V_{IN}, the C_{DD} capacitor trickle charged up to $V_{VDD(on)}$. The flyback controller samples the input through N_P/N_A turns ratio and will detect an input UVLO fault and stops switching. The controller enters fault mode operation during this time interval. At the beginning of time interval t_B the input voltage is increase to 120 V, however, the flyback controller is still not switching, it waits until C_{DD} is charge up to $V_{VDD(on)}$ to gives three DRV pulses to sample the input voltage. At the beginning of time internal t_C the flyback controller based on input sampling is no longer in a UVLO condition and the flyback converter will continue switching. The C_{DD} capacitor will discharge down to the reflected output voltage determined by the N_A/N_S turns ratio, at this point the flyback controller will be powered by the auxiliary winding (N_A) of T1. At the beginning of time interval t_D the input voltage was removed from V_{IN} simulating a brown out condition. The input bulk capacitor C_{IN} discharges based on the loading on the output of the flyback converter. At the beginning of time interval t_E capacitor C_{IN} will have discharged to a point where the input voltage will cause a UVLO fault. The UVLO fault has to be sampled in three consecutive switching cycles before the flyback controller stop switching. The flyback controller will remain operating in this mode until an input voltage is applied to V_{IN} that causes the I_{VLS} current to be greater than $I_{VSL(run)}$.



While Gate Driver (DRV) is Switching Flyback Converter is Sampling for OVP, LINE and OCP FAULTS

- If a fault is detected for three consecutive switching cycles DRV stops switching
  1. C_{VDD} is discharge until the voltage at VDD reaches VDD(off)
  2. C_{VDD} is trickle charged by R_T or an internal trickle charge startup circuit until the voltage at VDD reaches $V_{VDD(on)}$ reaches

Figure 4-1. Example of UVLO Fault Detection

5 Output Overvoltage (OVP) Protection

These flyback controllers sense the output voltage on V_{AUX} through a resistor divider formed by R_{S1} and R_{S2} and flyback controller's sense pin (VS). If the VS pin exceeds the V_{OVP} threshold for three consecutive switching cycles the controller determines that an OVP event has occurred and gate driver switching stops.

$$V_{OVP} = 4.6\ V \tag{9}$$

$$V_{OUT} \geq \frac{V_{OVP} \times (R_{S1} + R_{S2})}{R_{S2}} \times \frac{N_S}{N_A} \tag{10}$$

The schematic in Figure 1-1 represents a flyback converter that was designed to step down an input voltage (V_{IN}) of 75 V to 390 V DC to a regulated 12 V, 10 W output. The N_S/N_A turns ratio used in this design was 1. In this example, the flyback converter shuts down if V_{OUT} for three consecutive switching cycles is greater than 13.6 V triggering OVP protection, Equation 11.

$$V_{OUT} \geq \frac{4.6\ V \times (26.1\ k\Omega + 51.1\ k\Omega)}{26.1\ k\Omega} \times 1 = 13.6\ V \tag{11}$$

If an OVP fault is detected DRV switching stops and the C_{DD} capacitor is discharged down to $V_{VDD(off)}$. The C_{DD} capacitor trickle charges through R_T until V_{CDD} reaches $V_{VDD(on)}$. At this point the controller gives three DRV sample pulses at $f_{SW(max)}$ controlling the primary current to $I_{PP(max)}$ /4 and t_{LK_RESET} blanking is set to its minimum of 750 ns. Remember that VS will detect an OVP from the end of T_{LK_RESET} to the end of t_{DMAG} . Refer to Figure 3-1 and Figure 3-2 for details. The CDD and DRV behavior during an OVP fault behaves in similar to UVLO fault presented in Figure 4-1.

6 Not Recognizing a UVLO or OVP Fault

Some designers report that on their initial prototypes that flyback controllers using PSR fault sensing do not startup. They report either there are no gate drive pules and or VDD looks like a saw tooth presented in Figure 6-1. In this case, the flyback controller is only going into UVLO, OVP or OCP fault protection. When the fault is cleared, VDD will stop cycling between V_{VDDon} and V_{VDDoff} and the flyback resumes normal operation.

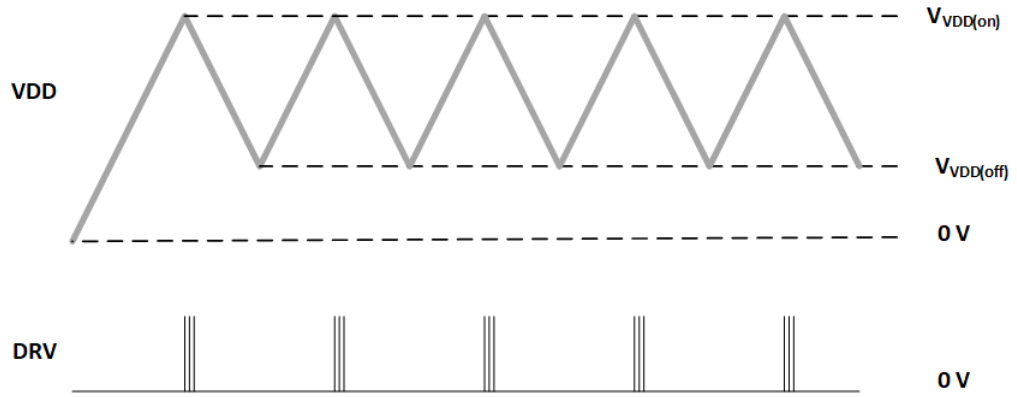


Figure 6-1. VDD Cycling During Between VDD(on) and VDD(off) Indicates a UVLO or OVP Fault

7 Separate Bias Supply Startup Issue and Resolution

When starting up a prototype flyback converter some engineers use a separate bias supply for powering VDD of the flyback controller. Some of these designers have mentioned that there are no gate driver pulses observed and the flyback controller appears to be not functioning. Most of the time the issue is when power was applied to VDD there was no input voltage applied to the flyback converter. The flyback converter had already sampled the input voltage and because there was none present the controller entered input UVLO fault protection. The gate driver stopped switching and the external bias supply is prevents cycling of the VDD pin between $V_{VDD(off)}$, $V_{VDD(on)}$ and $V_{VDD(off)}$ to reset the fault.

To resolve this issue apply the input voltage to V_{IN} that is greater than the UVLO trip point. Then bring the bias voltage to VDD above $V_{VDD(on)}$. The other option is adjust the bias voltage at VDD below $V_{VDD(off)}$ and then above $V_{VDD(on)}$ to reset and clear the UVLO fault.

8 Not Having a Clean Aux Winding Signal

The waveform in Figure 8-1 is a simulation of a flyback converters switch node (V_{SW}), the aux winding voltage (V_{AUX}), and the flyback current sense signal (V_{CS}) of a flyback converter that uses a TVS clamp and no provisions for dampening aux winding ringing. This simulation is based on the flyback converter presented in Figure 1-1 without the circuitry that was highlighted in green.

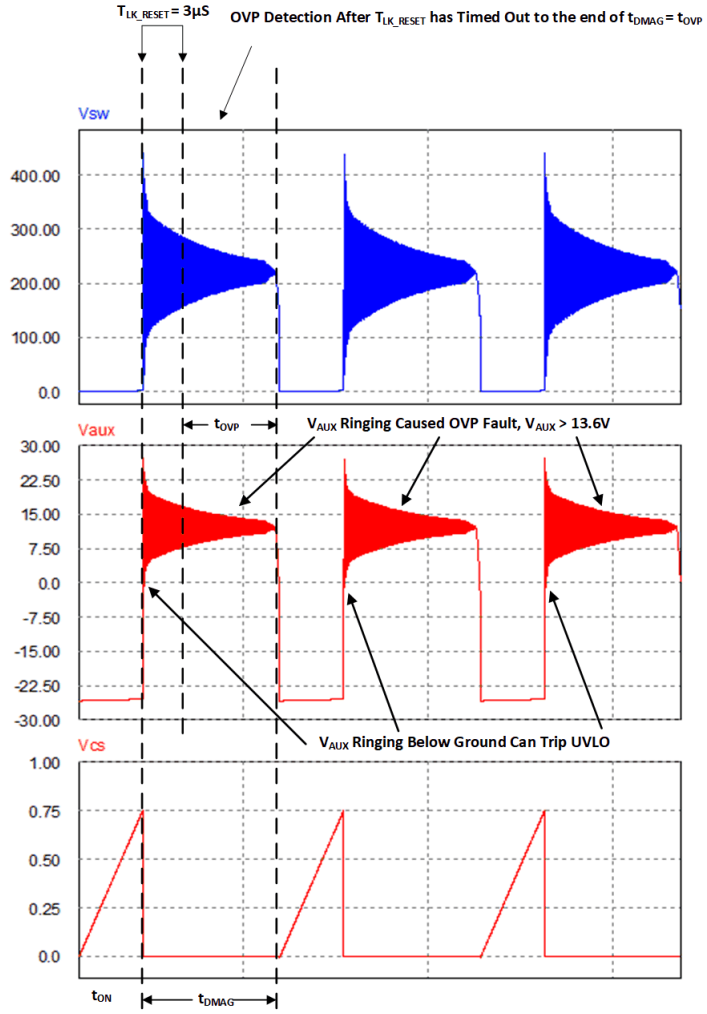


Figure 8-1. Noisy VAUX Falsely Trigger OVP and/or UVLO Fault Protection

The flyback converter was designed to trigger OVP when V_{OUT} and V_{AUX} were greater than 13.6 V. This flyback converter did not have any previsions for dampening the switch node (V_{SW}) ringing cause by parasitic

inductance and capacitance at the switch node. The noise at V_{SW} is couple through the auxiliary to primary turns ratio (N_A/N_P) and will falsely trip OVP fault protection.

The flyback controller samples for an OVP (t_{OVP}) after T_{LK_RESET} has timed out to the end of the transformer demagnetizing time (t_{DMAG}). The waveform in Figure 8-1 shows the ringing on V_{AUX} is greater than 13.6 V during the over voltage protection sampling time (t_{OVP}). This ringing causes the design to shut down and not regulate the output voltage correctly.

The Vaux ringing in Figure 8-1 is excessive and rings down below ground during t_{LK_RESET}. This behavior is known to trigger a UVLO faults and shut down the converter. This is because when the VS pin crosses ground it activates input UVLO fault.

9 Removing Aux Winding Ringing to Resolve False Triggering of OVP and UVLO Faults

Parasitic inductances and capacitances are the major cause of aux winding ringing that can falsely trip OVP is in the design. To help reduce this ringing it is recommended through layout and transformer design that you keep the parasitic inductances and capacitances as small as possible.

The layout section (Section 10) of UCC28704 data sheet (SLUSCA8A) gives recommendations on how to layout the PSR flyback with minimal trace inductance and capacitance. It also has a layout that was constructed based on these recommendations in section 10.2, SLUSCA8.

When selecting and or designing your transformer (T1) it is recommended that a transformer have a primary leakage inductance (L_{PLK}) of less than three percent of the primary magnetizing inductance (L_{PM}), Figure 1-1. This will help to reduce ringing at the switch nodes.

$$L_{PLK} \leq 0.03 \times L_{PM} \tag{12}$$

During layout process, keep the PCB traces in the power stage; as short as, possible. Keep in mind that every inch of trace adds roughly 10 nH of parasitic trace inductance (L_{TRACE}). Keeping the traces as short as possible removes unwanted antennas from the design helping to improve noise impunity as well..

$$L_{TRACE} \cong \frac{10\ \text{nH}}{\text{in}} = \frac{10\ \text{nH}}{2.54\ \text{cm}} \tag{13}$$

Use an RCD clamp (R_A , R_C, C_A, D_A) over a TVS clamp (D_A, D_Z), (Figure 1-1). An RCD clamp will provide dampening at the switch node, where TVS clamp will only clamp the voltage when the switch node rings above the clamp voltage and provides very little to no dampening. Set the R_A and C_A time constant of the clamp to greater than 10 times the maximum switching period, Equation 14 and Equation 15. Please note for safety the designer want to use D_Z to clamp V_{SW} as well.

$$R_A \times C_A \geq \frac{10}{f_{SW(max)}} = \frac{10}{100\ \text{kHz}} = 100\ \mu\text{s} \tag{14}$$

$$R_A \times C_A = 511\ \text{k}\Omega \times 1\ \text{nF} = 511\ \mu\text{s} \tag{15}$$

To reduce excessive ringing across the secondary (V_{SEC}) winding it will couple into V_{AUX} through the auxiliary to primary turns ratio. The waveform presented in Figure 9-1 shows ringing on the secondary of simulated from a 390 V to 12 V, 10 W, flyback converter. Excessive ringing present on V_{SEC} will couple onto V_{AUX} and if it severe enough can cause and OVP. As a result, the design will not lose output voltage regulation causing the design to misbehave.

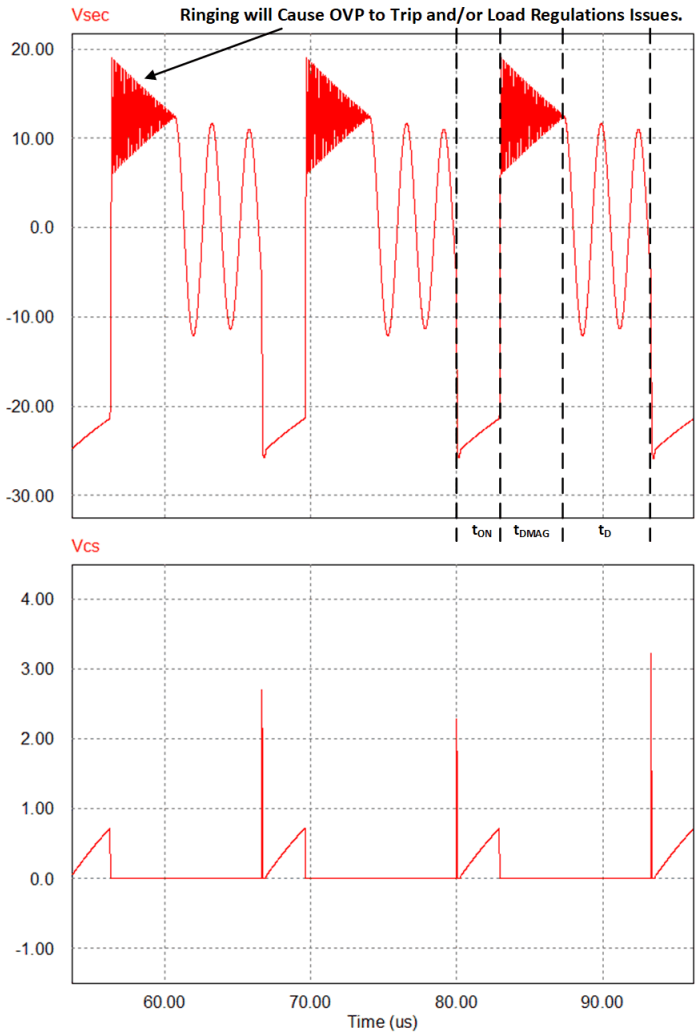


Figure 9-1. Flyback Secondary Voltage with Excessive Ringing

The cycle by cycle energy transfer between parasitic leakage inductances and parasitic switch node capacitances causes ringing at the flyback converter switch nodes. This ringing will couple through the flyback converter's switch nodes to V_{AUX}. Excessive voltage ringing on V_{AUX} can accidentally trigger an OVP.

The energy cycling by the transformer's primary leakage inductance (L_{PLK}) and primary switch node (C_{SW1}) is one contributor this high frequency V_{AUX} ringing that causes OVP issues. Another contributor is the energy cycling by the transformer's secondary leakage inductance (L_{SLK}) and the secondary switch node capacitance (C_{SW2}). This excessive ringing can generally be dampened with an RC snubber (R_B, R_C) across the converters output rectifier (D_C) shown in Figure 9-2.

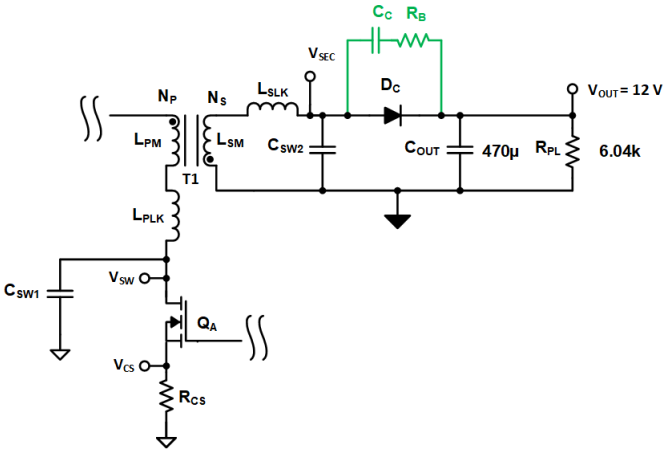


Figure 9-2. Simplified Flyback Schematic with Parasitic.

To give an example of how to implement a snubber circuit, a 12 V, 10 W flyback design was created and simulated. The waveforms from this circuit are presented in Figure 9-2 and would trigger an OVP fault incorrectly due to ringing on the secondary winding (V_{SEC}) through the transformer to V_{AUX}.

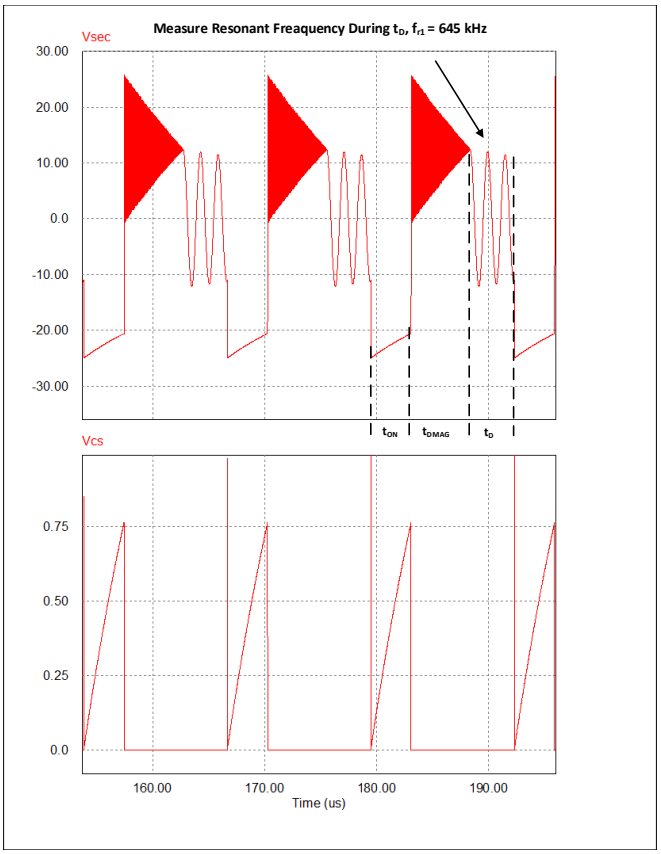


Figure 9-3. Measuring Low Frequency Ringing to Calculate C_{SW2}

To setup the snubber requires knowing or calculating the transformer's primary (L_{PM}) and secondary L_{SM} magnetizing induct, L_{SLK}, C_{SW2}. With this information the secondary magnetizing inductance (L_{SM}) can be calculated by knowing the transformer primary to secondary turns ratio (N_P/N_S) and primary magnetizing inductance (L_{PM}) which are given in the transformer data sheet and using equations Equation 16 and Equation 17. For this example the transformer had an L_{PM} of 680 µH and N_P/N_S of 5.8. L_{SM} for this design was calculated to be 20 µH.

$$\frac{N_P}{N_A} = 5.8 \tag{16}$$

$$L_{SM} = \frac{L_{PM}}{\left(\frac{N_P}{N_S}\right)^2} = \frac{680\ \mu H}{5.8^2} \cong 20\ \mu H \tag{17}$$

To calculate C_{SW2} requires knowing L_{SM} and studying the V_{SEC} waveform and measuring the low frequency ringing (f_{r1}) during the t_D time interval, Figure 9-3. f_{r1} should be measured when the flyback converter is operating at light load and operating deep into DCM. In this example f_{r1} was measured to be 645 kHz. C_{SW2} can then be calculated using Equation 19, which for this example was 3 nF

$$f_{r1} = 645\ kHz \tag{18}$$

$$C_{SW2} = \frac{1}{(2 \times \pi \times f_{r1})^2 \times L_{SM}} = \frac{1}{(2 \times \pi \times 645\ kHz)^2 \times 20\ \mu H} \cong 3\ nF \tag{19}$$

The next step is to measure the high frequency ringing (f_{r2}). during time interval t_{DMAG}, Figure 9-4. This resonant frequency is caused by the interaction of C_{SW2} and L_{SECP}. Based on f_{r2} and C_{SW2}, L_{SECP} can be calculated using Equation 21. With a measured f_{r2} of 14 MHz and C_{SW2} of 3 nF the calculated L_{SECP} is approximately 43 nH.

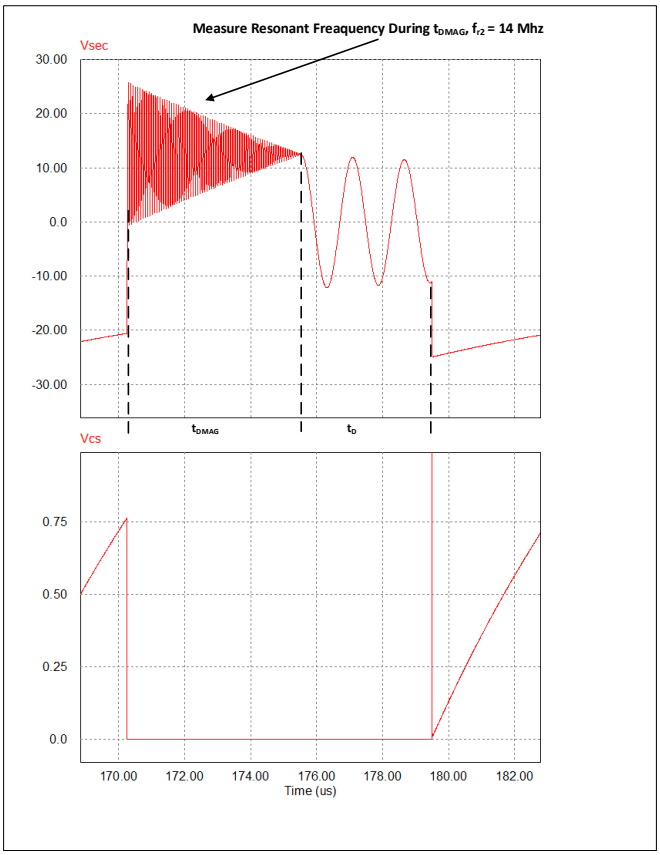


Figure 9-4. Measure High Frequency Ringing During Time Interval t_{DMAG}

$$f_{r2} = 14\ MHz$$,Measured high-freqeunecy ringing durring interval t_{DMAG} (20)

$$L_{SECP} = \frac{1}{(2 \times \pi \times f_{r2})^2 \times C_{SW2}} = \frac{1}{(2 \times \pi \times 14Mhz)^2 \times 3nF} \approx 43nH \tag{21}$$

Snubbing resistor R_B is chosen to critically dampen the high-frequency ringing and can be calculated using Equation 22.

$$R_B = \frac{1}{Q}\sqrt{\frac{L_{SECP}}{C_{Sw2}}} = \frac{1}{1}\sqrt{\frac{43\ nH}{3\ nF}} \cong 3.8\ \Omega \quad (22)$$

A standard resistor was chosen for resistor R_B :

R_B = 3.83

The snubbing capacitor C_C was chosen based on Equation 23, based on the converter's maximum nominal switching frequency (f_{SW}). By setting C_C this way the snubber will only be active for 1% of the switching period, keeping snubber losses to a minimum. The flyback design being evaluated had a f_{SW} of 75 kHz.

$$C_C = \frac{0.01}{f_{SW} \times R_B \times 5} = \frac{0.01}{75\ kHz \times 3.8\ \Omega \times 5} \cong 7\ nF \quad (23)$$

A standard capacitance value for C_C was chosen for the design:

C_C = 6.8 nF

The snubber components that were selected for R_B and R_C were applied to the circuit presented in Figure 1-1 and Figure 9-2. The result was the secondary winding was critically damped. Please refer to Figure 9-5 for damped waveforms results.

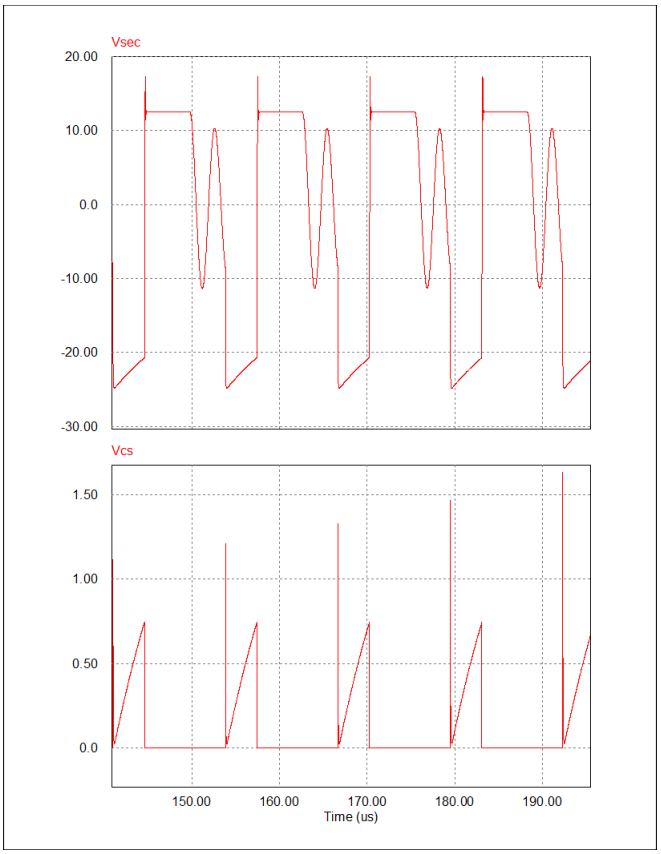


Figure 9-5. Snubber, RB 3.83 ohms, CC = 6.8nF

10 Noise on CS Pin Tripping Over Current Protection (OCP)

To help protect the FET from damage, these flyback controllers have an over current protection (OCP) circuit that trips when the CS pin senses a current sense signal that is 2X the nominal peak. In the case of the UCC28704 this OCP trip point is 1.5 V.

When first turning on a FET there is a leading-edge current spike caused by the charging the gate to source capacitance of the FET used in the design. This generally can be seen on the current sense signal (V_{CS}), please refer to Figure 10-1 for details. To prevent the controller from falsely tripping OCP due to this leading-edge gate

driver spike the flyback controller uses current sense leading edge blanking. The flyback controller will not sense the current sense signal during a predetermined blanking time (T_{CSLEB}). In this example, the UCC28704 was evaluated and had a T_{CSLEB} of 255 ns. Please note this time will vary based on flyback controller that is used in the design.

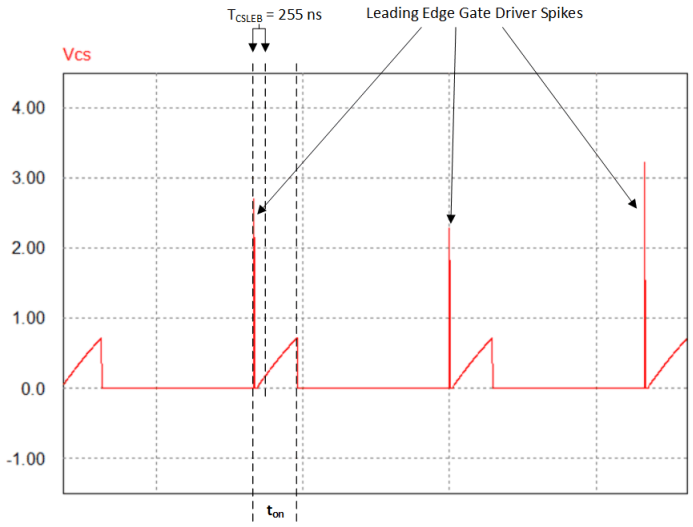


Figure 10-1. CS Leading Edge Blanking Helps Prevent False OCP Shutdown

These flyback designs sometimes shut down due to noise on the CS pin (V_{CS}). This behaivor is not related to OVP or input UVLO sensing. This occurs by noise being coupled into the circuit through parasitic capacitance and/or poor layout. The problem occurs if these noise spikes are outside the T_{CSLEB} blanking window and are larger than the OCP trip point. Please refer to Figure 10-2 for details.

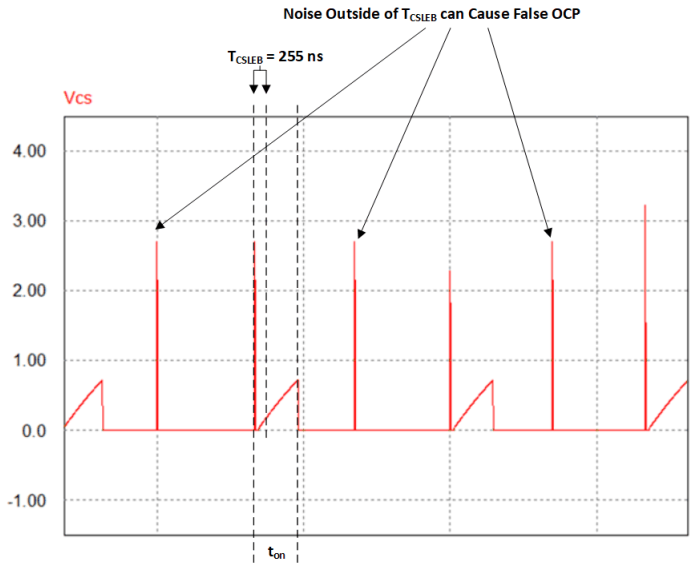


Figure 10-2. Noise Spikes Outside the T_{CSLEB} Window will Cause a False OCP Fault

A poor PCB layout can cause this fault as well. It is recommended to avoid this that the designer fallow the layout guidelines given in the TI flyback controller data sheets.

As an alternative, these noise spikes can be removed by using a low pass RC filter formed by R_{LC} and C_S presented in Figure 1-1. Resistor R_{LC} is selected based on data sheet requirements and filter capacitor C_S sets the pole of the low pass filter that can be adjusted. Select C_S to put the filter pole at 10 times the converters maximum frequency. Equation 24 can be used to calculate C_S. Please note if the flyback was designed for a maximum frequency of 75 kHz and had an R_{LC} resistor of 1 k ohm it would require a C_S of roughly 212 pF for snubbing.

$$C_S \leq \frac{1}{2 \times \pi \times 10 \times f_{SW(max)} \times R_{LC}} = \frac{1}{2 \times \pi \times 10 \times 75\ kHz \times 1\ k\Omega} \cong 212\ pF \quad (24)$$

11 Summary

Remember when designing a DCM flyback controller that uses the transformer aux winding for fault sensing to sample the input and output voltage. It is critical that the aux winding waveform is as clean as possible with as little ringing on it as possible. Some designers struggle with this ringing caused by parasitic inductances and capacitances that cause false OVP or UVLO faults. This application note describes how to prevent false OVP and UVLO faults, A RCD clamp and or a snubber across the flyback converter's output rectifier is recommended to dampen the aux winding ringing.

12 References

1. Texas Instruments, *Trouble Shooting TI PSR Controllers*, application report.
2. Texas Instruments, *UCC28701,2,3 Constant-Voltage, Constant-Current Controller With Primary-Side Regulation*, data sheet.
3. Texas Instruments, *UCC28704 High-Efficiency Off-Line CV and CC Flyback Controller with Primary-Side Regulation (PSR)*, data sheet.
4. Texas Instruments, *UCC28710/1/2/3 Constant-Voltage, Constant-Current Controller With Primary-Side Regulation*, data sheet.
5. Texas Instruments, *UCC28740 Constant-Voltage Constant-Current Flyback Controller Using Optocoupled Feedback*, data sheet.
6. Texas Instruments, *UCC28742 High-Efficiency Flyback Controller with Optocoupler Feedback*, data sheet.
7. Texas Instruments, *UCC28910, UCC28911 High-Voltage Flyback Switcher with Primary-Side Regulation and Output Current Control*, data sheet.

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