

Application Note

BQ79718-Q1 Daisy Chain Communications



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ABSTRACT

This application note is designed to demystify the bq7971x daisy chain communications interface when stacking multiple devices for high voltage applications. The goal is to provide a deeper understanding of the protocol when evaluating the device. Additionally, this report provides recommended isolation components and typical application practices for system designs to take full advantage of designing with the daisy chain interface.

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1 Introduction

The daisy chain communication interface on the bq7971x family of devices is a proprietary protocol developed by Texas Instruments. It is designed using differential signaling to minimize Electro-Magnetic Susceptibility (EMS) and strengthen Bulk Current Injection (BCI) immunity. The differential communication transmits complement data on the COM*P and COM*N pins, respectively. This interface is bi-directional and half duplex, and, therefore, has a transmitter (TX) and receiver (RX) on the COMH (high-side) and COML (low-side) interfaces.

The device supports the use of transformers or capacitors to electrically isolate the signals between devices in the stack. There are configurations where the devices are physically located on the same board or located in entirely separate packs connected with twisted pair wiring. For applications that have multiple devices on the same PCB, a single capacitor is connected between the COMH/L pins of the devices. For extremely noisy environments and stringent EMI/EMC requirements, additional filtering can be required. For devices that are separated by cabling, additional isolation components are used.

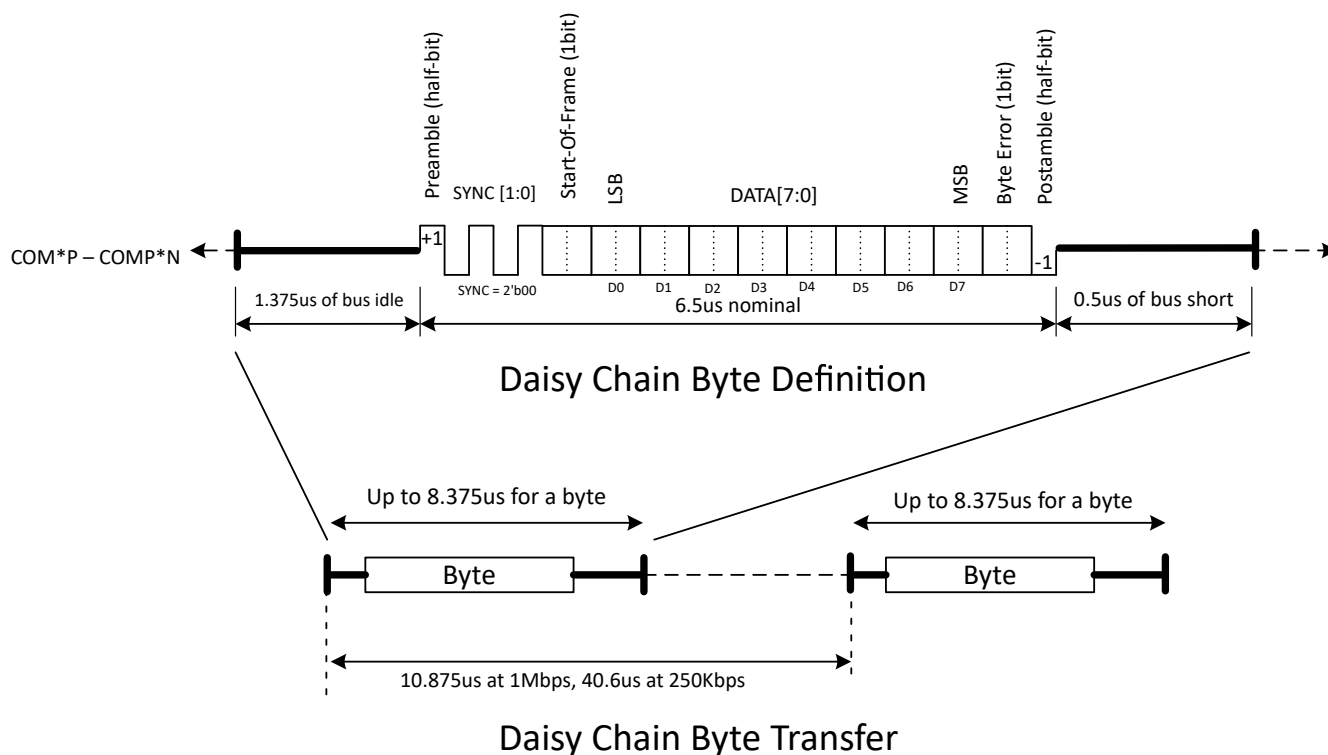


Figure 1-1. Daisy Chain Byte Level Definition

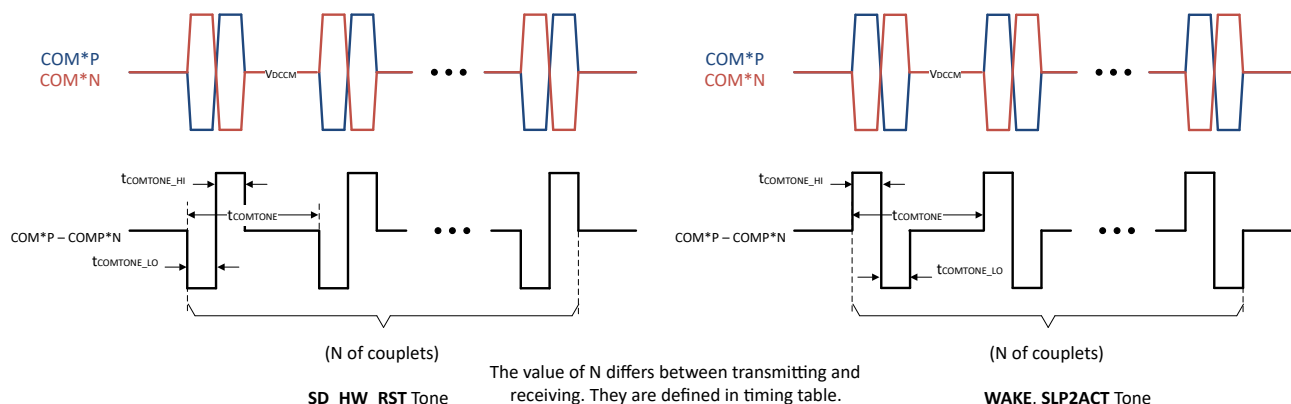


Figure 1-2. Communication Tones

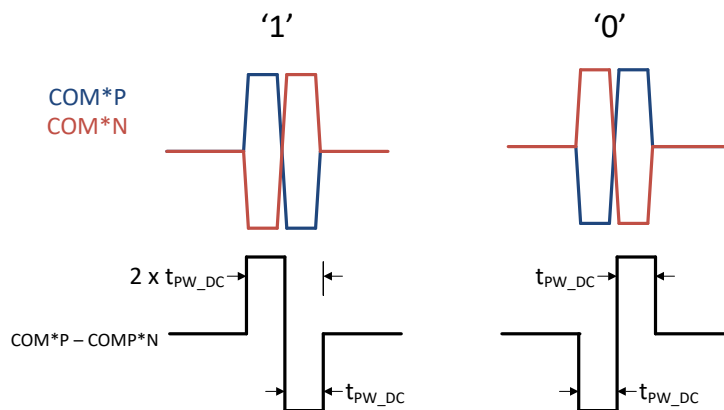


Figure 1-3. Daisy Chain Bit Level Definition

2 Receiver Topology and Common Mode Voltages

The daisy chain is bi-directional and half duplex, and, therefore, has a transmitter (TX) and receiver (RX) on the COMH and COML interfaces. The TX and RX functions are controlled automatically by the hardware based on the device's base/stack detection. When a WAKE ping/tone is received, the communication direction is set by CONTROL1[DIR_SEL] and the COMM_CTRL[TOP_STACK] configurations. See Auto Addressing in the bq79718-Q1 data sheet for details. Additionally, a user overwrite to take over the complete control of the COMH and COML is available under communication debug mode using the DEBUG_CTRL_UNLOCK, DEBUG_COMM_CTRL1, and DEBUG_COMM_CTRL2 registers. See the Debug Control Registers section for more details in the bq79718-Q1 data sheet.

The RX topology of the bq7971x devices is similar to RS485 but with added design mechanisms to attenuate common mode voltages of up to $\pm 25V$ due to noisy conditions. This common mode voltage limit for the differential signals is best explained by the chart in Figure 2-1.

In the event of a common mode voltage swing due to noisy conditions such as EV inverter noise or Bulk Current Injection (BCI) testing – the common mode voltage seen at the COM pins may oscillate up to $\pm 25V$ depending on the isolation components and current injected. The device is designed to withstand this type noise level up to $\pm 25V$ because of the internal attenuation that allows the 5V transceivers to handle the response and therefore the differential signal would still remain intact. Above this $\pm 25V$ level, there is risk of clamping the internal ESD structure or causing damage to the COM pins. This limit should be taken into consideration when determining BCI limits and testing.

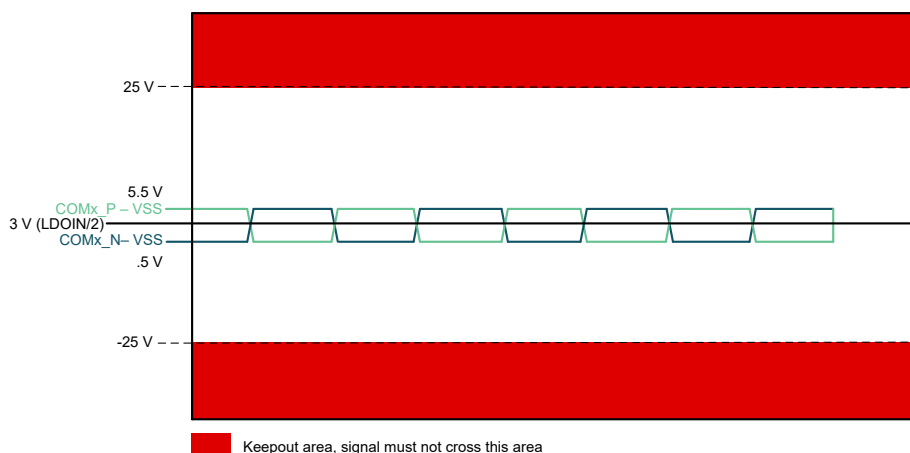


Figure 2-1. Common Mode Voltage Diagram

3 Signal Integrity Requirements

Proper receiver waveform timing and thresholds are critical factors for the internal digital circuitry to correctly interpret tones and data communications. Note that these factors can be affected by isolation component choices and cabling.

3.1 Receiver Timing Requirements

As [Figure 3-1](#) shows below, the high and low timing differs between a tone signal (1 μ s pulse width at 500 kHz) or data communications (approximately 250ns pulse width at 2MHz) waveform. However, both tones and data communications share similar rise/fall times and must both be rectangular waveforms with a maximum decay below 1V. Note that the timing for the $t_{\text{high}}/t_{\text{low}}$ refers to the time that the signal must be above or below the proper threshold value for the integration to succeed. If the signal is noisy during this $t_{\text{high}}/t_{\text{low}}$ time and droops below the threshold value for some time - then there is risk of the signal being detected. We expect that roughly 1 μ s $\pm$ 8% for tones and 250ns $\pm$ 20ns for data communications is the allowed timing variation for these signals to still be properly detected.

3.2 Receiver Threshold Requirements

The thresholds at which the internal digital circuitry is able to properly detect a high vs. low transition are shown in [Figure 3-1](#). A good quality waveform will have a differential voltage above 1.8V (and below -1.8V on the negative side). It typically resembles a square wave with rounded edges.

The image below shows a poor quality or drooping waveform that still meets the criteria for a valid communication. The first diagram is showing a starting voltage (VSTART) of 1.7V with an ending voltage (VEND) of 1.2V. The second diagram shows a second scenario where the starting voltage (VSTART) is only 1.6V with an ending voltage (VEND) of 1.3V. If the starting amplitude is not at least 1.6V, then the bit will not be detected, regardless of ending amplitude. These types of drooping waveforms most often are seen when there are two adjacent bits of opposite polarity, forming what can be referred to as a double-bit.

Note

The color red in [Figure 3-1](#) indicates the region that the signal may or may not be detected (poor quality waveform zone) whereas orange indicating the area the area near the triggering threshold range. A good quality waveform would remain in the green region above 1.7V for the duration of the positive pulse width.

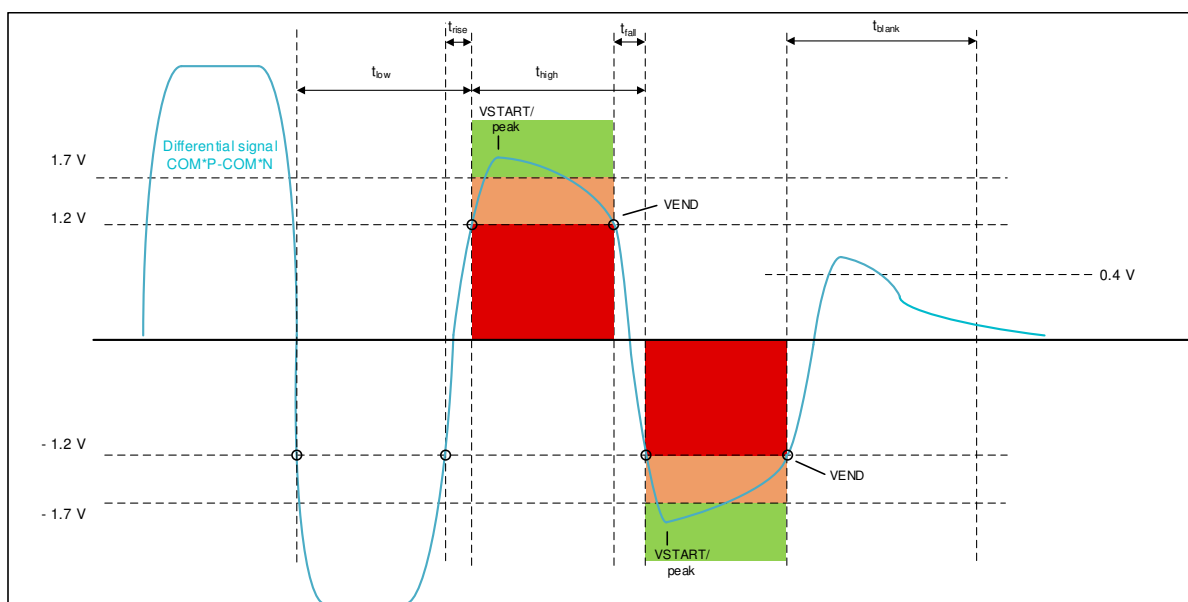


Figure 3-1. Differential Signal Eye Diagram - 1.7 V VSTART

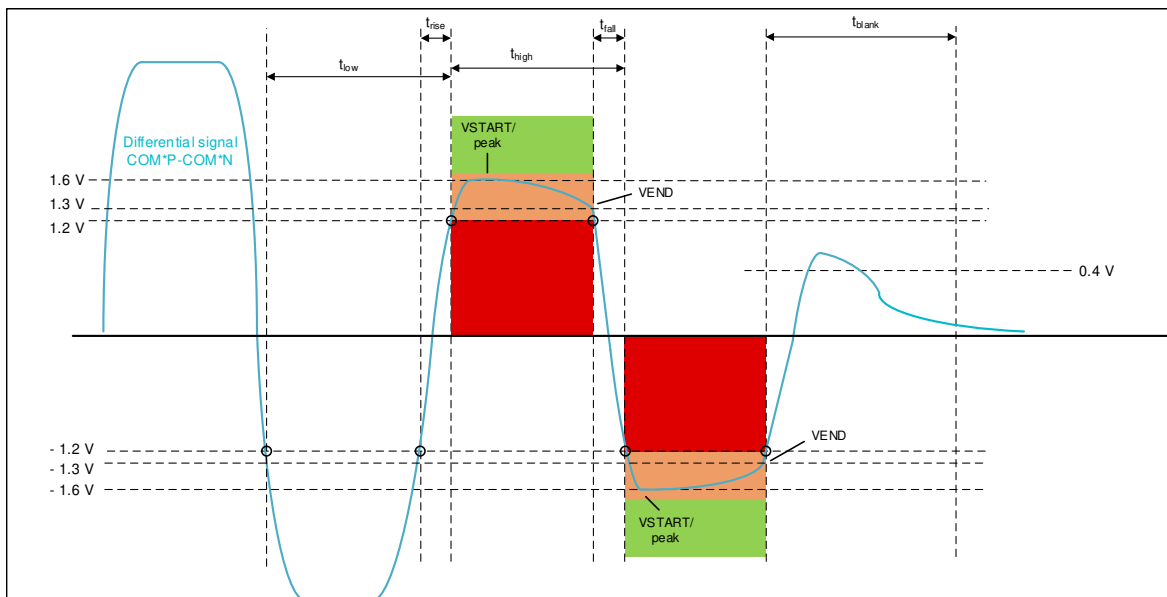


Figure 3-2. Differential Signal Eye Diagram - 1.6 V VSTART

Table 3-1 gives the specific timing and voltage requirements for valid daisy-chain communication. Variations of +/-1 HFO cycle (31.25ns) are within recommended timing limits. Outside of this range, we recommend customers to utilize the IC's built-in fault monitoring features to ensure proper communication is achieved.

Table 3-1. Timing Chart

	Parameter	Conditions	Min	Typ	Max
t_{high}	positive pulse width	COMP-COMN from +1.2V of rising edge to -1.2V of next falling edge	220ns	250ns	300ns
t_{low}	negative pulse width	COMP-COMN from -1.2V of falling edge to +1.2V of next rising edge	200ns	250ns	280ns
t_{rise}	Rising slew rate	COMP-COMN from -1.2V to +1.2V of rising edge			60ns
t_{fall}	Falling slew rate	COMP-COMN from +1.2V to -1.2V of falling edge			60ns
V_{start}	Starting amplitude	If ending amplitude is above 1.3V	1.6V		
V_{start}	Starting amplitude	If ending amplitude is between 1.2V and 1.3V	1.7V		
t_{blank}	Blanking time	After last bit	4us		
Wake Tone (t_{high}/t_{low})	Wake Tone pulse widths	COMP-COMN from +1.2V of rising edge to -1.2V of next falling edge during and vice versa for Wake tones	1us		

Figure 3-3 shows the threshold required for interfacing with the BQ79600 device. The primary difference is the threshold and timing references are based on a 1.8V threshold.

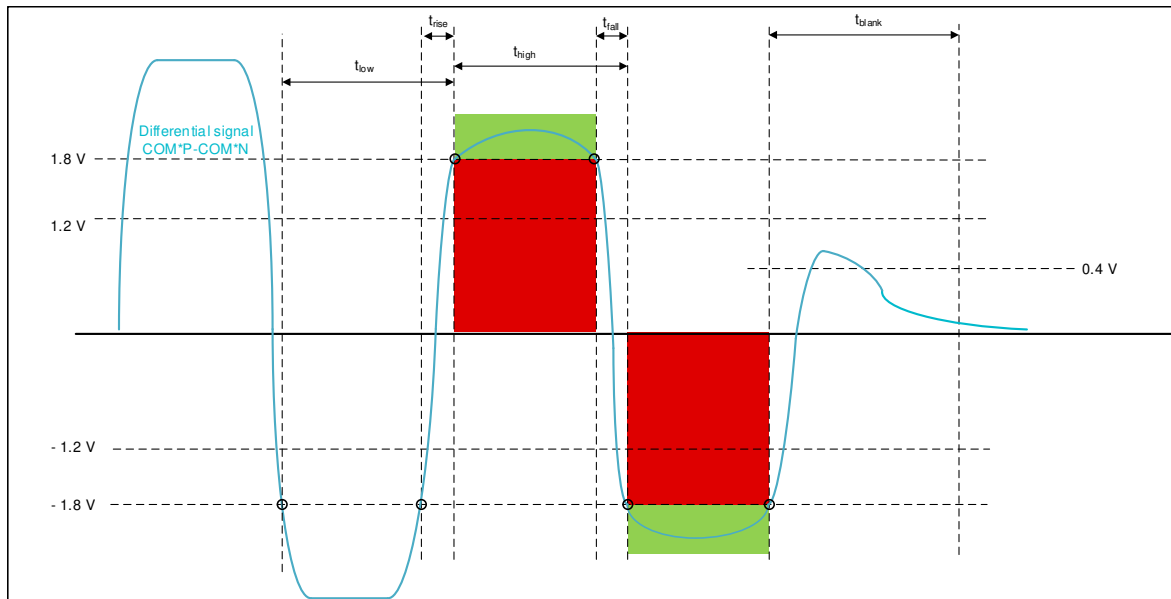


Figure 3-3. Differential Signal Eye Diagram - BQ79600

4 Debug Fault Registers

The bq7971x devices come equipped with many fault registers that help the user determine the cause and effect of signal noise between devices. Most importantly, TI recommends always checking the `FAULT_SUMMARY` register to determine if an error occurs during communication. If the `FAULT_SUMMARY` flags a `FAULT_COMM` error then the next steps are to read back the `FAULT_COMM` register and `DEBUG` registers to identify the exact issue.

5 Isolation Types

With the bq7971X family of devices, we offer several options for designing an isolation interface between stacked devices in a complete system. These include:

1. Transformer, Galvanic, or Inductive
2. Capacitive and Choke
3. Capacitive Only

Note that individual component properties and characteristics can affect signal integrity, robustness, and EMC performance. In the following sections there are detail of each isolation type and recommended component choices.

5.1 Transformer Isolation

For longer daisy chain cable lengths or highly noisy applications, the system may require the use of transformer isolation to provide the most robust form of communications. This design choice allows the daisy chain communications to be galvanically isolated and withstand higher sources of noise compared to capacitively coupled communications. It is recommended to use a certain set of parameters to meet automotive qualified temperature, voltage, and reliability ratings. It is recommended to choose parts that remain in the 300– 1000 μ H inductance range for best performance. [Table 5-1](#) is a list of recommended part numbers that were tested using the bq7971X devices. Choosing a part outside of this list or parameters would require thorough validation on the system designer side to make sure that the communication is robust over temperature, can withstand rapid communication transactions, and provides proper EMI filtering. Note that it is important and highly recommended to use the same transformer part number on both sides of a daisy chain interface (COML of top device and COMH of connected lower device).

Table 5-1. Recommended Transformer Part Numbers

Part Number	Supplier	Inductance (OCL) μ H	Height (mm)
HMU1228NL	Pulse	300-370	6.85
SM91525AL	Bourns	300-1000	4.95
XFBMC29-BA09-B	XFMRS	350	5.00

5.2 Capacitor Only Isolation

For low noise environments or devices mounted on the same pcb, typically it is best to select capacitors only for isolation. TI recommends these capacitors to be 2.2nF, high voltage rated (twice the voltage of the total pack voltage of the system), and automotive qualified. Our reference schematic uses the 1206J2K00222KXR supplied by Knowles. It is possible to use a capacitor of up to 10nF for this isolation.

5.3 Capacitor and Choke Isolation

If the system uses capacitive based isolation, then it can be required for longer daisy chain cable lengths or highly noisy applications to use an additional common-mode choke filter in series with the capacitors. For these applications, it is recommended use an automotive grade 100 μ H common-mode filter minimum for proper operation. To achieve the best performance in noisy environments, use dual common-mode filters (100 μ H and 470 μ H). For single common-mode filter applications, the TDK 51 μ H 2.8k Ω choke (ACT45B-510-2P-TL003) is recommended. For dual common-mode filter applications, the TDK 100 μ H 5.8k Ω choke (ACT45B-101-2P-TL003) and Würth 470 μ H 2.2 k Ω (744242471) are recommended. Note that the common mode impedance specification is most critical to suppressing the higher noise sources. The same principle can be applied when determining choice of a ferrite bead.

6 Mixed Isolation Circuits Using bq79600-Q1

When using the bq79600-Q1 device as the communication bridge in combination with any variant of the bq79718-Q1 device as the stack device, it is important to validate the robustness of the isolation interface between the base and first stack device. This is because the devices are designed to support a mixed isolation type on the COMH side of the base vs. the COML of the stack device. Typically this means that the bq79600-Q1 will have a transformer from the above list, and then the user may select any of the 3 supported isolation types for the bq79718-Q1 stack device side (that is the same transformer part number on both sides if transformer isolation is desired). Every scenario with different transformer, cap, and choke part numbers mixed has not been tested so it is important for the user to ensure that the signal integrity is maintained after choosing isolation components. Schematically, the key difference is that the decoupling capacitors on the bq79600-Q1 circuit are 100pF compared to 220pF for the bq79718-Q1 device.

6.1 Isolation when using BQ79600-Q1 Reverse Wake Up Feature

The BQ797xx can be configured to work with the Reverse Wake Up feature in the BQ79600-Q1. [Table 6-1](#) gives the voltage requirements needed for signals to be detected by the BQ79600-Q1 for using the reverse wake up feature.

Table 6-1. Voltage thresholds for receiving data, tones and sniff detection

Parameter		BQ79600	BQ797xx
COMM port data received threshold range ($V_{COMP} - V_{COMN}$)	V_{COMM_DATA}	> 1.6V	> 1.3V in ACTIVE mode > 1V in SLEEP and SHUTDOWN mode
COMM port HB/Fault tone received threshold range ($V_{COMP} - V_{COMN}$)	V_{COMM_TONE}	> 1.6V	
SNIFF detector threshold	$V_{VAL\_THR\_P}$	> 3.4V (rising swing on COMHP)	N/A

If the BQ797xx-Q1 isolation to a BQ79600 is cap isolation, a modification to the transformer isolation on the BQ79600-Q1 side is required for utilizing reverse wakeup with signals that meet the voltage dictated above. Shown in [Figure 7-1](#), the changes are:

- Transformer ratio increases from 1:1 to 1:1.5
- Termination resistance increases from 1-kOhm to 4-kOhm

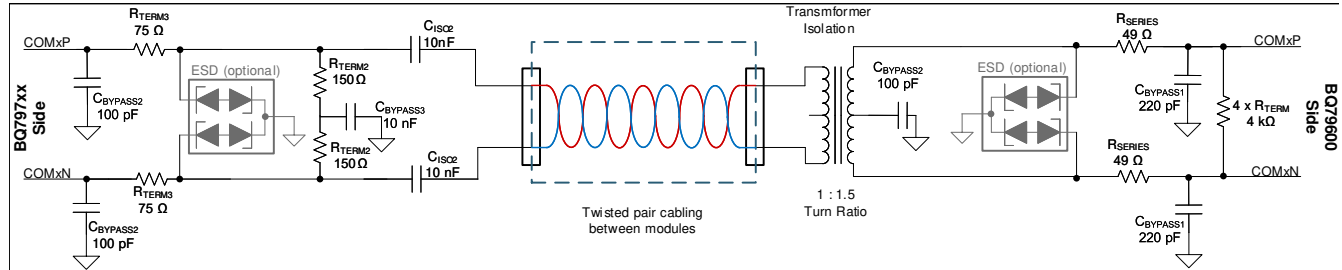


Figure 6-1. Isolation from BQ797xx-Q1 to BQ79600-Q1

7 Noise Immunity and Emissions

To determine that the bq7971x daisy chain architecture can be considered in automotive/EV applications, several EMI/EMC tests were performed to showcase the robustness. However, these results vary based on schematic or PCB layout design choices, external noise sources, distance from UART/MCU connections, and calibration equipment. Reach out to the TI sales team or support team representative to receive more details on these specifications passed. The following is a list of common practices to replicate best case results.:

1. Layout Recommendations in the bq79718-Q1 data sheet
2. Closely follow our reference EVM schematic and layout detailed in the EVM user's guide
3. Common practices include isolating UART/MCU connections with ferrite beads and filtering components.

8 Daisy Chain Cable Selection

Typically daisy chain testing is done with minimally short, symmetrical, matching impedance on-board pcb traces between devices or a 1 - 1.7m long twisted pair cabling between two separate pcbs or evaluation modules. However, depending on proper layout, isolation, and delay between commands - the communication protocol can support cabling up to 20-40m if needed but this would not be recommended for most robust designs. The cabling material, twisting, and connectors can play a role in communication robustness but we do not provide strict requirements for these factors due to the flexibility provided to many different system architectures. However, testing has been completed with basic copper twisted pair wiring (no shielding) for many of our temperature and EMC testing. Although it may be best to use PP material rather than PVC material which changes the dielectric constant of the cable over time and temperature and thus has an impact on the transferred signals as opposed to more expensive, but better PP material. Typically a rule of thumb is to support at least 1-2 twists per cable inch and start the twisting very close to the connectors. This will help reduce external effects of EMI interference.

9 Summary

Overall, the proprietary daisy chain protocol was designed to minimize electromagnetic susceptibility and to be robust against electromagnetic interference. When designing with the daisy chain protocol, measuring the communication waveforms to make sure the timing and threshold meet the requirements for the internal circuitry to correctly interpret data is essential. Additionally, choosing proper isolation components and circuitry on the communication lines is crucial to make sure the daisy chain waveforms are robust against high noise environments. Choosing between transformer, capacitive + choke, and capacitive only isolation must be thoroughly thought out by the system designer.

10 References

- Texas Instruments, [BQ79600-Q1 Automotive SPI/UART Communication Interface Functional-Safety Compliant With Automatic Host Wakeup](#), data sheet.
- Texas Instruments, [BQ79718-Q1 Functional Safety-Compliant Automotive 18S Battery Monitor](#), data sheet.

11 Revision History

Changes from Revision * (September 2023) to Revision A (December 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated <i>Recommended Transformer Part Numbers</i> table.....	6

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